# CRYOGENIC TEMPERATURE CHARACTERISTICS OF BULK SILICON AND SILICON-ON-SAPPHIRE DEVICES

by

STEVEN ALLEN MELTON

B.S., Kansas State University, 2010

A THESIS

submitted in partial fulfillment of the requirements for the degree

MASTER OF SCIENCE

Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2012

Approved by:

Major Professor
Dr. William Kuhn

# Copyright

STEVEN ALLEN MELTON

2012

# Abstract

Studies of Silicon-on-Sapphire (SOS) CMOS device operation in cryogenic environments are presented. The main focus was to observe the characteristic changes in high, medium and low threshold SOS NFETs as well as SOS silicide blocked (SN) resistors when the operational temperature is in the devices' freeze-out range below 77 Kelvin. The measurements taken will be useful to any integrated circuit (IC) designer creating devices based on an SOS process intended to operate in cryogenic environments such as superconducting electronics and planetary probes.

First, a 1N4001 rectifier and a 2N7000 NFET were tested to see how freeze-out effects standard diode and MOS devices. These devices were tested to see if the measurement setup could induce carrier freeze-out.

Next, SOS devices were studied. Data was collected at room temperature and as low as 5 Kelvin to observe resistance changes in an SN resistor and kink effect, threshold voltage shifts and current level changes in transistors. A 2μm high threshold NFET was tested at room temperature, 50 Kelvin, 30 Kelvin and 5 Kelvin to observe effects on I-V curves at different temperatures with-in the freeze-out range. A 2μm medium threshold NFET was tested down to 56 Kelvin to see if the behavior is similar to the high threshold FET. A 2μm intrinsic, or low threshold, NFET was also tested with the assumption it would be the most susceptible to carrier freeze-out. All of the devices were found to behave well with only mild effects noted.

# Table of Contents

List of Figures ........ vi
List of Tables ........ viii
Acknowledgements ........ ix
Dedication ........ x
Chapter 1 - Introduction ........ 1
1.1 Importance of Cryogenic Temperature Testing ........ 1
1.2 Prior Work ........ 2
1.3 Thesis Outline ........ 3
Chapter 2 - Semiconductor Properties ........ 4
2.1 Energy Band Diagram ........ 4
2.2 Carrier Freeze-Out ........ 6
2.3 The Kink Effect ........ 8
2.4 Bulk Process Overview ........ 9
2.4.1 Resistors ........ 9
2.4.2 Diodes ........ 10
2.4.3 Field Effect Transistors (FETs) ........ 11
2.5 Silicon-on-Insulator (SOI) Overview ........ 12
2.5.1 SOS Silicide Blocked (SN) Resistor ........ 13
2.5.2 SOS Field Effect Transistors (FETs) ........ 14
Chapter 3 - Measurement Systems and FET Curve Tracer Program ........ 15
3.1 Cryogenic Cooling System One: Janis ST-100 ........ 15
3.2 Cryogenic Cooling System Two: CTI-Cryogenics Model 22 Refrigerator and Model SC Compressor ........ 17
3.3 Temperature Measurement Validation ........ 19
3.4 LabVIEW FET Curve Tracer ........ 20
Chapter 4 - Measured Results ........ 24
4.1 SOS SN Resistor ........ 24
4.2 Bulk Rectifier ........ 27

4.3 Bulk MOS FET ........ 30
4.4 SOS FET Measurements ........ 33
4.4.1 2µm HN FET ........ 34
4.4.2 2µm IN FET ........ 40
4.4.3 2µm RN FET ........ 42
Chapter 5 - Conclusions and Future Work ........ 46
5.1 Future Work ........ 47
References ........ 49
Appendix A - LabVIEW FET Curve Tracer F2012 Code ........ 51

# List of Figures

Figure 2.1: Energy Band Diagram (after [9]) ..... 4
Figure 2.2: (a) n-Type and (b) p-Type Energy Band Diagrams (after [9]) ..... 5
Figure 2.3: Electron Density vs Inverse Temperature (after [11]) ..... 7
Figure 2.4: Kink Effect in an NFET ..... 8
Figure 2.5: n+ Diffusion Resistor (after [10]) ..... 9
Figure 2.6: Lateral p-n Diode (after [10]) ..... 10
Figure 2.7: Diffused Junction Rectifier ..... 11
Figure 2.8: Bulk CMOS FETs (after [10]) ..... 12
Figure 2.9: (a) Typical BOX Layer Process and (b) Thin Film SOS Process Comparison ..... 13
Figure 2.10: SOS Silicide Blocked (SN) Resistor ..... 14
Figure 2.11: SOS NFET and PFET Transistors (after [1]) ..... 14
Figure 3.1: Janis ST-100 System Setup ..... 15
Figure 3.2: Photo of the Janis System Setup ..... 16
Figure 3.3: CTI-Cryogenics Model 22 Refrigerator and Model SC Compressor Diagram ..... 17
Figure 3.4: CTI-Cryogenics System Setup Photo ..... 18
Figure 3.5: Temperature Diode and Thermocouple Comparison ..... 19
Figure 3.6: Temperature Sensor Placement (a) Side View and (b) Top View ..... 20
Figure 3.7: LabVIEW Control Diagram ..... 21
Figure 3.8: New LabVIEW FET Curve Tracer Program Block Diagram ..... 23
Figure 4.1: SN Resistor Value vs Temperature ..... 24
Figure 4.2: SN Resistor I-V Characteristics at 11 Kelvin ..... 25
Figure 4.3: Resistance vs Power Dissipation at 11 Kelvin ..... 26
Figure 4.4: Expanded View of Resistance vs Power Dissipation ..... 27
Figure 4.5: 1N4001 Rectifier at 294 Kelvin ..... 28
Figure 4.6: 1N4001 Rectifier at 5 Kelvin ..... 29
Figure 4.7: 1N4001 Rectifier at 50 Kelvin ..... 30
Figure 4.8: 2N7000 NFET Id vs Vds at 294 Kelvin ..... 31
Figure 4.9: 2N7000 NFET Id vs Vgs Curves at 294 Kelvin ..... 31
Figure 4.10: 2N7000 NFET Id vs Vds Curves at 5 Kelvin ..... 32

Figure 4.11: 2N7000 NFET Id vs Vgs Curves at 5 Kelvin ........ 33
Figure 4.12: 2µm HN FET Id vs Vds Curves at 294 Kelvin ........ 34
Figure 4.13: 2µm HN FET Id vs Vgs Curves at 294 Kelvin ........ 35
Figure 4.14: 2µm HN FET Id vs Vds Curves at 50 Kelvin ........ 36
Figure 4.15: 2µm HN FET Id vs Vgs Curves at 50 Kelvin ........ 36
Figure 4.16: 2µm HN FET Id vs Vds Curves at 30 Kelvin ........ 37
Figure 4.17: 2µm HN FET Id vs Vgs Curves at 30 Kelvin ........ 38
Figure 4.18: 2µm HN FET Id vs Vds Curves at 5 Kelvin ........ 39
Figure 4.19: 2µm HN FET Id vs Vgs Curves at 5 Kelvin ........ 39
Figure 4.20: 2µm IN FET Id vs Vds Curves at 5 Kelvin ........ 41
Figure 4.21: 2µm IN FET Id vs Vgs Curves at 5 Kelvin ........ 41
Figure 4.22: 2µm RN FET Id vs Vds Curves at 294 Kelvin ........ 42
Figure 4.23: 2µm RN FET Id vs Vgs Curves at 294 Kelvin ........ 43
Figure 4.24: 2µm RN FET Id vs Vds Curves at 56 Kelvin ........ 44
Figure 4.25: 2µm RN FET Id vs Vgs Curves at 56 Kelvin ........ 44
Figure A.1: FET Curve Tracer F2012 Front Panel ........ 51

# List of Tables

Table 1.1: Typical Operational Temperatures (after [6])................................................................ 1

# Acknowledgements

I would like to acknowledge the help from Andy Fund in obtaining a lot of the test data included in this thesis. Dr. William Kuhn and Dr. Andrew Rys for their insight, countless hours of help and discussion. I would also like to thank Dr. William Hageman for his time and suggestions.

I would like to thank Dr.Vikas Berry for allowing us to use his Janis ST-100 Cryogenic System to make measurements.

My officemates, Chelsi Koval and Matt Clewell, for good conversation and helping my explanations makes sense.

I would especially like to acknowledge UES Inc., whose support made this research possible.

Last but not least, anyone who has had to endure a conversation with me about the topics in this thesis. Sometimes speaking out loud helps to refine your thoughts and ideas.

# Dedication

I dedicate this thesis to my Mom, Dad, Grandma and Grandpa; without your unconditional support I never would have come this far or accomplished this much. Thank you.

# Chapter 1 - Introduction

## 1.1 Importance of Cryogenic Temperature Testing

This research was funded to explore the feasibility of creating an amplifier to work with a Superconducting QUantum Interference Device (SQUID). The SQUID is a superconducting ring with a Josephson Junction, which must be submerged in liquid nitrogen to function properly. The SQUID can detect a single quantum change in magnetic flux [3]. The SQUID creates a signal, which must be amplified in order to detect. The amplifier needs to operate at or below 77 Kelvin because the entire device is submerged in liquid nitrogen. Prior to designing the amplifier, the operational characteristics of a commercial Silicon-on-Sapphire (SOS) process had to be obtained to ensure the proposed design could work in a cryogenic environment.

Cryogenic testing is an important part of device characterization, especially devices that will be used in harsh environments. Such environments include terrestrial application circuits such as SQUIDs and deep space planetary probes such as those sent to the moons of Saturn or Jupiter. Table 1.1 shows the typical temperatures for a few destinations in our solar system.

**Table 1.1: Typical Operational Temperatures (after [6])**

| Destination | Temperature (Kelvin) |
|---|---|
| Mars | 253 to 153 |
| Jupiter | 122 |
| Saturn | 90 |
| Uranus | 64 |
| Neptune | 51 |
| Pluto | 44 |

Table 1.1 shows the temperature extremes electronic devices must be able to handle if a device will be operating in the ambient environment. The Low Temperature Electronics Program at NASA's Glenn Research Center conducts cryogenic temperature tests on electronic devices with the hopes of creating smaller lighter systems. The cold space environment lead to the development of radioisotope heating units (RHUs), to maintain a constant temperature and ensure electronics will continue functioning properly. RHUs are complex systems that require containment structures, which add both weight and development time to launch missions.

Eliminating the need for RHUs by further development of cryogenic capable electronic systems would reduce the cost of future space missions [6].

Understanding the behaviors of semiconductor devices in cryogenic environments, like the ones in Table 1.1, is essential for designing reliable systems. When semiconductor electronics are subjected to cryogenic temperatures; a few important design characteristics change. The kink effect [8][14] may be seen and, threshold voltages, operational currents and resistances will all change. There is also a phenomenon called carrier freeze-out, which can prevent a semiconductor device from working at all. It is difficult and often impossible to repair systems while they are in harsh environments and understanding how basic semiconductor devices work in such environments is crucial.

## 1.2 Prior Work

The importance of cryogenic research has lead to a large accumulation of information on the topic. The majority of this thesis will focus on bulk process and SOS technologies.

Bulk semiconductor processes are the traditional technologies found in personal computers and rectifier diodes, like a 1N4001. When bulk transistors are brought down to cryogenic temperatures the presence of the kink effect is noted [5].

SOS devices also exhibit interesting characteristics at cryogenic temperatures. The threshold voltages and drain currents tend to increase [15], and transistors show an increasing kink effect at temperatures below 180 Kelvin [4] [14].

A description of the freeze-out phenomenon, a set of medium transistor Id vs Vds and Id vs Vgs curves and a test on an n+ diffusion resistor are given at 300 K, 4.2 K and mK temperatures in [4]. However, a comprehensive collection of transistor curves with a linear scale and the testing of a silicide blocked (SN) resistor are not given. The log scale of the transistor curves presented in [4] make it hard to see the kink effect. This thesis will expand upon the types of transistors tested, the temperatures they are tested at and provide a clearer view of the kink effect. An intrinsic transistor (IN) was examined and measurements were taken on FETs with larger channel lengths. To better display kink effect magnitude, a linear current axis was used. Finally, the SN resistor is tested since it is valuable to analog circuit design and is the most likely device to exhibit freeze-out effects.

## 1.3 Thesis Outline

This thesis will discuss the general concepts and device comparison between a bulk process and SOS process starting in Chapter 2. The traditional construction of a bulk silicon process diode and MOSFET will be shown and a basic overview of transistor and resistor construction in an SOS process is provided. An explanation of the benefits of a SOS process and other information will be presented. An explanation of the freeze-out phenomenon and the basic theory surrounding it will also be covered.

Chapter 3 will describe the cryogenic systems used to test devices and how the data was collected. A redesigned LabVIEW program will be presented which improves the data collection process previously used at K-State [13]. A more detailed view of the program is located in Appendix A.

The acquired data and explanation of results will be presented in Chapter 4. Observations of kink effect, threshold shifts, and increased currents will be shown.

Finally, Chapter 5 will state the major conclusions and point out future work that should be completed in this research area.

# Chapter 2 - Semiconductor Properties

## 2.1 Energy Band Diagram

A semiconductor is exactly what the name suggests; it is a material that has conductivities between metals and insulators [9]. A common semiconductor used in industry is silicon. Semiconductors have a valence band and conduction band with a band-gap between them. Figure 2.1 is an energy band diagram for an intrinsic semiconductor.

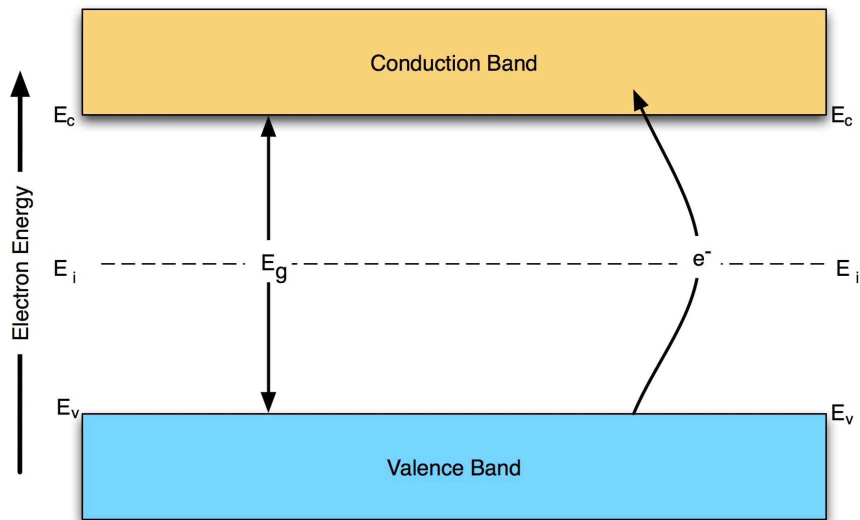


**Figure 2.1: Energy Band Diagram (after [9])**

When sufficient energy is applied to a semiconductor an electron moves into the conduction band. The conduction band edge is $E_c$ and the valence band edge is $E_v$. The energy required for an electron in the valence band to jump into the conduction band is $E_g$ or the band-gap energy. Once an electron is in the conduction band it is considered a free electron because it is no longer bound to its original nucleus and can move freely under the influence of a small electric field. The intrinsic Fermi energy, $E_i$, is located halfway between the conduction and valence bands. This results in a very small probability that any given electron will make the jump, since the average thermal energy is much less than $E_g/2$.

Semiconductors are usually doped to change the electrical characteristics. There are two main types of semiconductor materials; n-type materials have electrons as their majority carriers while p-type materials have holes as their majority carriers. The n-type material is doped with impurities called donors because they “donate” easily excitable electrons from introduced states

just below $E_c$. The p-type material is created with impurities called acceptors because they "accept" electrons from the valance band. P-type materials introduce states just above $E_v$. Figure 2.2 demonstrates a band diagram for an n-type and p-type semiconductor.

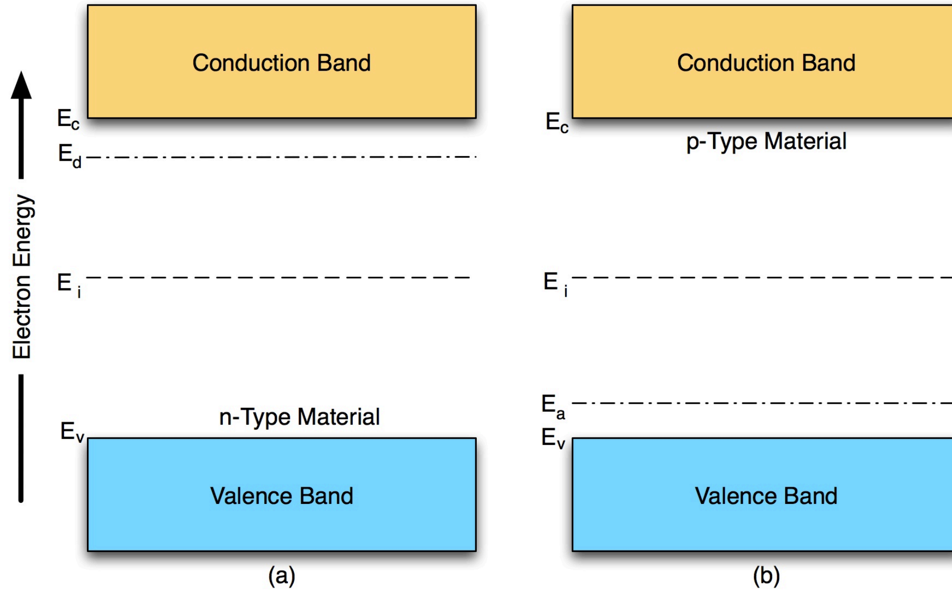


**Figure 2.2: (a) n-Type and (b) p-Type Energy Band Diagrams (after [9])**

$E_d$ is the donor energy level and $E_a$ is the acceptor energy level. Now, instead of an electron having to jump from the valence band to the conduction band they only have to jump from the donor energy band to the conduction band for n-type and jump from the valence band to the acceptor energy band in p-type. The band-gap is essentially reduced, which means more electrons can be in the conduction band at lower thermal energy levels.

The Fermi-Dirac Distribution Function models the probability of having an electron at an energy level, E. If there is not an available energy state at level E there will not be any electrons present with that energy. This is an area called a forbidden region.

Equation 2.1 is the Fermi-Dirac Distribution Function.

$$\frac{N(E)}{g(E)} = f_F(E) = \frac{1}{1+e^{\left(\frac{E-E_F}{kT}\right)}} \tag{2.1}$$

N(E) is the number of particles per unit volume per unit energy, g(E) is the number of quantum states per unit volume per unit energy and $f_F(E)$ is the ratio of filled states to total quantum states at energy level, E. The temperature, T, is in Kelvin, and k is Boltzmann's constant, which is $8.62 \times 10^{-5}$ eV/K. When $f_F(E)$ is one there is a 100% probability an electron is at the given

energy level, E, if $f_F(E)$ is zero there is a 0% probability an electron is at the given energy level. $f_F(E)$ is 0.5 when the desired energy level is equal to the Fermi level, in other words at the Fermi level the probability of finding an electron is 50%. It can be seen with the Fermi-Dirac equation that if the Temperature, T, is low the chances of finding electrons in higher energy levels decreases [9].

## 2.2 Carrier Freeze-Out

Carrier freeze-out is a phenomenon that occurs at cryogenic temperatures, where electrons do not have sufficient energy to jump to the conduction band. In the case of an n-type material, electrons are bound to the donors. The Fermi-Dirac Distribution Function, eqn 2.1, and the effective density of states for donors, $N_d$, can be used to estimate the density of electrons at the donor level. The probability function of electrons occupying the donor state is.

$$n_d = N_d - N_d^+ \tag{2.2}$$

The density of electrons occupying the donor level is $n_d$ and the density of states for donors is $N_d$. $N_d^+$ is the density of ionized donor atoms. $n_d$ can also be represented as follows:

$$n_d = \frac{N_d}{1+\frac{1}{g}e^{\left(\frac{E_d - E_F}{kT}\right)}} \tag{2.3}$$

If $(E_d - E_F) \gg kT$, then we can use the Boltzmann approximation and neglect the 1 in the denominator. We can also assume the degeneracy factor, g, is equal to 2 to account for electron spin. The following is the result:

$$n_d \approx 2N_d e^{\left[\frac{-(E_d - E_F)}{kT}\right]} \tag{2.4}$$

We can also approximate the density of electrons in the conduction band by the following:

$$n_0 \approx N_c e^{\left[\frac{-(E_c - E_F)}{kT}\right]} \tag{2.5}$$

Now, if we compare the number of electrons in the donor state, $n_d$, with the total number of electrons, $(n_d + n_0)$. The following relationship is found:

$$\frac{n_d}{n_d + n_0} = \frac{2N_d e^{\left[\frac{-(E_d - E_F)}{kT}\right]}}{2N_d e^{\left[\frac{-(E_d - E_F)}{kT}\right]} + N_c e^{\left[\frac{-(E_c - E_F)}{kT}\right]}} \tag{2.6}$$

If we simplify eqn 2.5 the Fermi energy, $E_F$, drops out to give:

$$\frac{n_d}{n_d+n_0} = \frac{1}{1+\frac{N_c}{2N_d}e^{\left[\frac{-(E_c-E_d)}{kT}\right]}} \tag{2.7}$$

Looking at eqn 2.7, it can be seen when the temperature, T, is equal to zero the exponential will become $e^{(-\infty)} = 0$. Eqn 2.7 must then be equal to 1; this means all the electrons are bound to their donors. The situation where all of the electrons are bound to their donors is called carrier freeze-out. When T is equal to room temperature, or 300 Kelvin, a situation called complete ionization occurs, where all of the donor atoms have given up their electrons. When T is between zero and 300K, partial ionization occurs. When T is at much higher levels the intrinsic carriers begin to exceed the donor densities [9]. Figure 2.3 shows the effective carrier density verses inverse temperature.

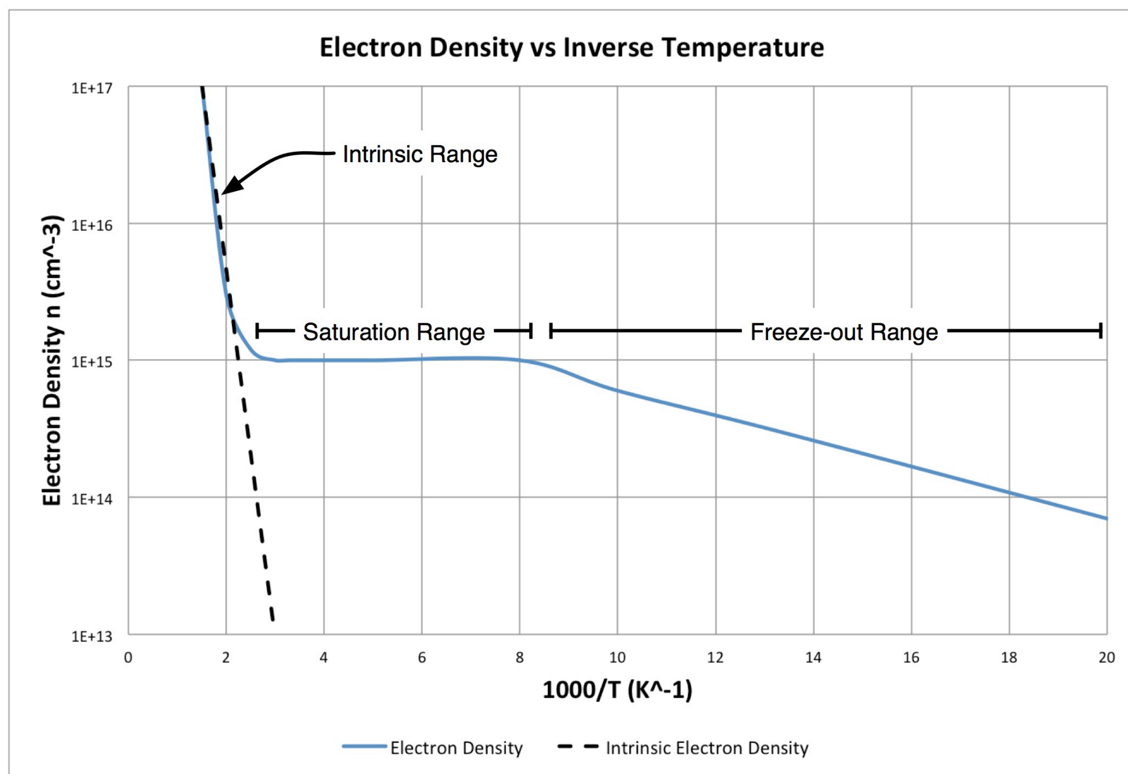


**Figure 2.3: Electron Density vs Inverse Temperature (after [11])**

Figure 2.3 shows how the effective electron density changes with decreasing temperature. The saturation range is where all the donor atoms are ionized and this is the preferred operational range for the semiconductor. The freeze-out range is where the donors are only partially ionized

and as the temperature decreases the probability of finding electrons in the conduction band decreases. The intrinsic range is where the temperature is high enough where the intrinsic carriers become ionized and overwhelm the donor ions. Please note the information presented in this chapter mainly pertains to lightly doped semiconductors. Heavily doped semiconductors require more in depth analysis not covered in this thesis. The information presented here is to give an understanding of basic semiconductor properties to help in the discussion later.

## 2.3 The Kink Effect

The kink effect phenomenon can occur in transistors when the body contact is floating or if the device is brought down to cryogenic temperatures. In NFETs, it is caused by holes moving from drain to source under the channel, lowering the threshold voltage thereby causing an increase in the Id current [8]. Figure 2.4 shows an example of the kink effect in an NFET.

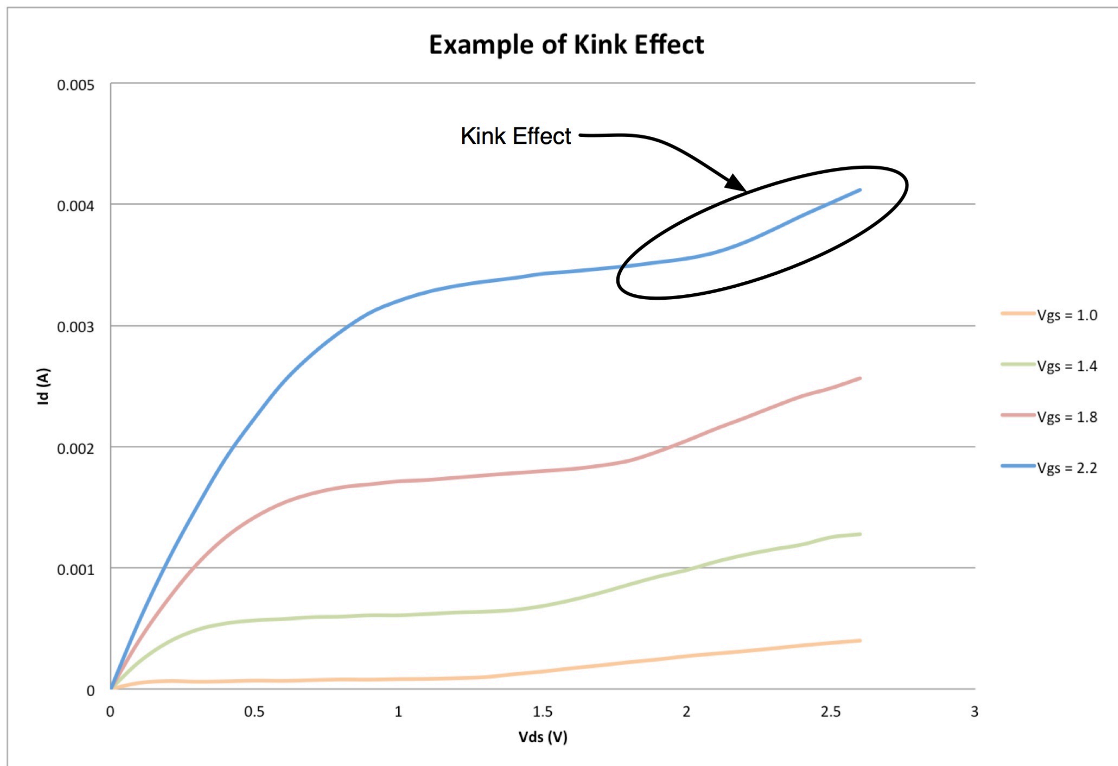


**Figure 2.4: Kink Effect in an NFET**

As can be seen in Figure 2.4, the kink effect starts in the saturation region of the transistor curve. The currents increase signifying a decrease in the output resistance because of:

$$r_{out} = g_{ds}^{-1} = \frac{\partial V_{ds}}{\partial I_d} \tag{2.8}$$

Equation 2.8 shows that as the change in current increases the output resistance decreases. In analog designs, the decreased output resistance causes the gain of the device to decrease.

## 2.4 Bulk Process Overview

A bulk process is the conventional method used in integrated circuit (IC) manufacturing. It starts with a "bulk" silicon substrate, which is usually p-type. Wells are often used in bulk processes to create an area of a different type compared to the substrate. NFETs are built directly in the substrate of a p-type wafer but PFETs must have an n-well to be functional in a bulk process [2]. The benefits of this process are the ease of mass production and maturity of the technology. This section will cover some of the basic structures for bulk process resistors, diodes and FETs.

### *2.4.1 Resistors*

A typical resistor type found in bulk CMOS is an n-diffusion resistor. If the resistor is built using a heavily doped n+ diffusion, it is useful for making low resistance devices in a circuit. Conversely, an n- doping such as that used in wells can be used to create larger resistance values. Figure 2.5 shows the layout of a typical n+ diffusion resistor.

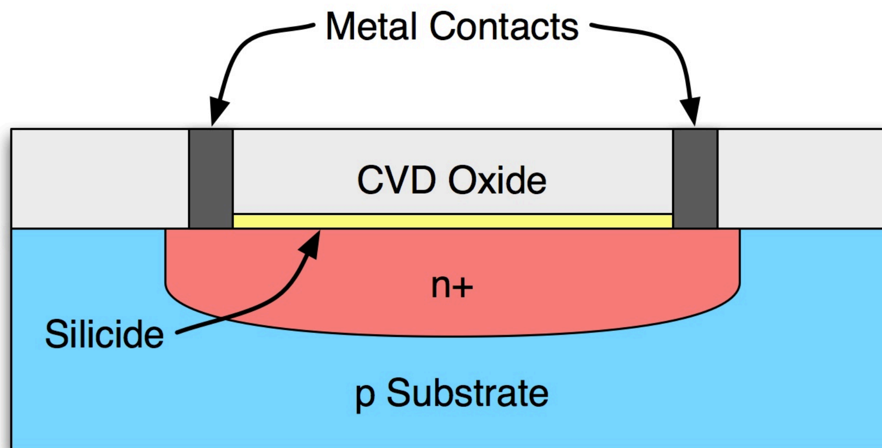


**Figure 2.5: n+ Diffusion Resistor (after [10])**

This resistor is composed of a heavily doped n+ region in a p-type substrate, with a silicide layer and metal contacts added. The silicide layer is a low resistive and thermally stable material made from silicon and another metal. Typical Silicides would be $TiSi_2$ and $CoSi_2$ [12].

When silicide is used to coat the top of an n+ diffusion region it acts to lower the resistance compared to the n+ region alone.

### *2.4.2 Diodes*

Diodes are made by the creation of a p-n junction. The typical lateral bulk CMOS process diode is created in an n-well. Figure 2.6 shows an example of a lateral diode.

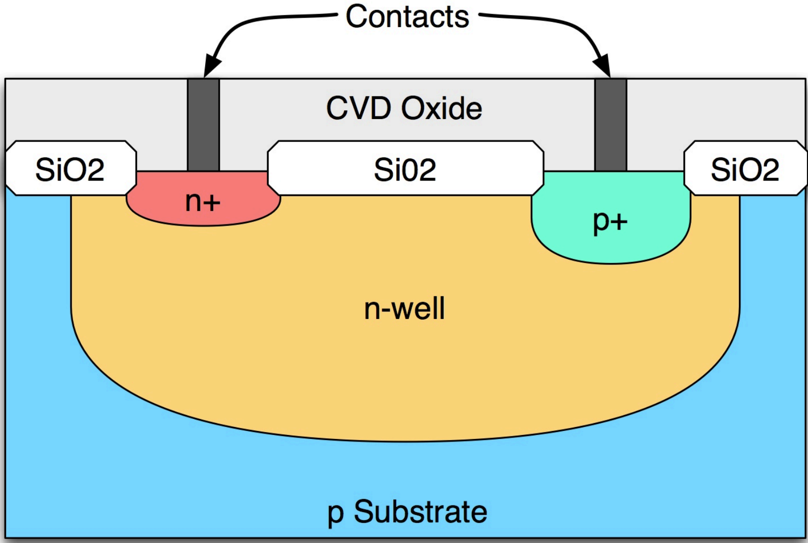


**Figure 2.6: Lateral p-n Diode (after [10])**

The diode is formed between the two metal contacts. The p+ region is the anode while the n- region is the cathode of the diode. A discrete rectifier is created a little differently. Rectifiers like the 1N4001 are diffused junction vertical diodes and need to handle larger voltages, so there is a high resistive π region. The π region is a lightly doped p- region. Figure 2.7 shows an example of a vertically created diffused junction rectifier.

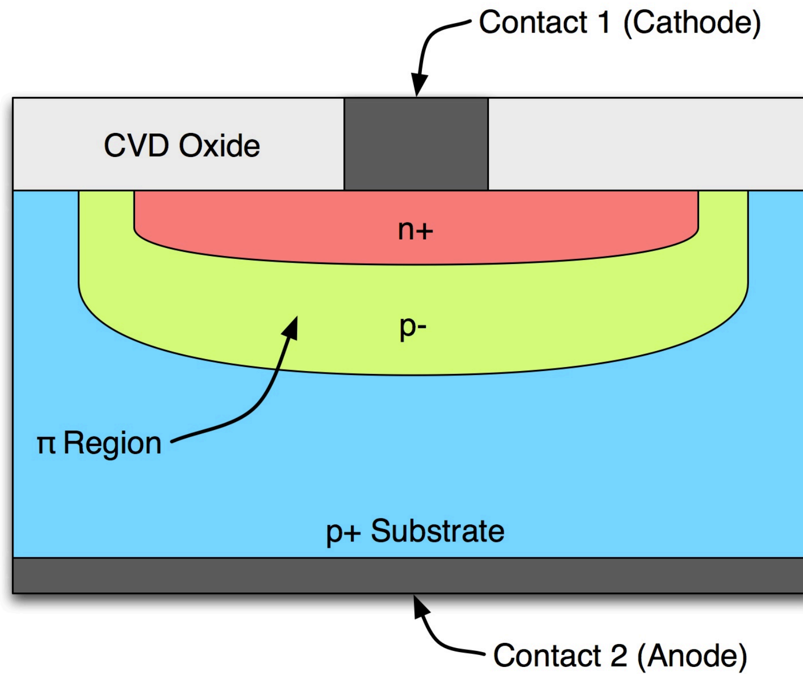


**Figure 2.7: Diffused Junction Rectifier**

The typical casing for a mass produced 1N4001 would be constructed vertically and the p+ substrate becomes the anode while the metal contact on the n+ region becomes the cathode. The p- region in the middle is the resistive π region.

### *2.4.3 Field Effect Transistors (FETs)*

FETs are one of the basic building blocks in most analog and digital designs. FETs essentially behave as electronic valves and allow the manipulation of signals and data. Figure 2.8 shows a typical bulk CMOS FETs construction.

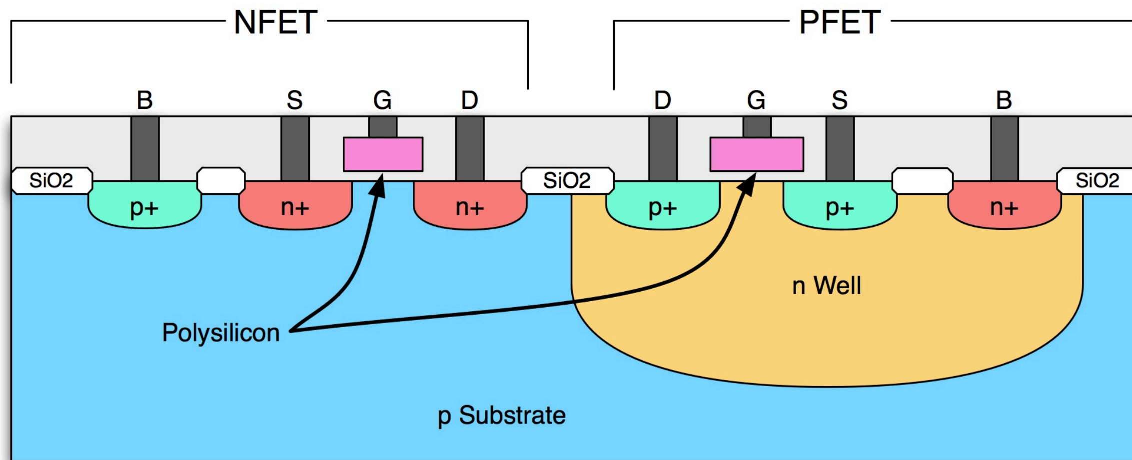


**Figure 2.8: Bulk CMOS FETs (after [10])**

Bulk CMOS FETs have body connections, which help mitigate latch up problems. The NFET is created directly in the substrate material while the PFET is created in an n well. There are parasitic capacitances, which impede the frequency of operation, because of the p substrate and the n+ diffusion regions. A similar observance is also seen in the n well with the p+ regions.

## 2.5 Silicon-on-Insulator (SOI) Overview

SOI is an area of semiconductor development with increased performance compared to bulk processes. SOI tends to have lower parasitic capacitances, which allows a higher frequency of operation in analog designs and reduced leakage and lower power dissipation in digital circuits. There are two main types of SOI processes; one uses a thin buried oxide (BOX) layer and the other is Silicon-on-Sapphire (SOS). Figure 2.9 shows a comparison between the two SOI Types.

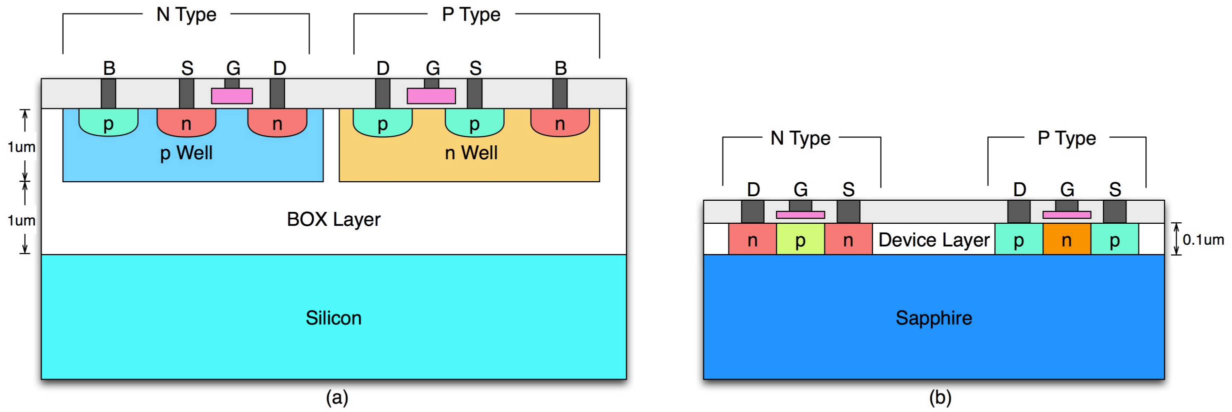


**Figure 2.9: (a) Typical BOX Layer Process and (b) Thin Film SOS Process Comparison**

The device layer can either be a thick film or thin film of silicon when the BOX insulation method is used. When the device layer is a thin film it is referred to as a fully depleted (FD) SOI because the charge carriers are depleted in the channel by the time a transistor turns on [7]. The reference to partially depleted (PD) SOI means the channel is only partially depleted of charge carriers by the time the transistor turns on.

The silicon layer for SOS is around 0.1um thick and the doped regions penetrate down to the insulating layer hence SOS is a fully depleted process. The thin film nature eliminates the need for creating wells. Instead n and p-type devices can be dielectrically isolated as shown in Figure 2.9 (b). Each transistor becomes a simple 3 terminal device without a body contact. However, the lack of a body contact makes the prevalence of the kink effect stronger in thin film SOI. Doping regions in thick film SOI do not penetrate down to the insulating layer so wells and body contacts are possible. The ability to have a body contact helps control the kink effect. This thesis will focus mainly on the thin film, fully depleted SOS process.

### *2.5.1 SOS Silicide Blocked (SN) Resistor*

The SOS SN resistor is similar in construction to the n+ diffusion resistor from the bulk silicon process except it does not have a silicide layer and the doping level is lower. The benefit of using an SN resistor is in situations where a higher resistance is needed. Figure 2.10 shows the construction of a typical SN resistor in SOS.

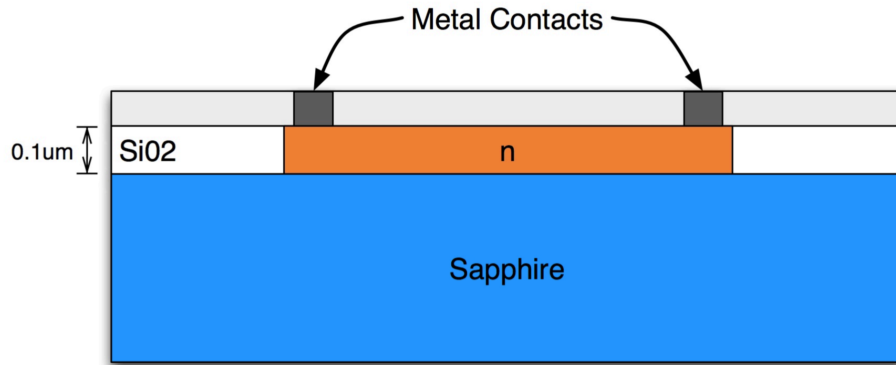


**Figure 2.10: SOS Silicide Blocked (SN) Resistor**

The n diffusion layer rests directly on the Sapphire substrate and the silicide layer has been blocked to increase the resistance.

### *2.5.2 SOS Field Effect Transistors (FETs)*

The SOS process offers a few different types of transistors. The three main categories are intrinsic, medium threshold and high threshold. The intrinsic NFET, IN, is ideally on at zero gate-source voltage. The medium threshold NFET, RN, behaves as most FETs are expected to requiring a gate-source bias of a few tenths of a volt. Finally, the high threshold NFET, HN, has a larger threshold than the normal RN FET. The same varieties of FETs are also available as PFETs. The intrinsic, medium and high threshold varieties are IP, RP and HP respectively. Figure 2.11 shows the typical construction of NFETs and PFETs in SOS.

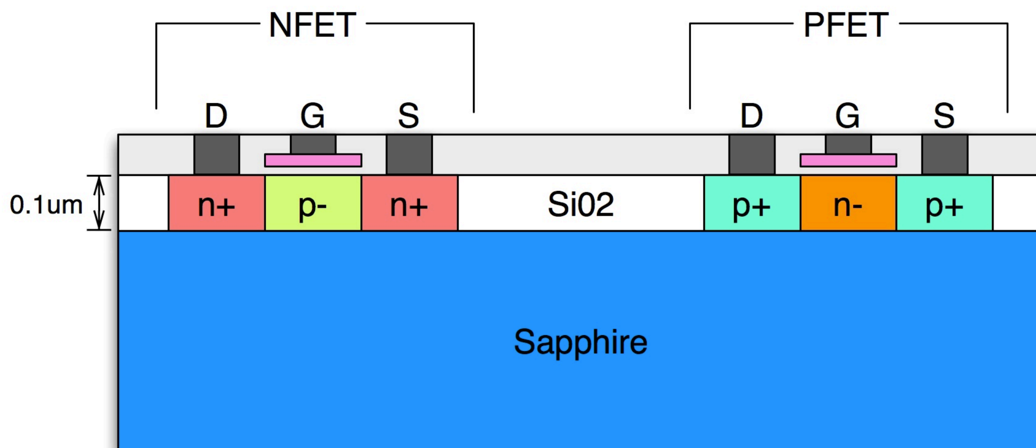


**Figure 2.11: SOS NFET and PFET Transistors (after [1])**

# Chapter 3 - Measurement Systems and FET Curve Tracer Program

Cryogenic measurements were conducted on two systems. The first system used was a Janis ST-100 with liquid helium and the second system was a closed cycle helium refrigeration system, a Helix CTI-Cryogenics Model-22 Refrigerator with a Helix CTI-Cryogenics Model SC Compressor. The Janis system setup used a LabVIEW based curve tracer program developed by a previous graduate student [13]. A new LabVIEW program was written for the CTI-Cryogenics system to address program instability, measurement quality and device protection issues such as not turning power supplies off at the end of a measurement run. Section 3.4 below overviews the new program developed. Detailed information on the newly developed LabVIEW program is located in Appendix A.

## 3.1 Cryogenic Cooling System One: Janis ST-100

The Janis ST-100 is a continuous flow cryostat system able to handle liquid helium temperatures. The system must have a continuous flow of liquid helium to maintain the desired temperature. The figure 3.1 shows the block diagram for the Janis ST-100 System.

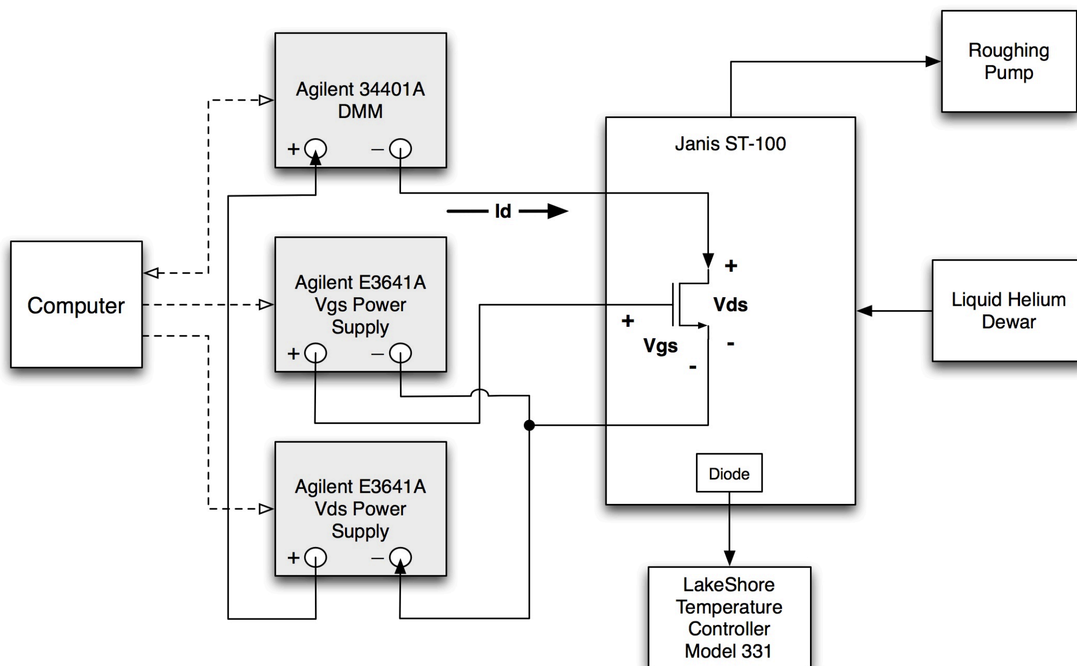


**Figure 3.1: Janis ST-100 System Setup**

The temperature controller shown in Figure 3.1 is a LakeShore 331. There is a temperature diode inside the vacuum chamber attached to the sample mount. A roughing pump must be used to create a vacuum inside the test chamber; this helps thermally isolate the device under test (DUT). Once the vacuum is at a sufficient level the transfer line could be inserted into the 60L Dewar of liquid helium to begin the cool down process. Once the system was cooled down to about 5 Kelvin, the system was allowed to saturate for about 10 minutes to make sure the temperature inside the chamber reached equilibrium.

For electrical device testing, a computer was used to control two Agilent E3641A power supplies and measure the current readings on an Agilent 34401A Digital Multi-Meter (DMM). Figure 3.2 shows a photo of the test setup.

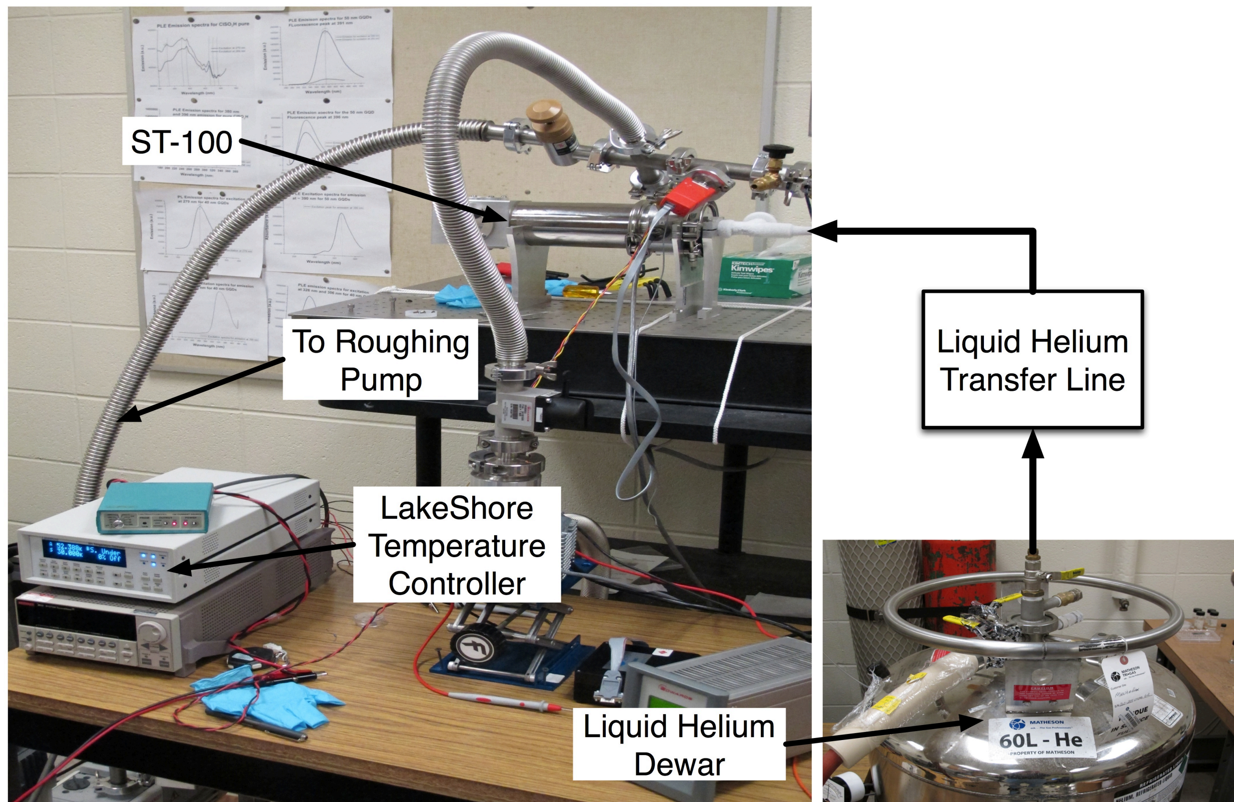


**Figure 3.2: Photo of the Janis System Setup**

SOS HN and IN transistors with 2μm channel lengths were measured as well as an SOS SN resistor. A 1N4001 diode and 2N7000 NFET were measured to see if freeze-out could be observed. These measurements are documented in chapter 4.

## 3.2 Cryogenic Cooling System Two: CTI-Cryogenics Model 22 Refrigerator and Model SC Compressor

The second system used to reach cryogenic temperatures was a closed cycle Helix CTI-Cryogenics Model 22 Refrigerator with a Helix CTI-Cryogenics Model SC Compressor. Pure helium is compressed and allowed to expand in the cold head, which extracts heat from the interior of a cryo-chamber. Figure 3.3 shows the diagram of the CTI- Cryogenics system.

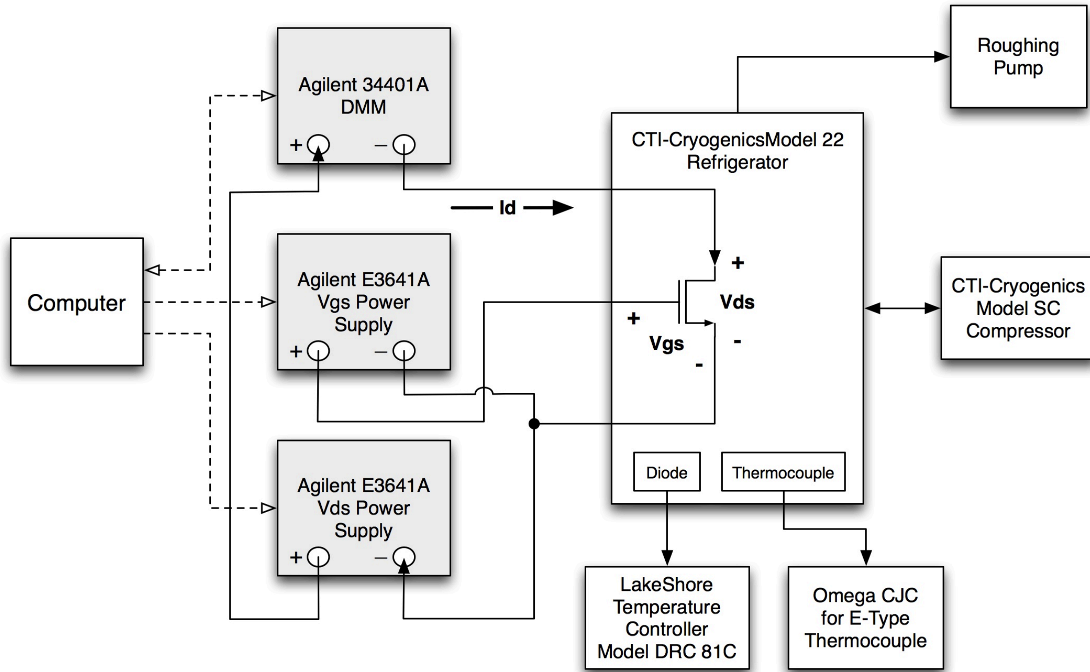


**Figure 3.3: CTI-Cryogenics Model 22 Refrigerator and Model SC Compressor Diagram**

A roughing pump is attached to the vacuum chamber. When the vacuum reaches about 15mTorr the compressor and refrigerator could be turned on. The temperature was monitored using a LakeShore Model DRC 81C Temperature Controller with a temperature diode and an E-type thermocouple with an Omega Cold Junction Compensator (CJC). The CJC returns a voltage, which can be translated into a temperature using an E-type thermocouple temperature table. The refrigerator was originally specified to reach 10 Kelvin. The system was built in 1985 and was unable to function at full potential. The system would reach 60 Kelvin after long wait times. A few measurements were taken at this temperature using two Agilent E3641A power supplies and an Agilent 34401A DMM controlled by a computer. The SOS SN resistor

was initially tested on this system using the original LabVIEW program. Figure 3.4 shows a few photos of the CTI-Cryogenics system.

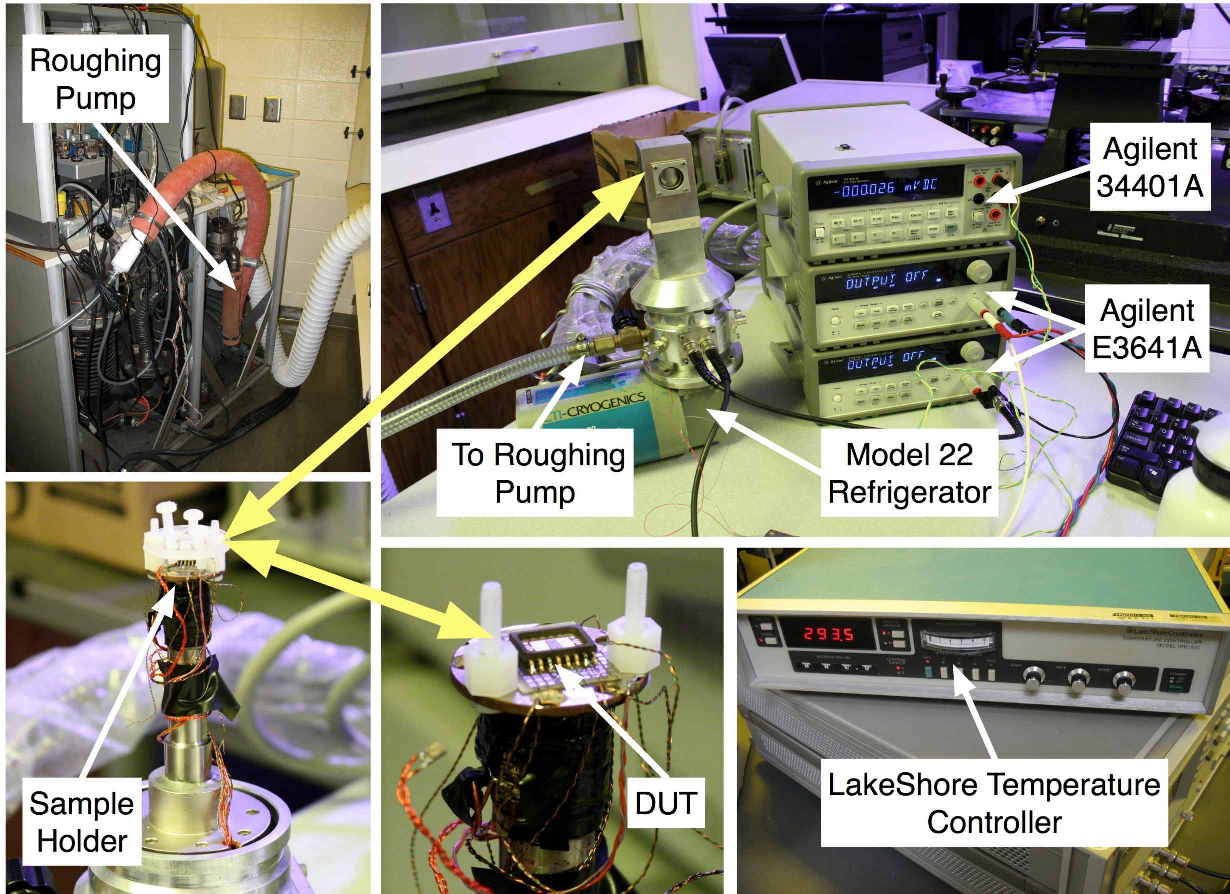


**Figure 3.4: CTI-Cryogenics System Setup Photo**

Initially, the system in Figure 3.4 was not working properly and needed to be rebuilt. Once the system was rebuilt, it was able to get down to 56 Kelvin without long wait times. Along with the system rebuild, the LabVIEW program was rewritten to increase the reliability and speed of data collection. The new system setup worked very well for a little while but began to leak helium. The leak prevented the system from reaching 56 kelvin because the required helium pressure for the compressor could not be sustained. The leak prevented more measurements from being taken, although a few measurements on a 2μm RN FET were obtained before the leak occurred. The 2μm RN FET measurements will be covered in the Chapter 4.

### 3.3 Temperature Measurement Validation

The CTI-Cryogenics systems had a temperature diode and an E-type thermocouple. Taking a measurement at room temperature and while submerged in liquid nitrogen validated the temperature sensors' accuracies. The sensors were about 4 Kelvin off at room temperature but read the same temperature at 77 Kelvin. Figure 3.5 shows how the sensors tracked each other while taking the CTI-Cryogenics system down to 50 Kelvin.

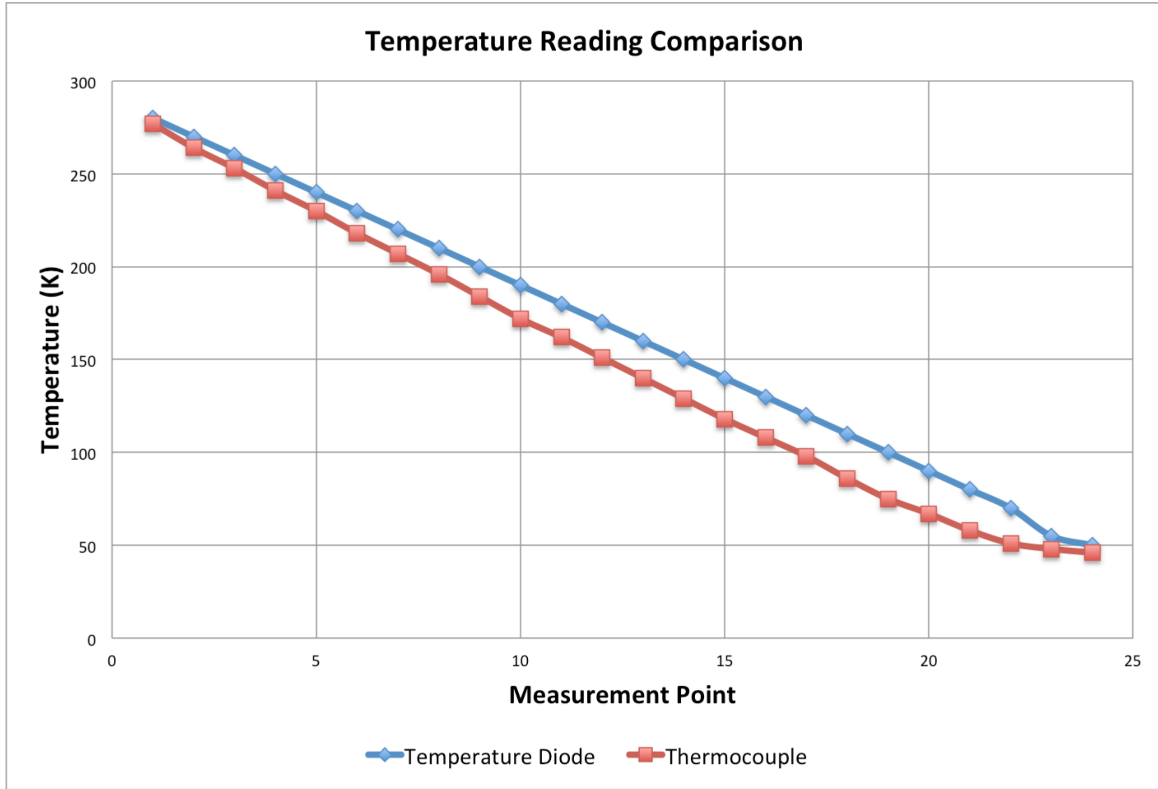


**Figure 3.5: Temperature Diode and Thermocouple Comparison**

The sensors were placed on either side of the device under test (DUT) where nylon screws were used to hold the diode and thermocouple in contact with the printed circuit (PC) board as can be seen in Figure 3.6.

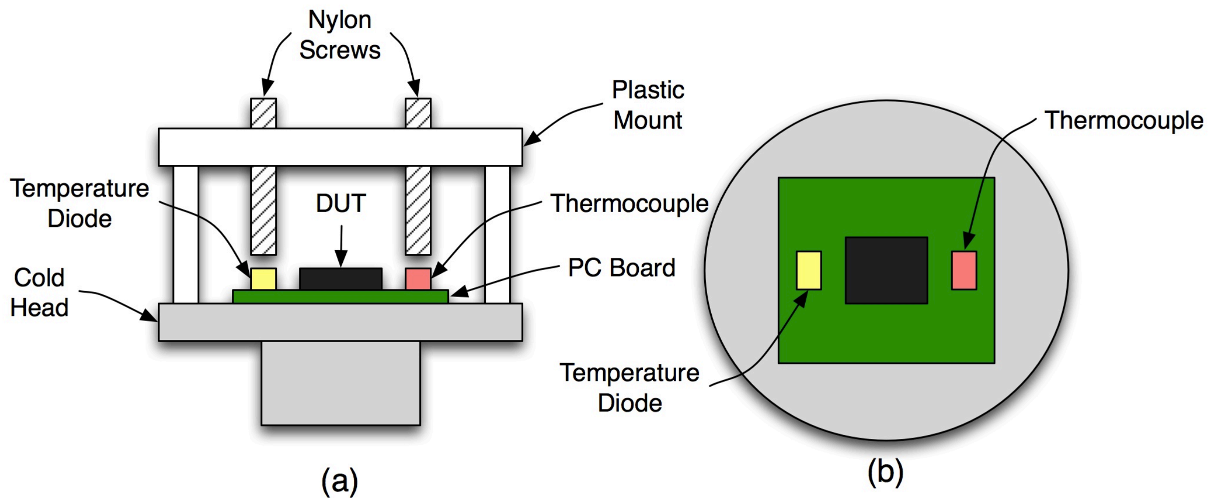


**Figure 3.6: Temperature Sensor Placement (a) Side View and (b) Top View**

Figure 3.6 (a) shows the side view of the CTI-Cryogenics System cold head and Figure 3.6 (b) shows the top view of the cold head. There was no thermal paste or other thermally conductive material used. The sensors seemed to have a slight deviation but when the system was allowed to reach a steady state the sensors started to match. This could mean the temperature diode lags slightly when measuring dynamic changes.

The Janis system only had one temperature diode so a direct comparison between two sensors was not possible. Comparing the resistor measurements on both systems allowed for verification of the temperatures measured down to 50 Kelvin. The only verification the temperature did actually get down to 5 Kelvin was the larger resistance measured. Also, Liquid helium is 4.2 Kelvin and the temperature diode measured 5 Kelvin, which is only a 0.8 Kelvin difference.

## 3.4 LabVIEW FET Curve Tracer

The LabVIEW programs were used to automate the data collection process. The original and new LabVIEW programs control the two Agilent E3641A power supplies and Agilent 34401A DMM to setup the source and drain voltages and measure drain current respectively. Figure 3.7 shows a block diagram of the LabVIEW control.

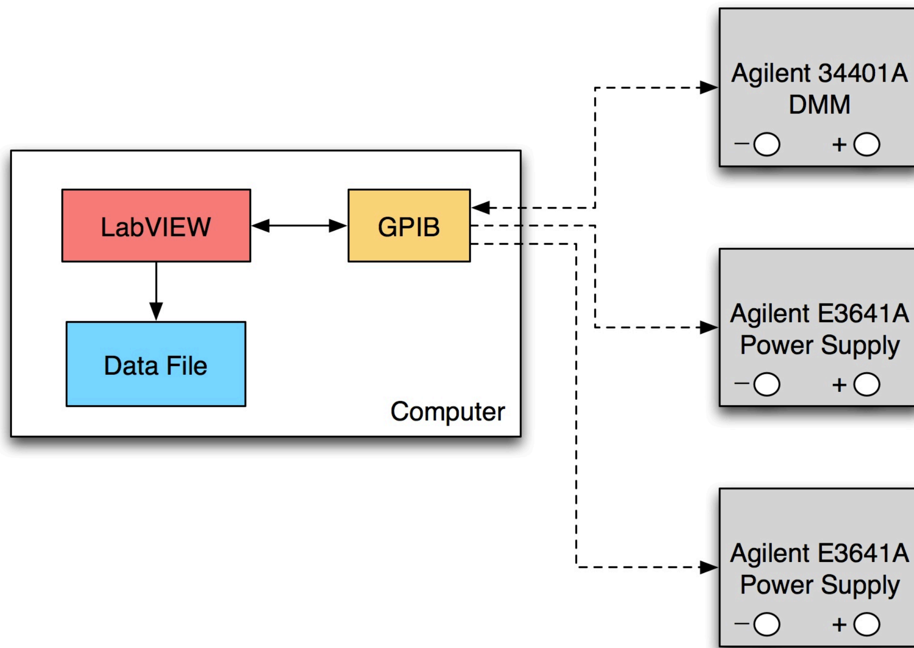


**Figure 3.7: LabVIEW Control Diagram**

The LabVIEW programs communicate through a GPIB Buss. The power supply voltages are swept and a DMM records the current measurement at each voltage step. The DMM sends the data collected back to LabVIEW, where the data is written to a file for storage. The basic format of this control diagram is the same for both LabVIEW programs the differences are how the programs handle the data.

The original LabVIEW program had a few problems. It would occasionally crash and it was a little slow. In addition, the original program was designed to work with a temperature controller, which was no longer being used and probably contributed to the crashes. The major changes in the rewritten LabVIEW program were:

1. The Front Panel display was simplified.
2. The real-time graph was changed to Id vs Vds instead of Id vs Vgs.
3. State machines were used to improve device protection and measurement speed.
4. File structure was changed to a .csv file to simplify import into Microsoft Excel
5. Added ability to put notes about experiment directly in save file.
6. Power supplies are turned off at the end of measurements, if measurements are stopped or on any error detected.
7. A control to disable the DMM auto-scale with ability to select range was added.

The front panel display in LabVIEW was simplified and the visible graph was changed from Id vs Vgs to Id vs Vds. Changing the plot to Id vs Vds changed which voltage sweep was in the inner loop of the program. The Vds sweep was moved to the inner loop while the Vgs sweep was moved to the outer loop. The ability to select what GPIB channel the associated instrument is located on was also added. The original program did not allow the user to select the GPIB channel for an instrument and instead was hard coded. The new program uses a method of programing called a state machine. The state machines make any additions to the program easier to implement. State machines also allow the program to stop anytime there is an error or if the user hits the STOP button. The old program used strict time blocks to set up timing, which can cause problems if there is an error. The time block must finish its execution before the program can terminate. If the error occurs while in a block, the program may never terminate and could cause damage to the DUT. Figure 3.8 shows the block diagram for the new program.

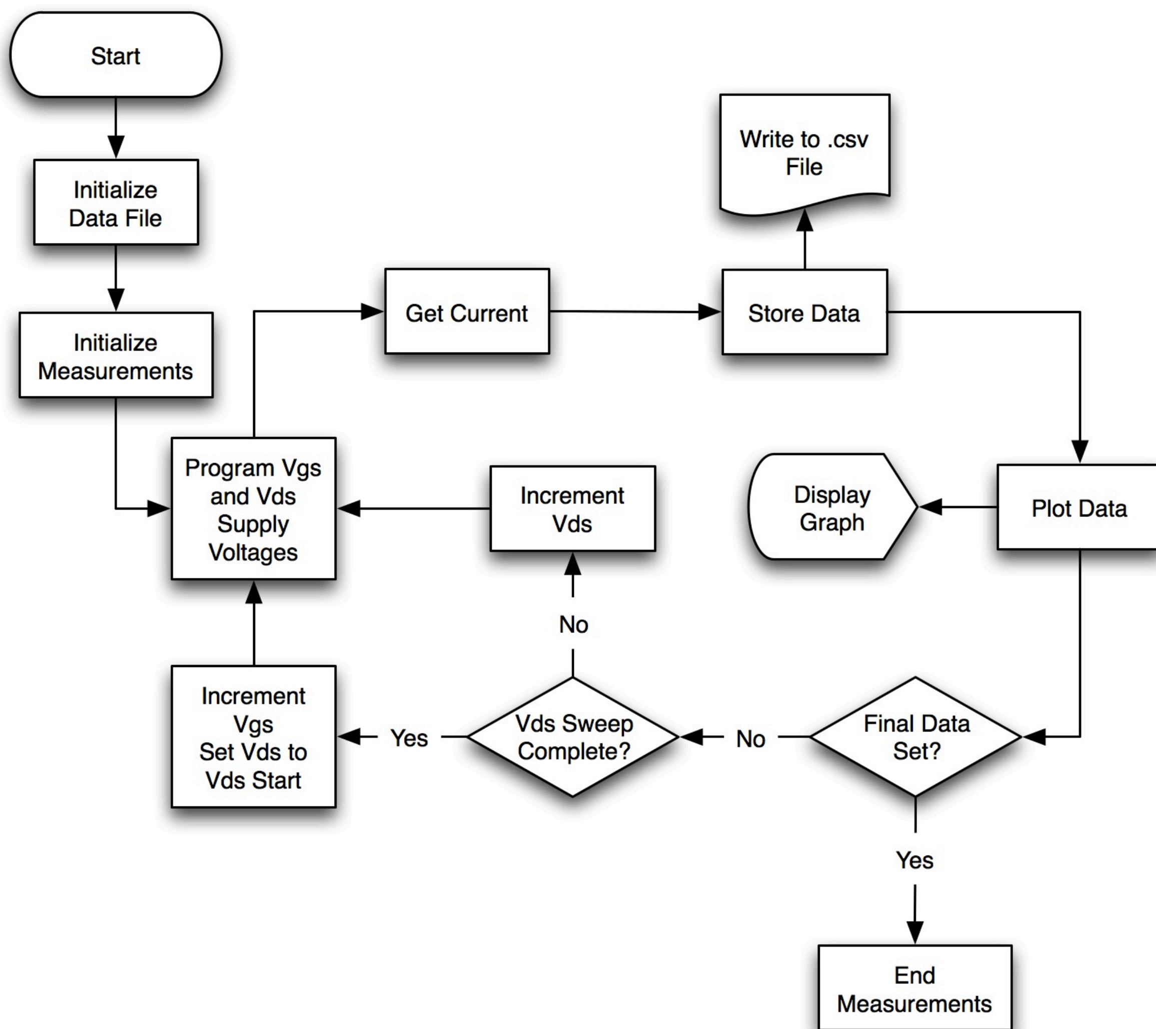


**Figure 3.8: New LabVIEW FET Curve Tracer Program Block Diagram**

The new program now has checks so if there is an error all power supplies are turned off. The original program would leave the last applied voltages instead of resetting the supplies to zero once measurements were concluded. This meant DUTs could be damaged from applying voltage levels too high for sustained operation. A more detailed overview of the LabVIEW program can be found in Appendix A.

# Chapter 4 - Measured Results

This chapter presents the data obtained from the measurement systems previously presented. The measurements are grouped by device type so a comparison between the different types can be seen. The system used to get the data is also noted.

## 4.1 SOS SN Resistor

The SOS SN resistor was measured at various temperatures with the expectation of viewing freeze-out. The SN resistor was believed to be a good candidate for observing freeze-out due to its high resistivity and lack of silicide. The SN resistor was approximately 11 kΩ at room temperature. Figure 4.1 shows how the resistance changes with temperature.

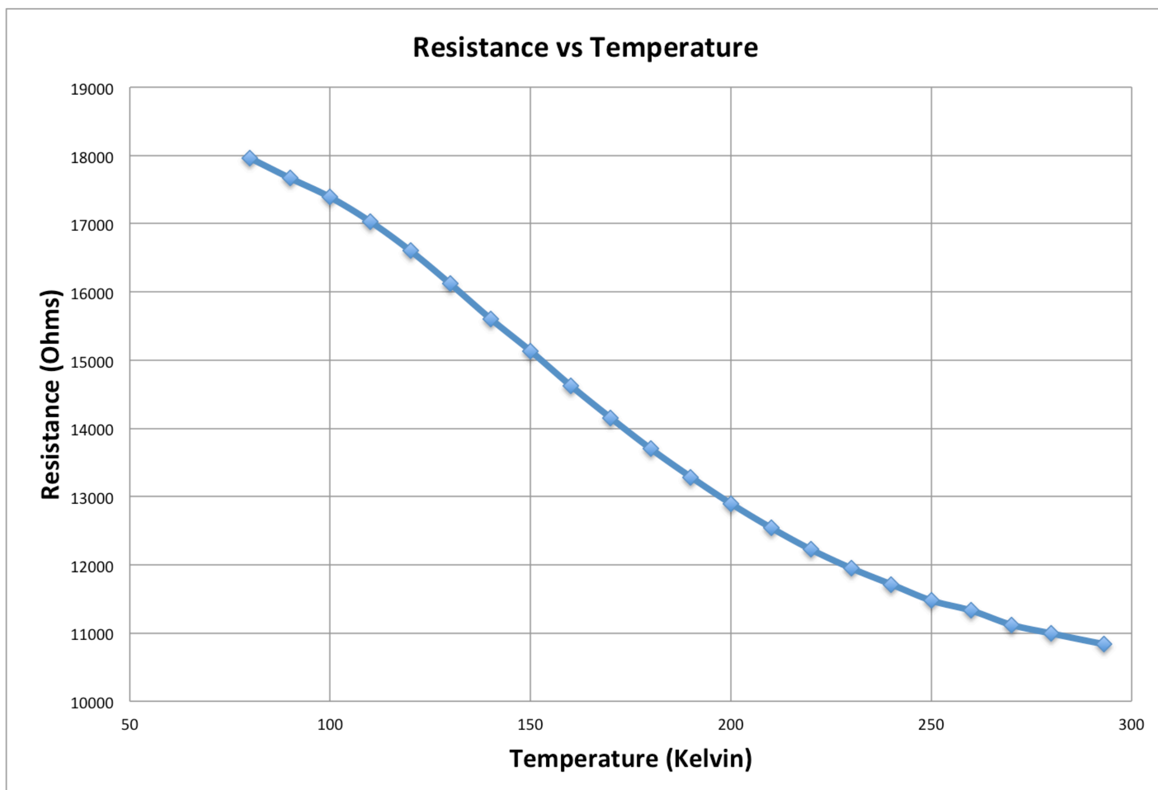


**Figure 4.1: SN Resistor Value vs Temperature**

Figure 4.1 results were obtained on the CTI-Cryogenics system and showed no freeze-out to 70 Kelvin. The SN resistor measured in Figure 75 of reference [13] increased about 34% at -110$^{o}$C (163 Kelvin) compared to about 32% at 160 Kelvin measured on the CTI-Cryogenics system shown in Figure 4.1. More tests were done on the Janis system to see how the resistor behaves at 11 Kelvin. Figure 4.2 shows the current-voltage characteristics.

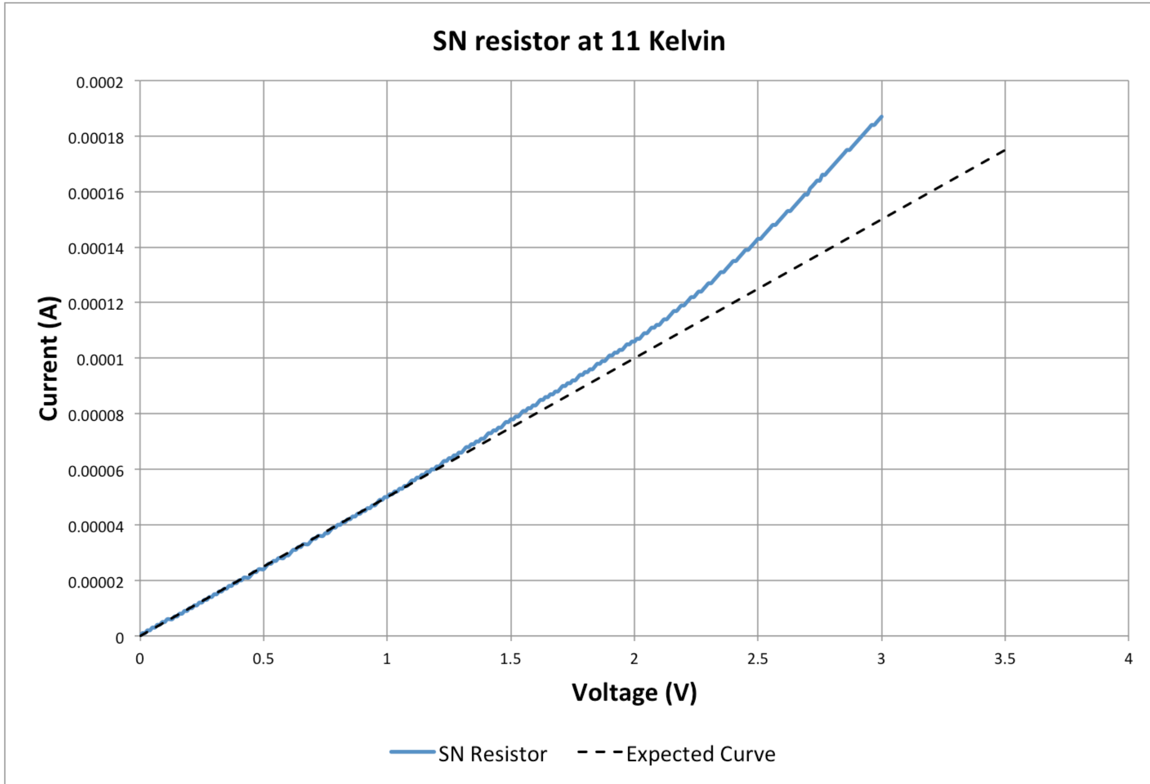


**Figure 4.2: SN Resistor I-V Characteristics at 11 Kelvin**

As shown, the device does not experience freeze-out, even at a temperature of 11 Kelvin and with very small voltages applied. However, the current-voltage curve does not follow the typical linear relationship expected. The dashed line is the expected relationship for a resistor. The curving upwards on the graph suggests the resistance is decreasing at higher voltages. The presumed reason for this non-linearity is localized heating. If the resistor is heating up, the resistance should decrease as can be seen in Figure 4.1. Figure 4.3 shows how the resistance changes with increased power dissipation.

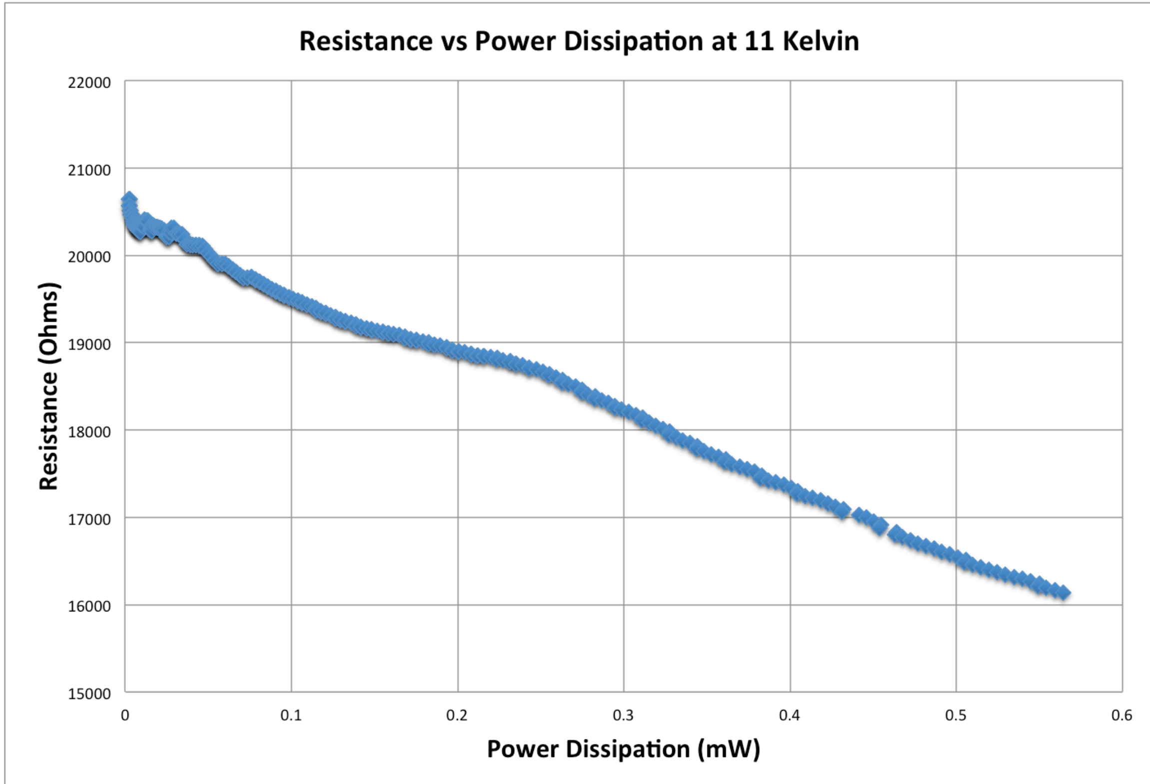


**Figure 4.3: Resistance vs Power Dissipation at 11 Kelvin**

Figure 4.3 shows that the resistance decreases with increased power dissipation. If the resistor was not heating up it should have stayed close to the maximum resistance value of about 20.5 kΩ. Figure 4.4 shows an expanded view of Figure 4.3 from 0mW to 0.1mW.

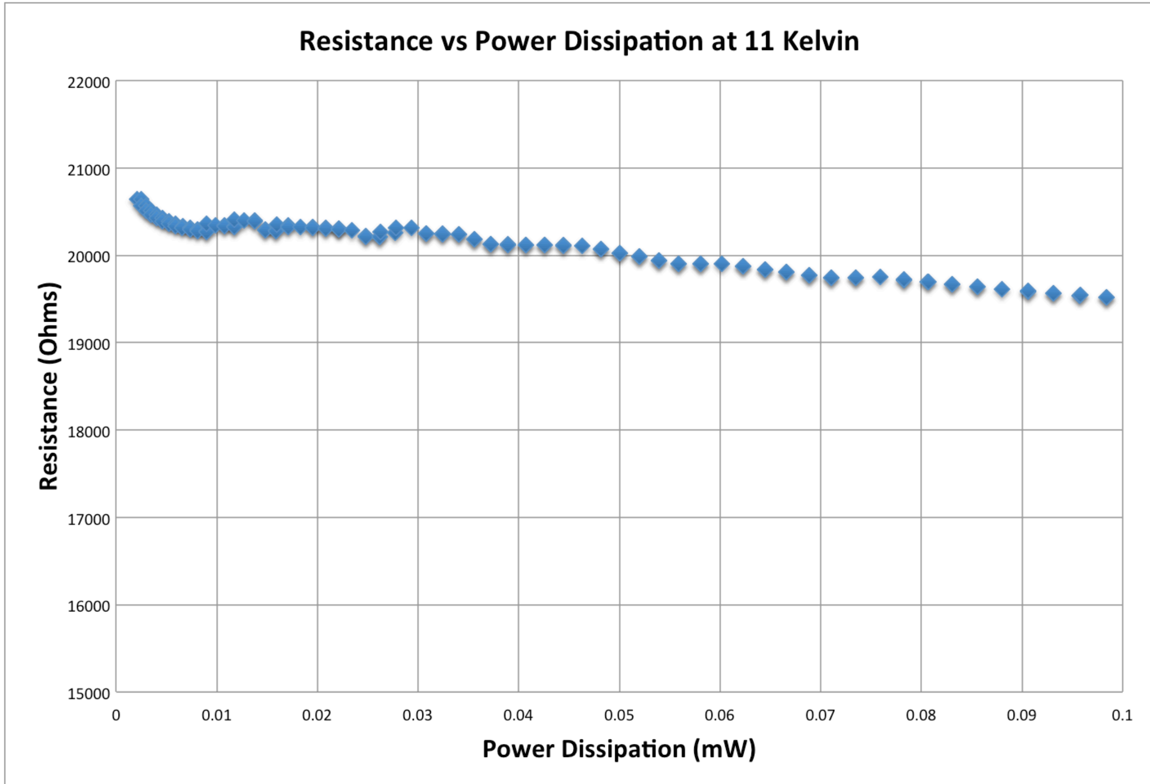


**Figure 4.4: Expanded View of Resistance vs Power Dissipation**

Figure 4.4 shows the resistance is decreasing slowly but is still close to the expected value. Since the resistance is decreasing at higher power dissipation, it is possible localized heating is occurring. If the resistor is becoming warm locally, the temperature diode may not detect the temperature change near the resistor.

## 4.2 Bulk Rectifier

A bulk process rectifier was measured to see if carrier freeze-out could be seen at 5 Kelvin. The rectifier was measured using the Janis system. The rectifier was a 1N4001 and was first tested at room temperature. Figure 4.5 shows the room temperature characteristics.

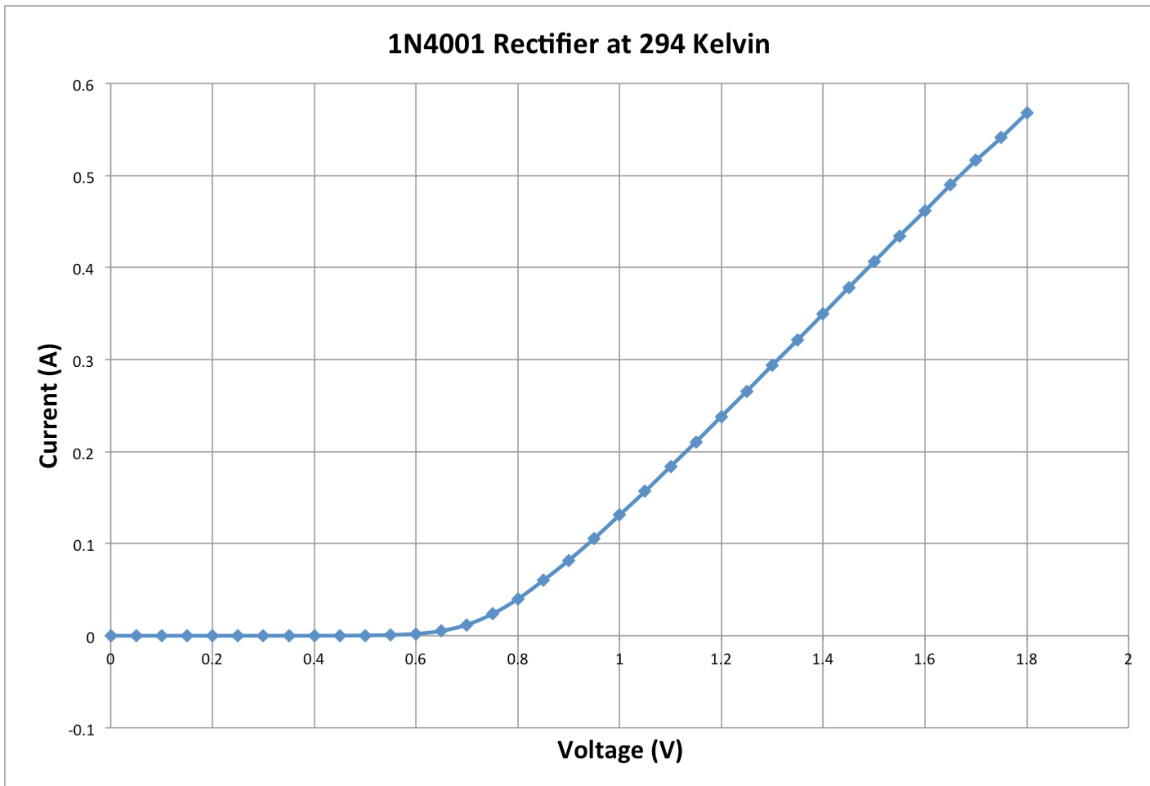


**Figure 4.5: 1N4001 Rectifier at 294 Kelvin**

As Expected, no current flows until about 0.6V where the rectifier turns on. When the rectifier turns on, it starts to follow a typical diode relationship following an exponential curve at low current and a resistive curve at higher currents. The temperature was then dropped to 5 Kelvin. Figure 4.6 shows the 5 Kelvin result.

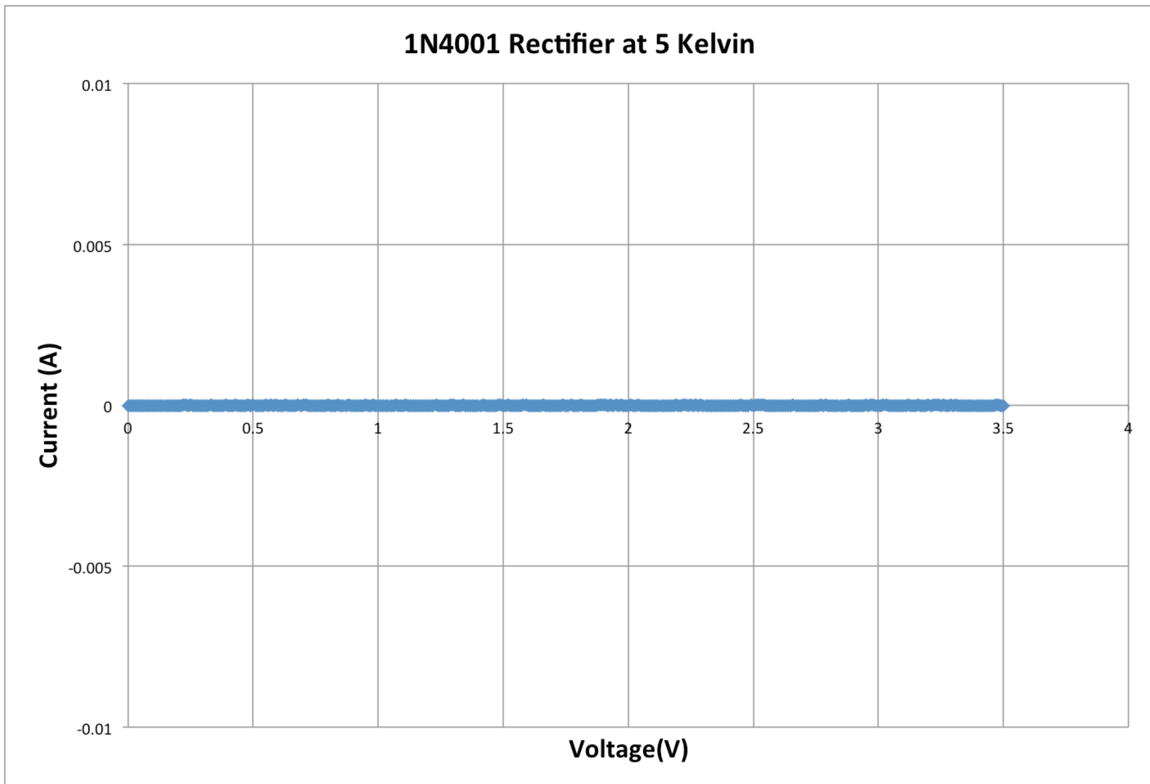


**Figure 4.6: 1N4001 Rectifier at 5 Kelvin**

Figure 4.6 shows carrier freeze-out of the 1N4001 rectifier. The voltage level went out to 3.5 volts and still there was no forward biased current. We now know the system being used can induce carrier freeze-out. The rectifier was then warmed up to 50 Kelvin. Figure 4.7 shows the 50 Kelvin result.

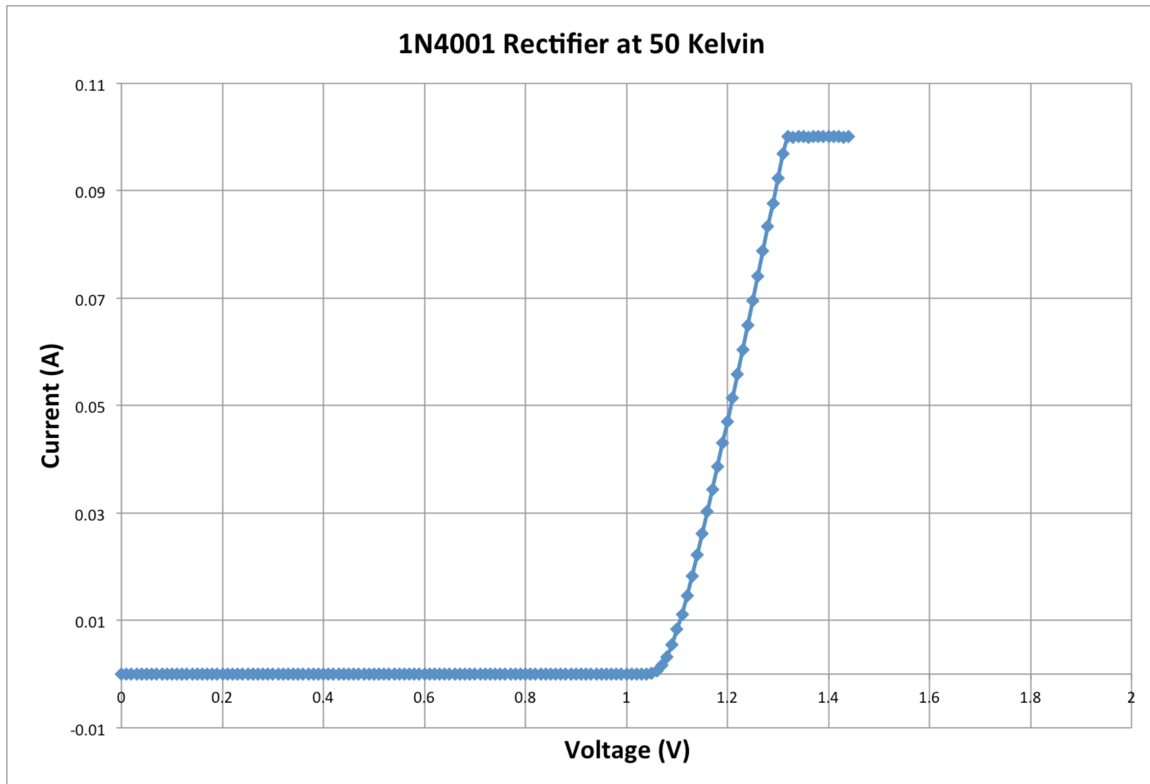


**Figure 4.7: 1N4001 Rectifier at 50 Kelvin**

Figure 4.7 shows the rectifier is still in working condition but the threshold voltage has shifted out to a little over one volt. The shifting of the threshold would be expected since there are now fewer electrons in the conduction band and the shift of approximately 500mV is in general keeping with the -2mV/$^{o}$C change expected for silicon. The flat line starting around 1.25 Volts was the current limit set for the test system.

The rectifier gives verification of theory, that carrier freeze-out does occur in semiconductors.

## 4.3 Bulk MOS FET

Next, a 2N7000 was tested at room temperature and at 5 Kelvin on the Janis system. This test was designed to give a base line for comparison to the SOS process FETs. Figures 4.8 and 4.9 show Id vs Vds and Id vs Vgs at room temperature for the 2N7000.

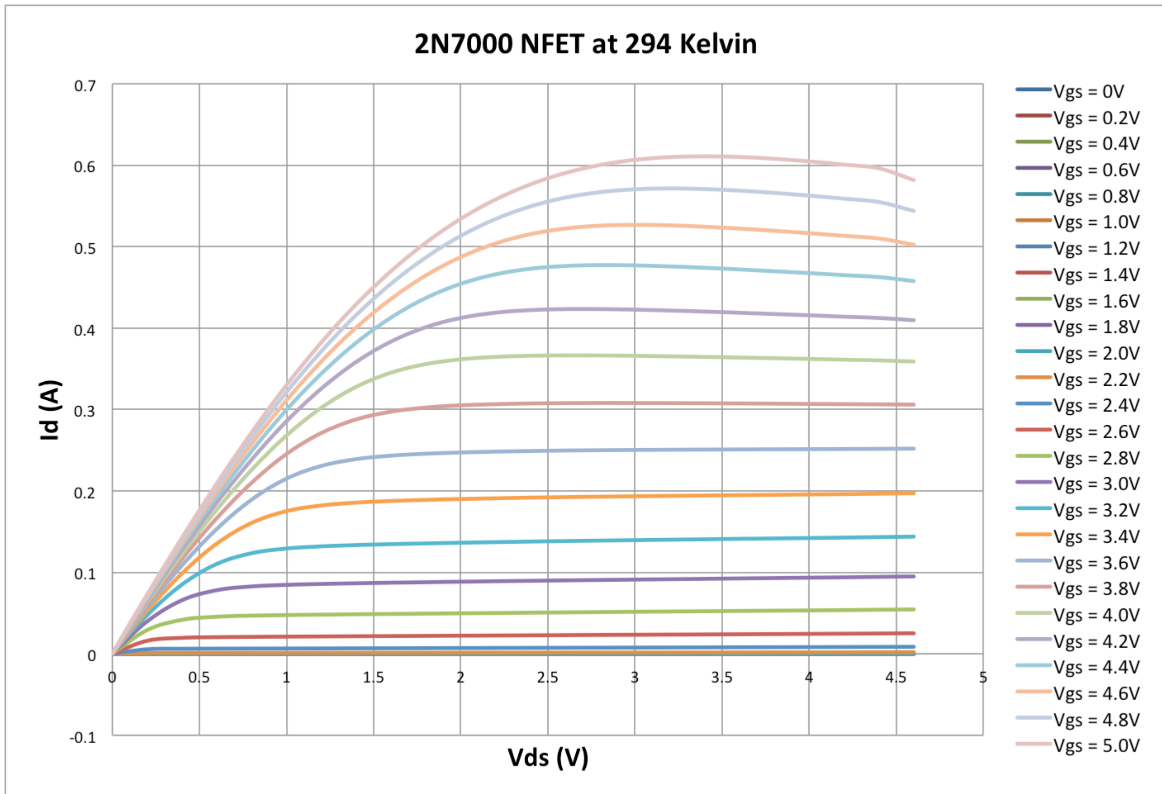


**Figure 4.8: 2N7000 NFET Id vs Vds at 294 Kelvin**

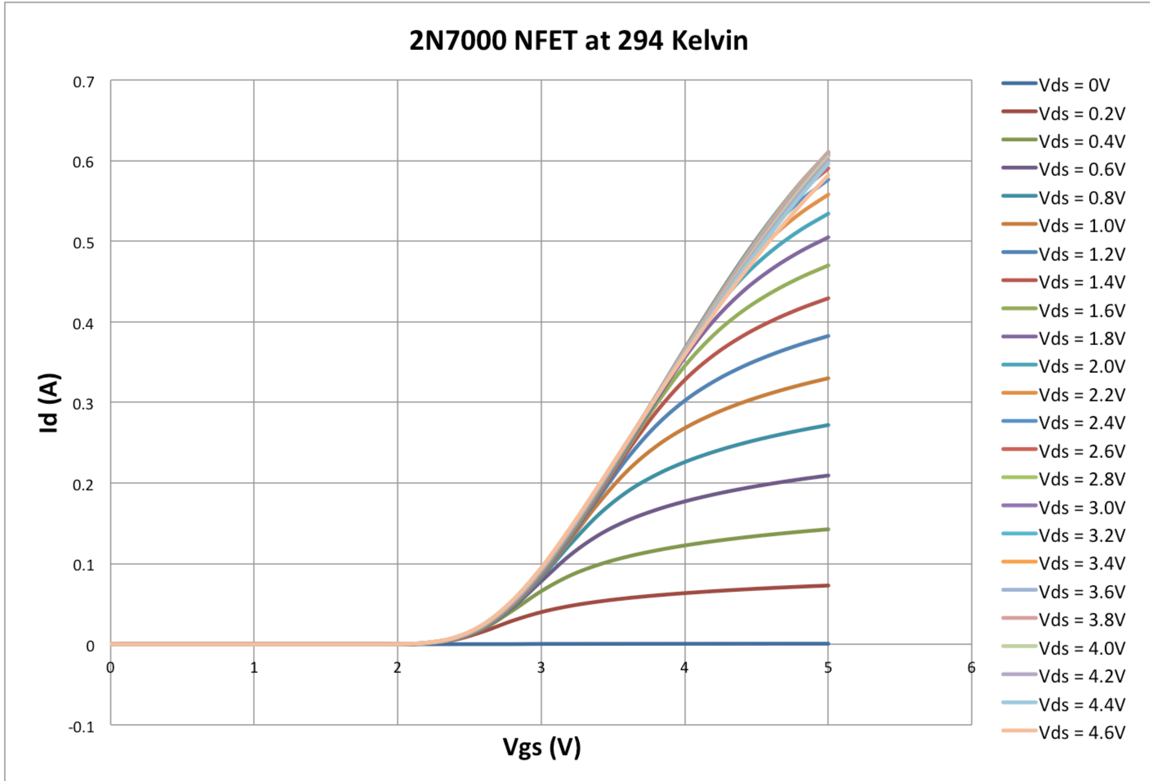


**Figure 4.9: 2N7000 NFET Id vs Vgs Curves at 294 Kelvin**

Figure 4.8 curves are as expected except for a little compression at higher Vgs values. The compression in the plots could be due to localized heating of the transistor. Figure 4.9 shows the threshold voltage appears to be around 2.2 volts.

Next, the 2N7000 transistor was brought down to 5 Kelvin to see if freeze-out occurs. Figures 4.10 and 4.11 show the Id vs Vds and Id vs Vgs curves for 5 Kelvin.

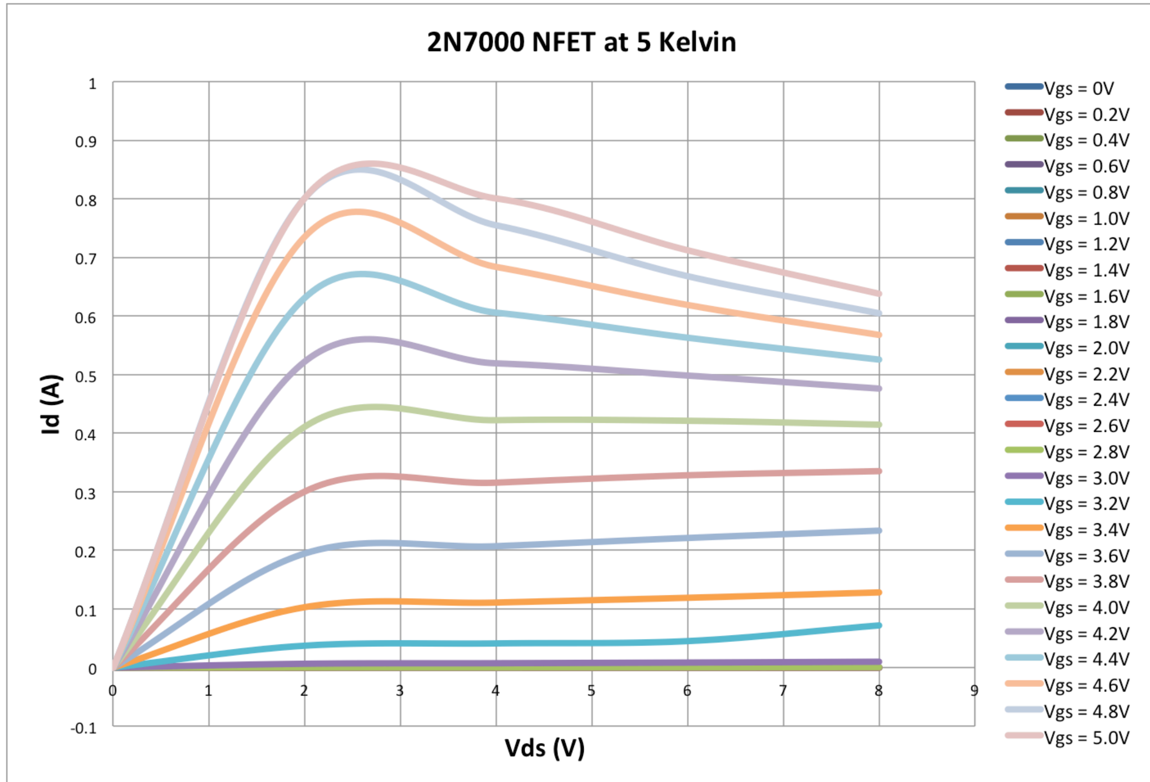


**Figure 4.10: 2N7000 NFET Id vs Vds Curves at 5 Kelvin**

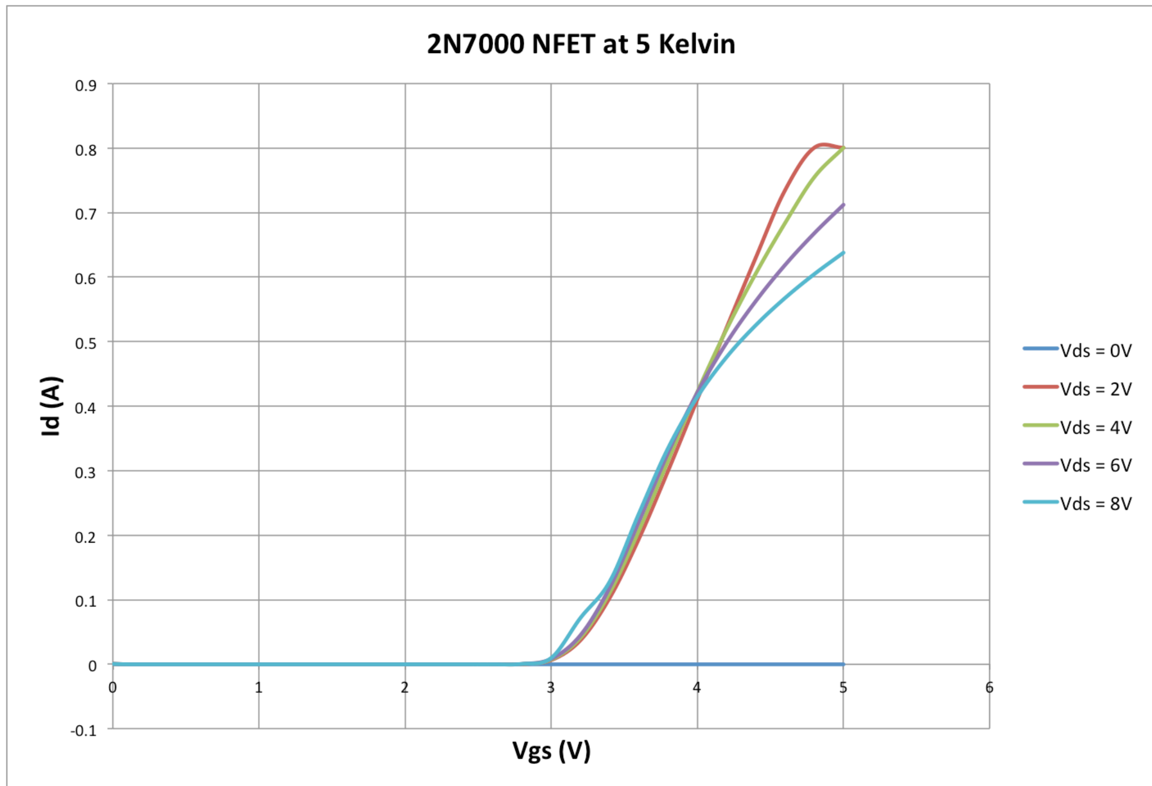


**Figure 4.11: 2N7000 NFET Id vs Vgs Curves at 5 Kelvin**

Figure 4.10 shows substantial compression in the curves at high Vgs voltages. This was presumed due to localized heating, similar to that seen in Figure 4.8. Figure 4.10 also shows a slight kink effect at low Vgs voltages. It is likely there is a kink in the other curves but due to heating could not be seen. A major difference in the 5 Kelvin measurements are the increased current levels the FET exhibits compared to the same points at room temperature. Figure 4.11 shows that the threshold voltage increased compared to the room temperature measurements. The threshold shifted out to about 3.0 Volts compared to 2.2 Volts at room temperature. This is most likely do to the FET operating near the freeze-out range. Complete carrier freeze out was not observed in this transistor.

## 4.4 SOS FET Measurements

The SOS FETs tested were 2µm HN and IN FETs on the Janis system and an RN FET on the CTI-Cryogenics system.

### *4.4.1 2µm HN FET*

The 2µm HN FET was tested at room temperature, 50 Kelvin, 30 Kelvin and 5 Kelvin. The 50 Kelvin and 30 Kelvin measurements help to fill in temperature data between room temperature and 5 kelvin not measured in [4]. Figures 4.12 and 4.13 show the room temperature results.

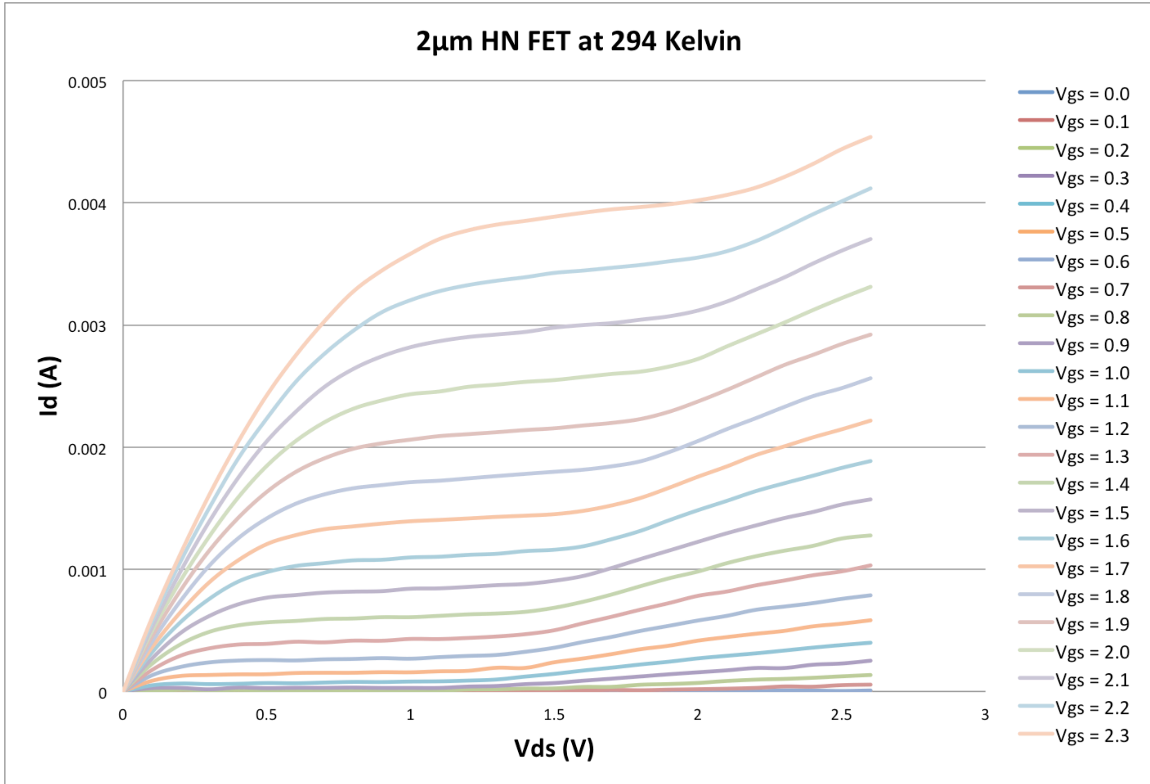


**Figure 4.12: 2µm HN FET Id vs Vds Curves at 294 Kelvin**

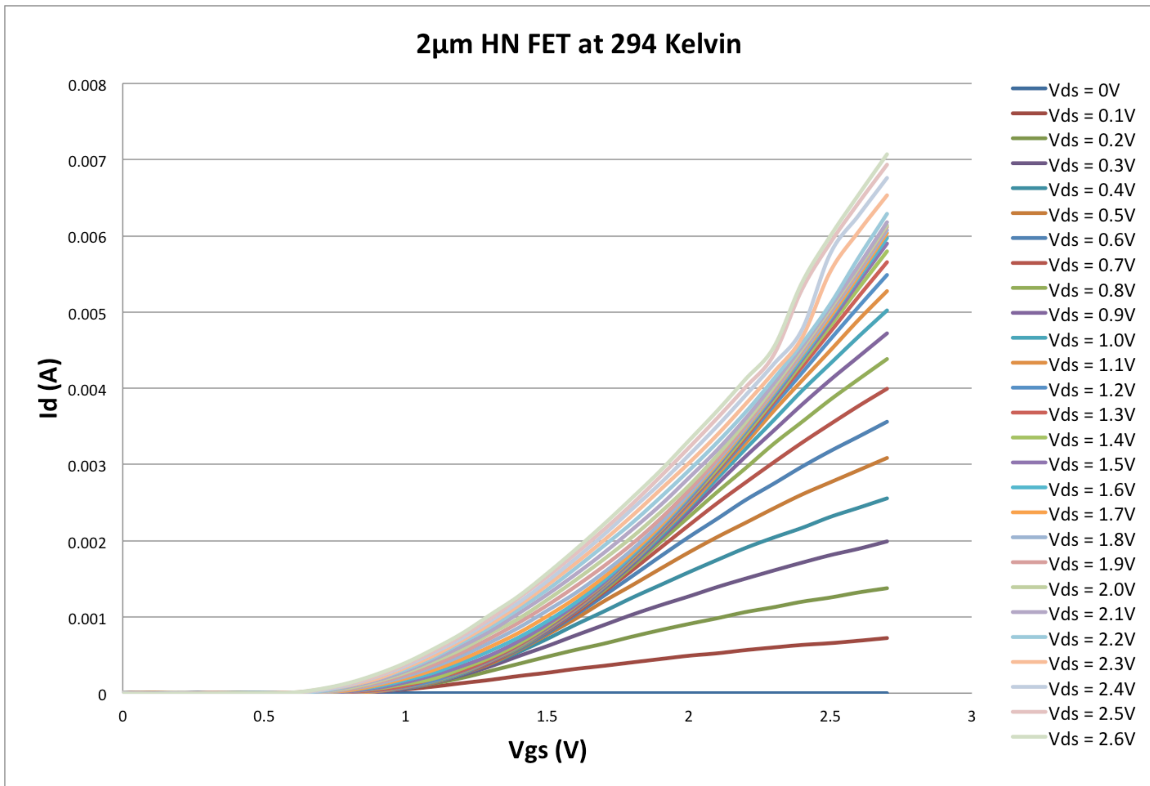


**Figure 4.13: 2µm HN FET Id vs Vgs Curves at 294 Kelvin**

Figure 4.12 clearly shows the kink effect known to exist in FD SOI although, the kink is very mild and limited to high Vds conditions. Figure 4.13 shows the threshold voltage is around 0.6 volts.

Figures 4.14 and 4.15 show the results at 50 Kelvin.

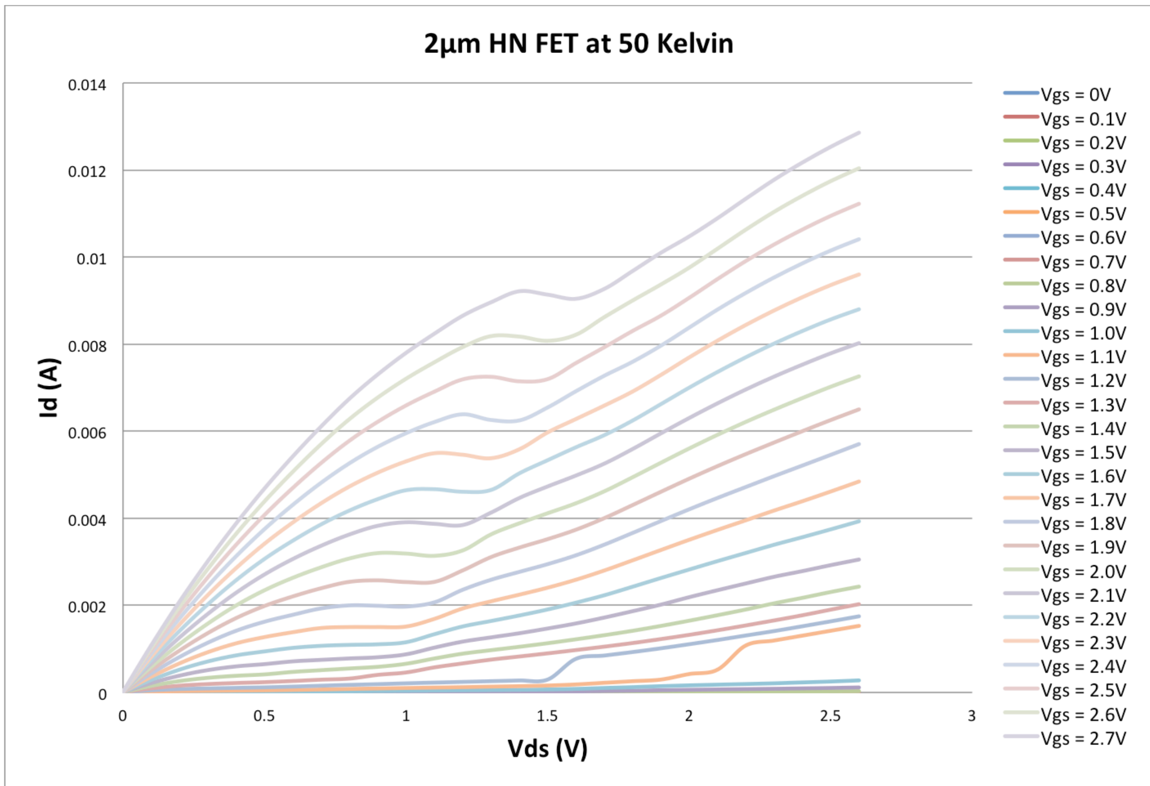


**Figure 4.14: 2µm HN FET Id vs Vds Curves at 50 Kelvin**

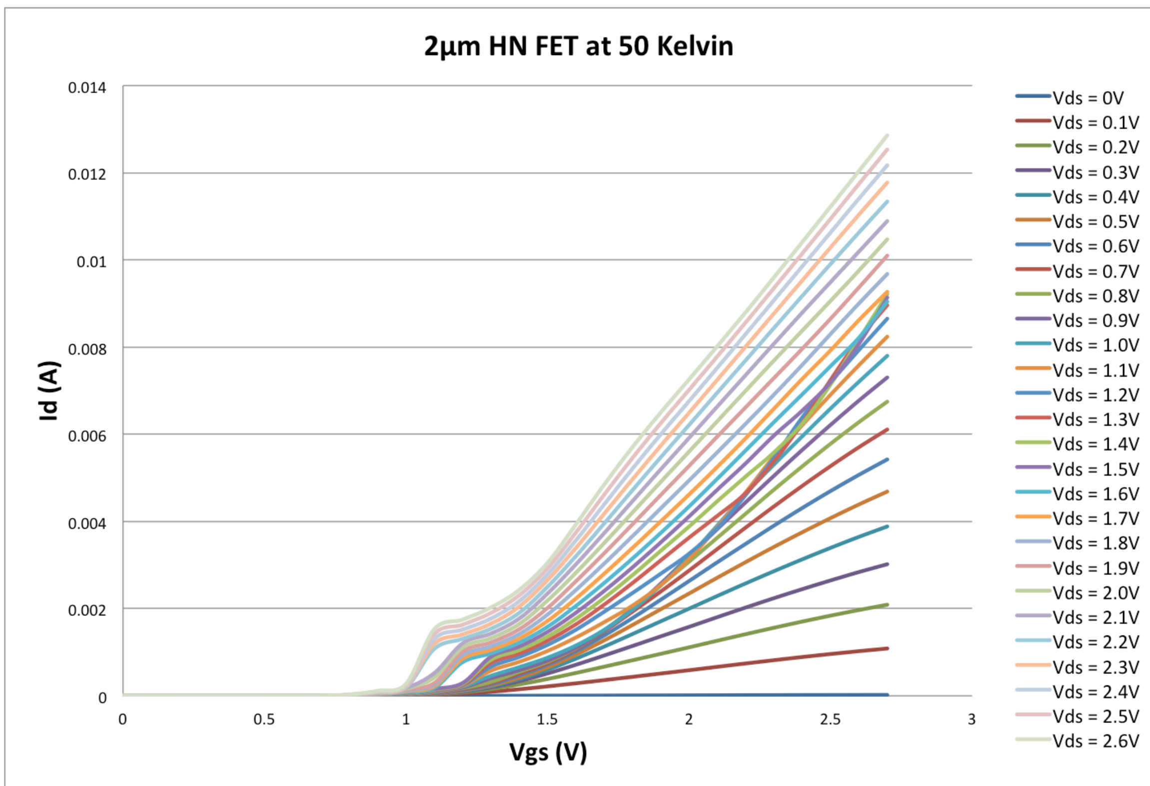


**Figure 4.15: 2µm HN FET Id vs Vgs Curves at 50 Kelvin**

At 50 Kelvin the kink effect becomes more extreme and starts at lower voltages. Figure 4.15 shows how the threshold voltages become larger. The threshold appears to be about 0.75 Volts, although the significant kinks make it difficult to specify a clear value. Figure 4.15 also shows an oddity at voltages just past the threshold, this maybe due to the kink effect occurring at lower voltages. The current levels have also increased. At Vgs = 2.1 Volts and Vds = 1 Volt, the current at 294 Kelvin was about 2.8mA and at 50 Kelvin it was about 3.9mA. Figures 4.16 and 4.17 show the results at 30 Kelvin.

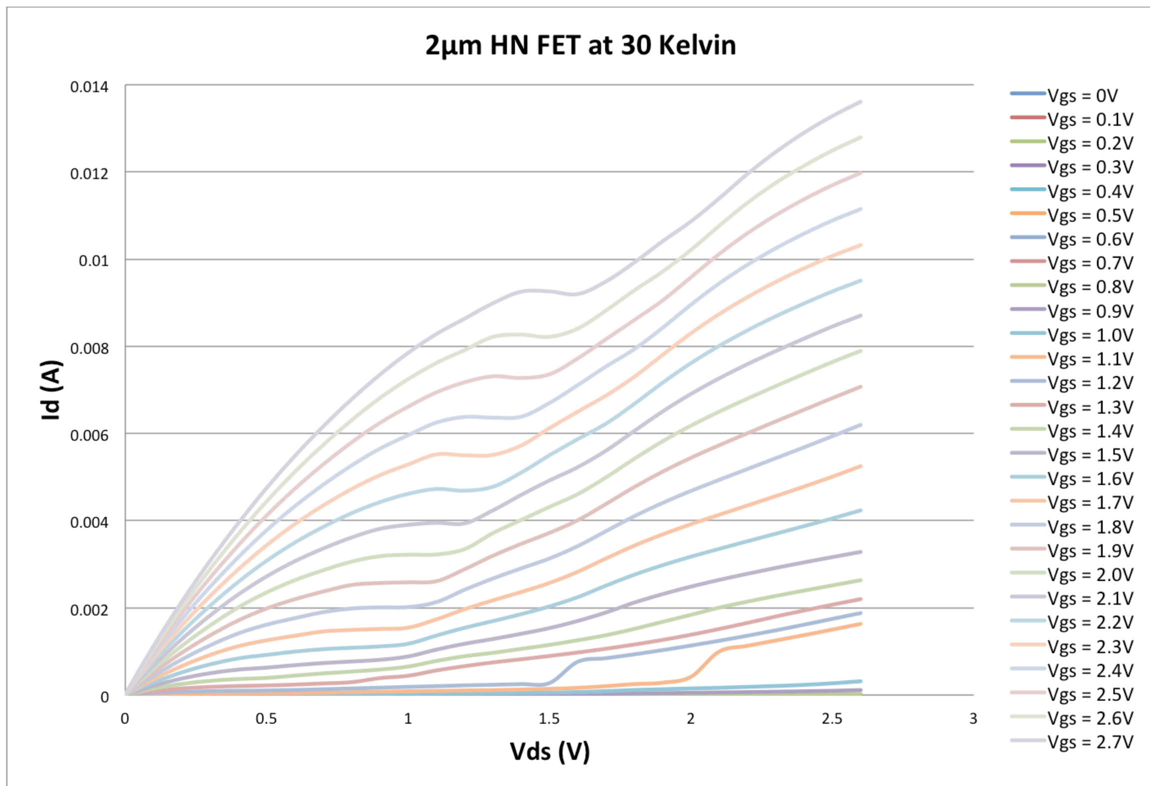


**Figure 4.16: 2µm HN FET Id vs Vds Curves at 30 Kelvin**

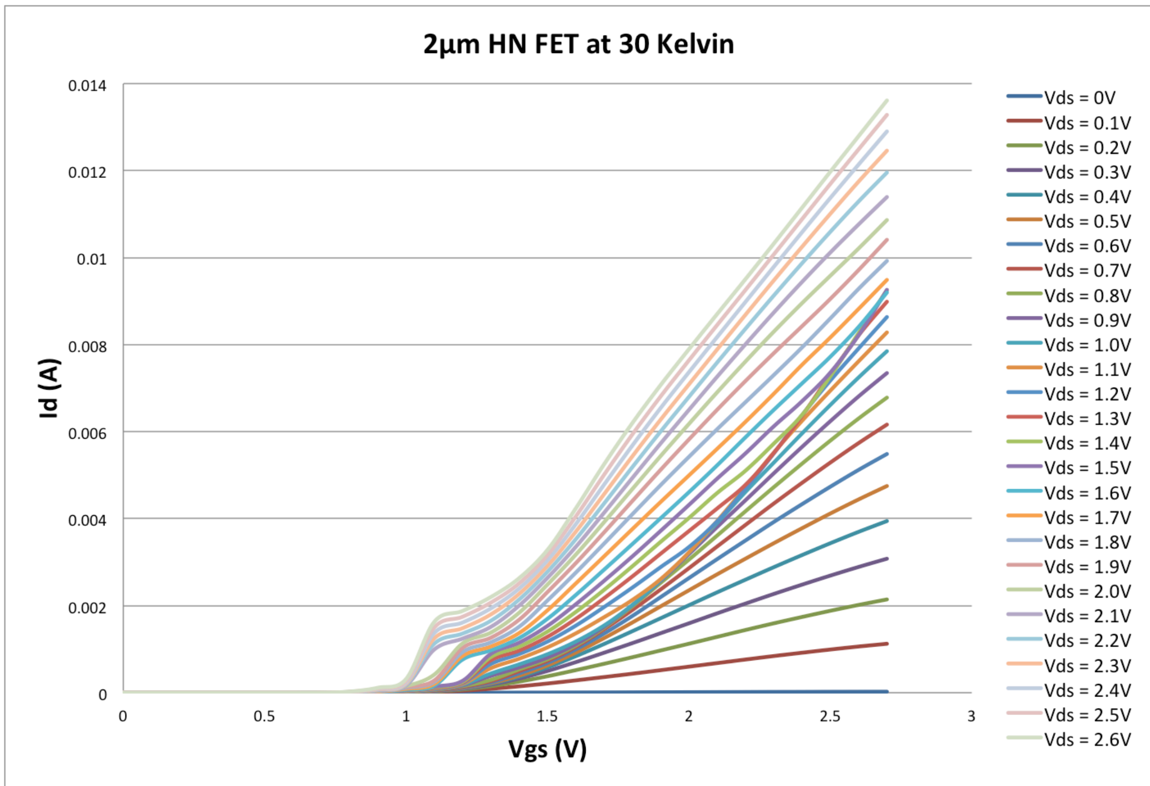


**Figure 4.17: 2µm HN FET Id vs Vgs Curves at 30 Kelvin**

Figures 4.16 and 4.17 appear almost the same except for an increase in maximum current at the same Vgs and Vds voltages. The strong kink effect is still visible and in similar places as at 50 Kelvin. The threshold voltage does not appear to have increased much if any.

Finally, Figures 4.18 and 4.19 show the HN FET results at 5 Kelvin:

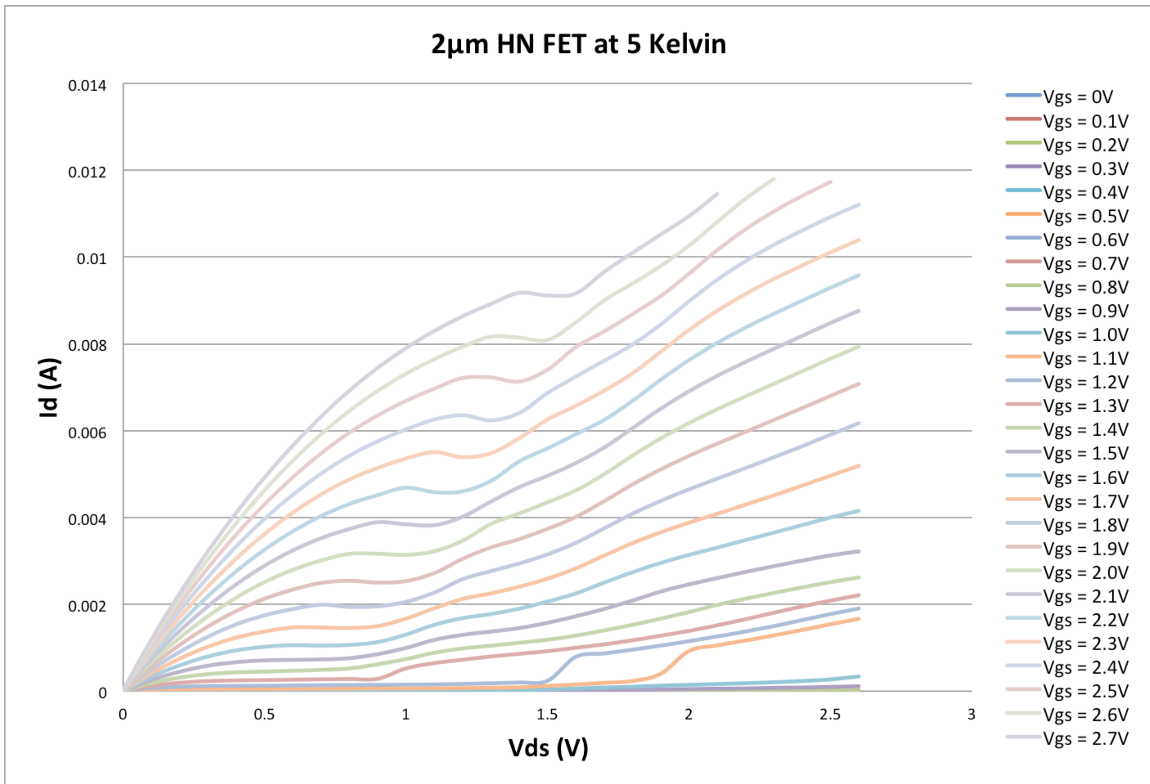


**Figure 4.18: 2µm HN FET Id vs Vds Curves at 5 Kelvin**

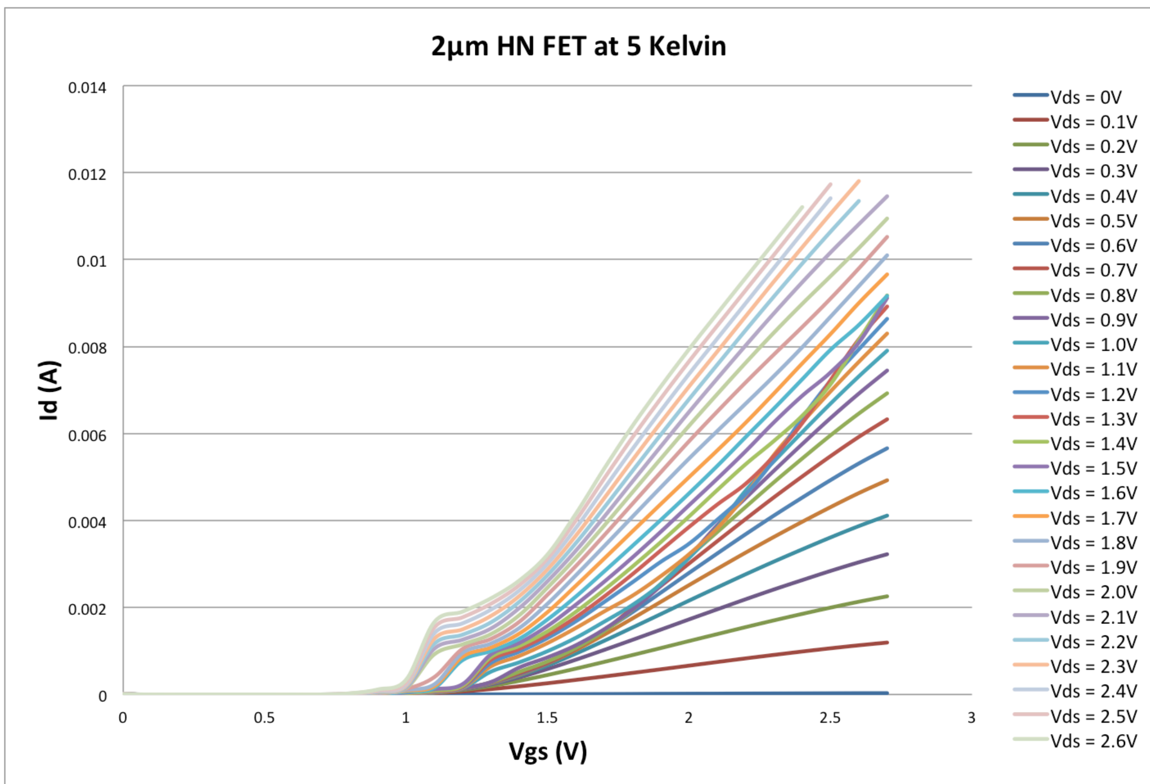


**Figure 4.19: 2µm HN FET Id vs Vgs Curves at 5 Kelvin**

There are a few data points missing from Figures 4.18 and 4.19 due to a problem in the original LabVIEW program. Figure 4.18 shows the kink effect appears to start at lower voltages compared to the 30 Kelvin measurements. The kink effect appearing at low Vgs voltages agrees with the results in Figure 2 (d) of [4]. The currents have stayed nearly the same, about 4mA. Figure 4.19 shows the threshold has not increased much if at all.

The main observations with the HN FET measurements are:

a) The kink effect becomes significant at cryogenic temperatures creating strong non-idealities in the Id curves.
b) Current levels increase and the threshold voltages increase.
c) The threshold voltage seemed to stop shifting once the temperature reached 50 Kelvin
d) The kink effect did not change much between 50 Kelvin and 30 Kelvin but did start a little earlier at 5 Kelvin.

Carrier freeze-out was never reached but the devices were clearly operating in the freeze out region.

### *4.4.2 2μm IN FET*

An intrinsic NFET was also tested with the hopes of observing freeze-out in a thin film transistor. Figure 4.20 and 4.21 show the results.

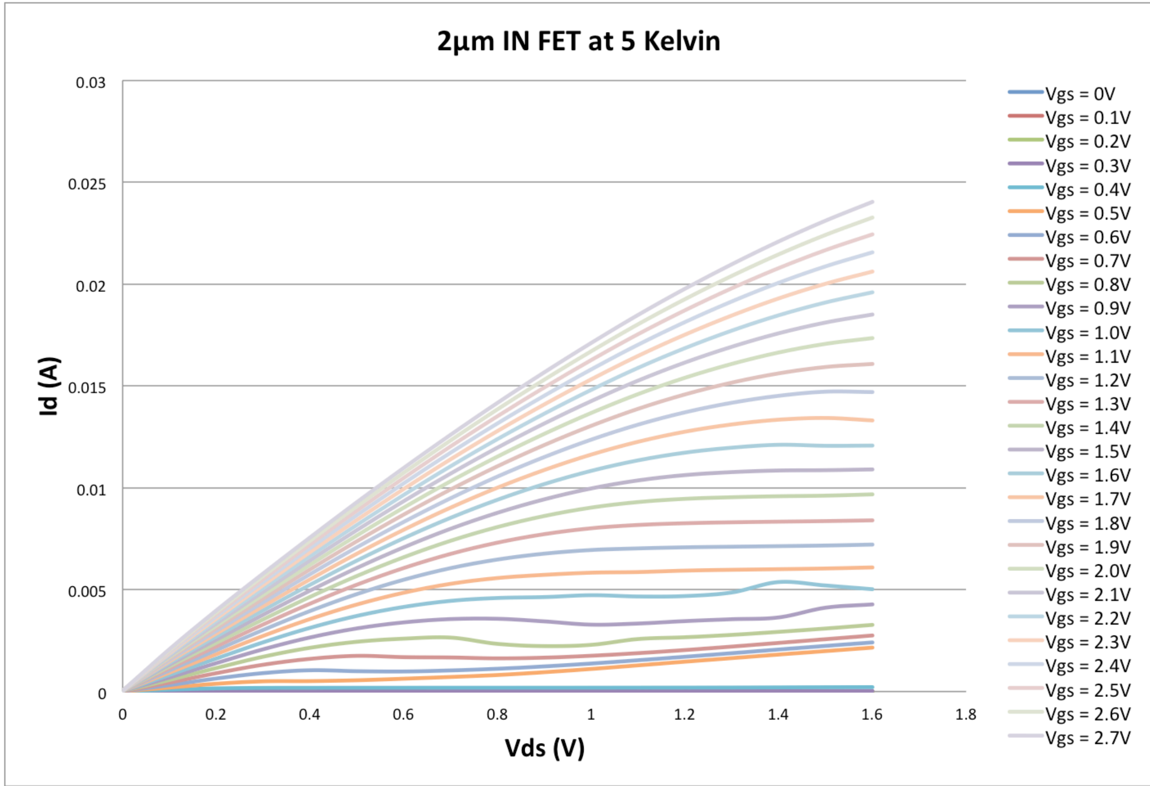


**Figure 4.20: 2µm IN FET Id vs Vds Curves at 5 Kelvin**

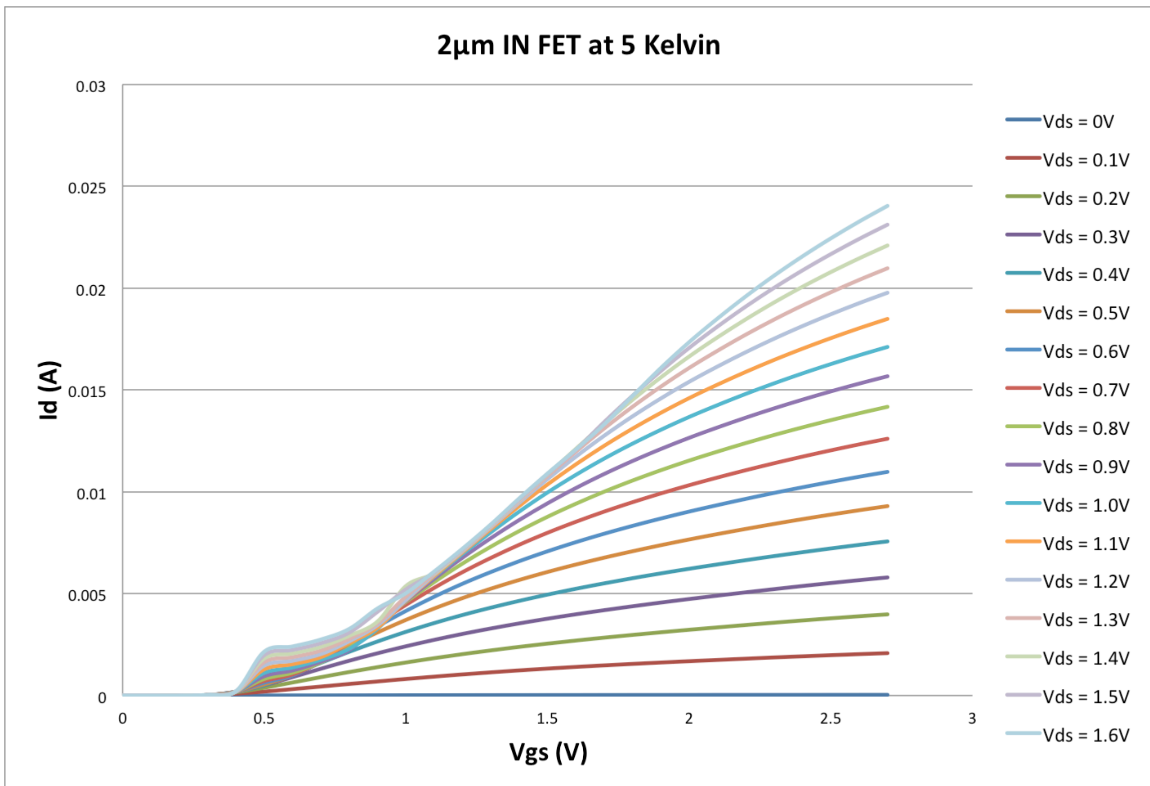


**Figure 4.21: 2µm IN FET Id vs Vgs Curves at 5 Kelvin**

Figures 4.20 and 4.21 are not on the same scales as previous graphs because there was an error when collecting the data. The error was most likely due to a problem in measurements because of the auto range setting on the DMM. Figure 4.20 does not show the kink effect. The kink effect was seen in the HN FET at 5 Kelvin as early as 0.75 volts. It is possible the kink effect is present but further out in the Id vs Vds curves where the data was excluded. The IN FET did not freeze-out and since it was presumed the IN FET would have a higher chance, it is reasonable to assume the SOS process will work down to at least 5 Kelvin.

### *4.4.3 2µm RN FET*

A few measurements were taken on a 2µm RN FET using the CTI-Cryogenics system. The new LabVIEW Program, documented in Appendix A, was used to obtain the data. Figures 4.22 and 4.23 show the RN FET characteristics at room temperature.

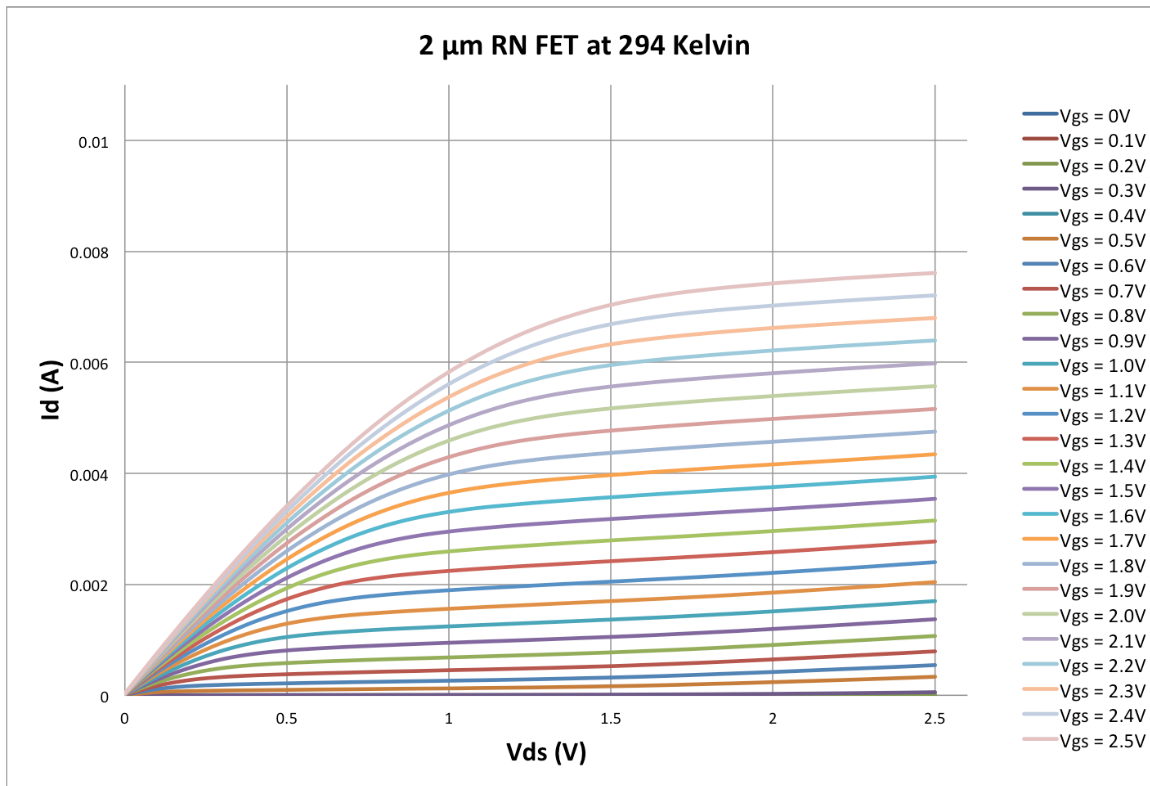


**Figure 4.22: 2µm RN FET Id vs Vds Curves at 294 Kelvin**

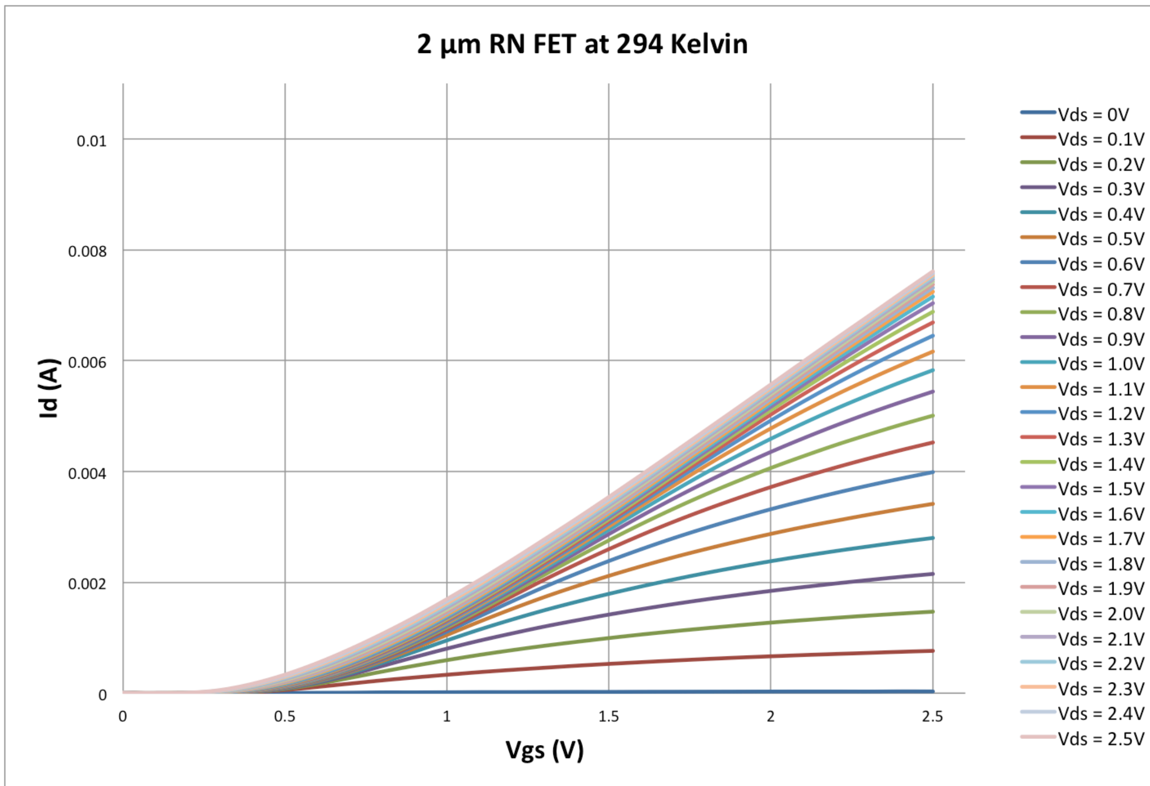


**Figure 4.23: 2µm RN FET Id vs Vgs Curves at 294 Kelvin**

Figure 4.22 shows the kink effect is not noticeable at room temperature. Figure 4.23 can be used to find the threshold voltage; it appears to be around 0.4 Volts. Figures 4.24 and 4.25 show the RN FET characteristics at 56 Kelvin.

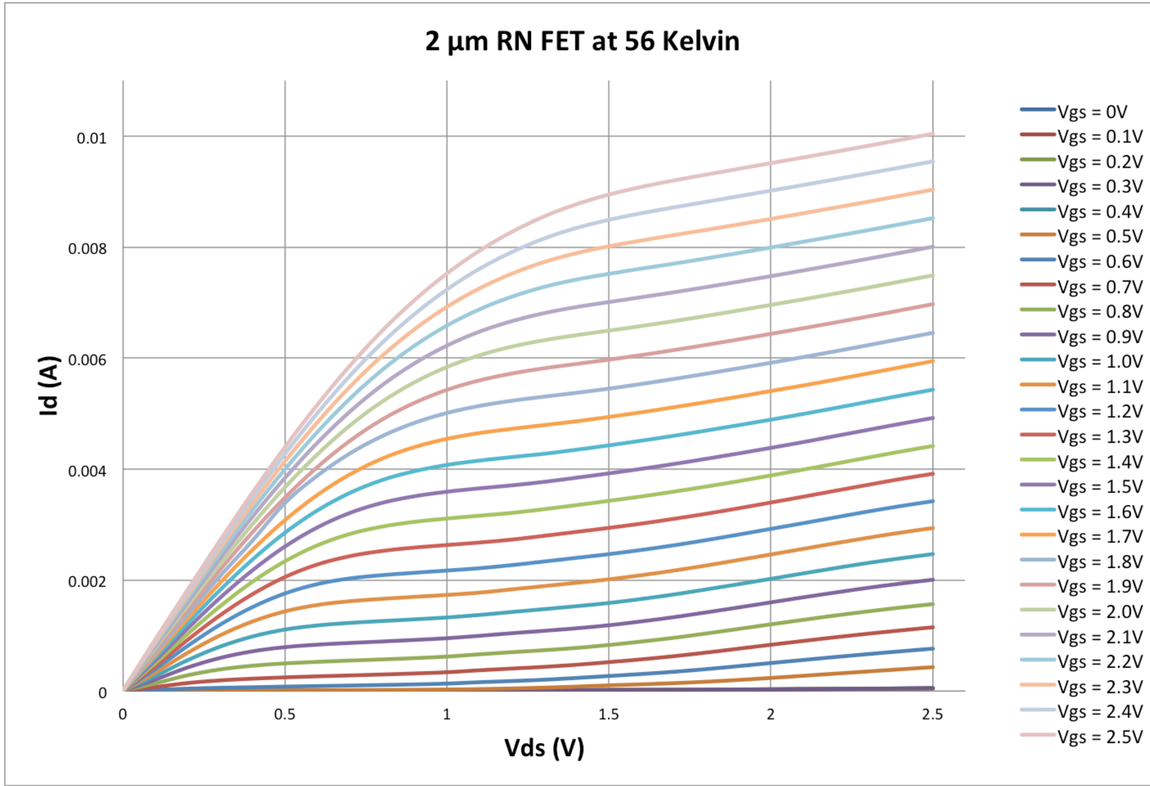


**Figure 4.24: 2μm RN FET Id vs Vds Curves at 56 Kelvin**

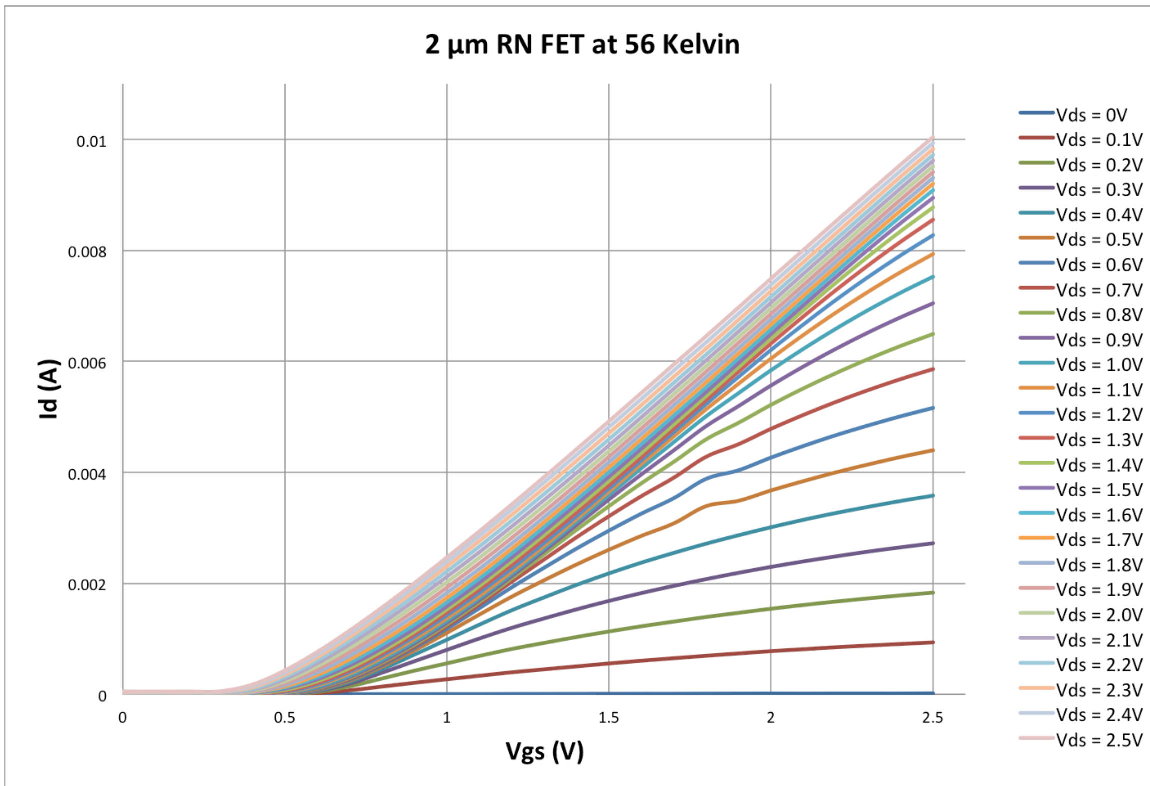


**Figure 4.25: 2μm RN FET Id vs Vgs Curves at 56 Kelvin**

Figure 4.24 shows how the currents have increased compared to room temperature and there is a slight kink effect. Figure 4.25 shows the threshold voltages have shifted out to about 0.5 Volts. There are some bobbles in a few curves in Figure 4.25; these are most likely instrumentation errors.

The RN FET seems to follow similar patterns seen in the HN and IN FETs. The threshold voltages and current levels increased, and the kink effect started earlier and became more evident. However, the degree of kink effect was substantially less than for the HN FET results.

# Chapter 5 - Conclusions and Future Work

This thesis presented data on the characteristics of bulk process and SOS devices at cryogenic temperatures. A resistor, a rectifier and several different types transistors were tested.

The SOS SN resistor did not experience carrier freeze-out but as temperature decreased the resistance increased from 11 kΩ to a maximum of 20.5 kΩ at 11 Kelvin. When operating in the freeze-out range there are fewer carriers in the conduction band, which increases the effective resistance in the SN resistor. The resistor also experienced localized heating, which changed the temperature the resistor was actually operating at, skewing the results. The localized heating problem is something designers should keep in mind, because if driving semiconductor devices at high power dissipations the local temperature will actually be warmer than the ambient environment.

A bulk process rectifier, a 1N4001, was tested to observe carrier freeze-out. When the rectifier was measured at 5 Kelvin, current never started to flow even with 3.5 Volts applied. The rectifier experienced carrier freeze-out, verifying the Janis system could induce the phenomenon. When the temperature was brought up to 50 Kelvin, the rectifier began to flow current again verifying it was still functional.

A 2N7000 bulk process NFET was tested at 5 Kelvin to see if carrier freeze-out could be seen. The transistor never experienced carrier freeze-out but the threshold voltage and currents increased. The increased currents may have caused localized heating, which appeared as compression of the curves at higher Vgs voltages. At low Vgs voltages the transistor showed a slight kink effect. The kink effect could be present in the other graphs but due to the localized heating could not be seen.

A 2µm SOS HN FET was tested at 294, 50, 30 and 5 Kelvin. The threshold voltages and currents increased at 50 Kelvin but seemed to stay the same or experienced minimal change at 30 and 5 Kelvin. The kink effect visible at 294 Kelvin became more extreme and occurred at lower Vds voltages as the temperature was lowered. It appears the threshold and currents will increase when the temperature is decreased and then remain relatively unchanged. The kink effect, on the other hand, will continue to occur at lower Vds values as temperature is decreased. The kink effect prevents the HN FET from being a reliable device for amplifier designs at cryogenic

temperatures because the saturation region is not stable. The output resistance decreases in the transistor and the gain decreases.

A 2μm SOS IN FET was tested because it is lightly doped and presumed to be more susceptible to carrier freeze-out. When tested at 5 Kelvin, the IN FET never experienced carrier freeze-out, which means it is likely most SOS devices will work down to 5 Kelvin.

Finally, a 2μm SOS RN FET was tested at 294 and 56 Kelvin. The RN FET did not show the kink effect at 294 Kelvin. When the RN FET was brought down to 56 Kelvin, it showed increases in the threshold voltage and current levels. The kink effect also began to appear at 56 Kelvin. The RN FET followed the same patterns seen in the previously tested devices.

When designing devices to operate at cryogenic temperatures, there are a few characteristic changes to consider. SN resistor values will increase steadily down to 5 Kelvin. The threshold voltages of transistors increase down to 50 Kelvin and remain somewhat consistent to 5 Kelvin. The currents follow a similar pattern as the threshold voltages. The kink effect appears to keep occurring earlier as temperature continues to fall. When designing circuits for cryogenic environments, it is recommended not to use HN FETs but instead use RN or IN FETs, which appear to be much more predictable while in saturation.

## 5.1 Future Work

Further experimentation should be done in cryogenic temperature testing. Testing a few SOS diodes would be a great expansion on this research. The bulk process rectifier tested may not have the same characteristics as an SOS diode. Different channel lengths should be tested to see if shorter or longer lengths change the effects at cryogenic temperatures. Testing a partially depleted (PD) SOI would also be a great addition. A wider range of temperature measurements should be done. More measurements should be taken at 150, 100, 77 and 25 Kelvin to see if the threshold voltages and currents stop increasing at specific temperature ranges. Estimating the temperature rise of the SN resistor at any given power through thermal modeling of the heat flow would expand on the data presented here.

The LabVIEW program developed in this thesis did not include code to support a temperature controller. It would be beneficial to have automated control of a temperature

controller.  The program also needs more error checking and safety features to prevent infinite loops.

# References

[1] Albers, K. B., “Noise Characteristics of Transistors in 0.25μm and 0.5μm Silicon-on-Sapphire Processes,” M.S. thesis, ECE, KSU, Manhattan, KS, 2010.

[2] Baker, R. J., *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ: Wiley, 2010.

[3] Clarke, J., “SQUIDS: Theory and Practice,” in *The New Superconducting Electronics,* Dordrecht, The Netherlands, Kluwer Academic, 1993, pp.123-180.

[4] Ekanayake, S.R.; Lehmann, T.; Dzurak, A.S.; Clark, R.G.; Brawley, A., "Characterization of SOS-CMOS FETs at Low Temperatures for the Design of Integrated Circuits for Quantum Bit Control and Readout," Electron Devices, IEEE Transactions on , vol.57, no.2, pp.539-547, Feb. 2010
doi: 10.1109/TED.2009.2037381

[5] Ghibaudo, G.; Balestra, F., "Low Temperature Characterization of Silicon CMOS Devices," Microelectronics, 1995. Proceedings., 1995 20th International Conference on , vol.2, no., pp.613-622 vol.2, 12-14 Sep 1995
doi: 10.1109/ICMEL.1995.500938

[6] Hammoud, A.; Patterson, R.L.; Gerber, S.; Elbuluk, M., "Electronic Components and Circuits for Extreme Temperature Environments," Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on , vol.1, no., pp. 44- 47 Vol.1, 14-17 Dec. 2003
doi: 10.1109/ICECS.2003.1301972

[7] Imthurn, G., “The History of Silicon-on-Sapphire,” Peregrine Semiconductor, San Diego, CA, 2007.

[8] Kato, K.; Wada, T.; Taniguchi, K., "Analysis of Kink Characteristics in Silicon-on-Insulator MOSFET's Using Two-Carrier Modeling," Solid-State Circuits, IEEE Journal of , vol.20, no.1, pp.378-382, Feb. 1985
doi: 10.1109/JSSC.1985.1052317

[9] Neamen, D. A., *Semiconductor Physics and Devices: Basic Principles*, 2nd ed. Chicago, IL: Irwin, 1997.

[10] Sedra, A. S and Smith, K. C., *Microelectronic Circuits*, 5th ed. New York, NY: Oxford University Press, 2004.

[11] Singh, J., *Semiconductor Devices: Basic Principles*, New York, NY: Wiley, 2001.

[12] Sze, S. M., *Semiconductor Devices: Physics and Technology*, 2nd ed. New York, NY: Wiley, 2001.

[13] Tugnawat, Y., "Low Temperature Performance of Commercial-Off-the-Shelf (COTS) Electronic Components for Future Mars Missions," M. S. Thesis, ECE, KSU, Manhattan, KS, 2001.

[14] Wang, J.; Chang, J.; Raman, V.K.; Vasudev, P.K.; Viswanathan, C.R., "Electrical characterization of SOS n-MOSFETs at cryogenic temperatures," SOS/SOI Technology Conference, 1989., 1989 IEEE , vol., no., pp.41-42, 3-5 Oct 1989
doi: 10.1109/SOI.1989.69756

[15] Yuan, J.; Patel, J.U.; Vandooren, A., "Performance Evaluation of Deep Sub-micron, Fully-Depleted Silicon-on-Insulator (FD-SOI) Transistors at Low Temperatures," Aerospace Conference Proceedings, 2000 IEEE , vol.5, no., pp.415-419 vol.5, 2000
doi: 10.1109/AERO.2000.878516

# Appendix A - LabVIEW FET Curve Tracer F2012 Code

This section will present the LabVIEW FET Curve Tracer Code Developed for this thesis. This appendix is an instruction manual on how to operate the program. This program was designed to work with one **Agilent 34401A DMM** and two **Agilent E3641A Power Supplies**.

## How to Use FET Curve Tracer F2012

This section will show how to use the newly developed FET Curve Tracer. The first thing you should do is hit “ctrl + h” to open up the LabVIEW context help window. Whenever you scroll over a section on the front panel a text help guide will appear in the new window. There is documented help for each part of the front panel in the context window. This section will also present information on the sections of the front panel in Figure A.1.

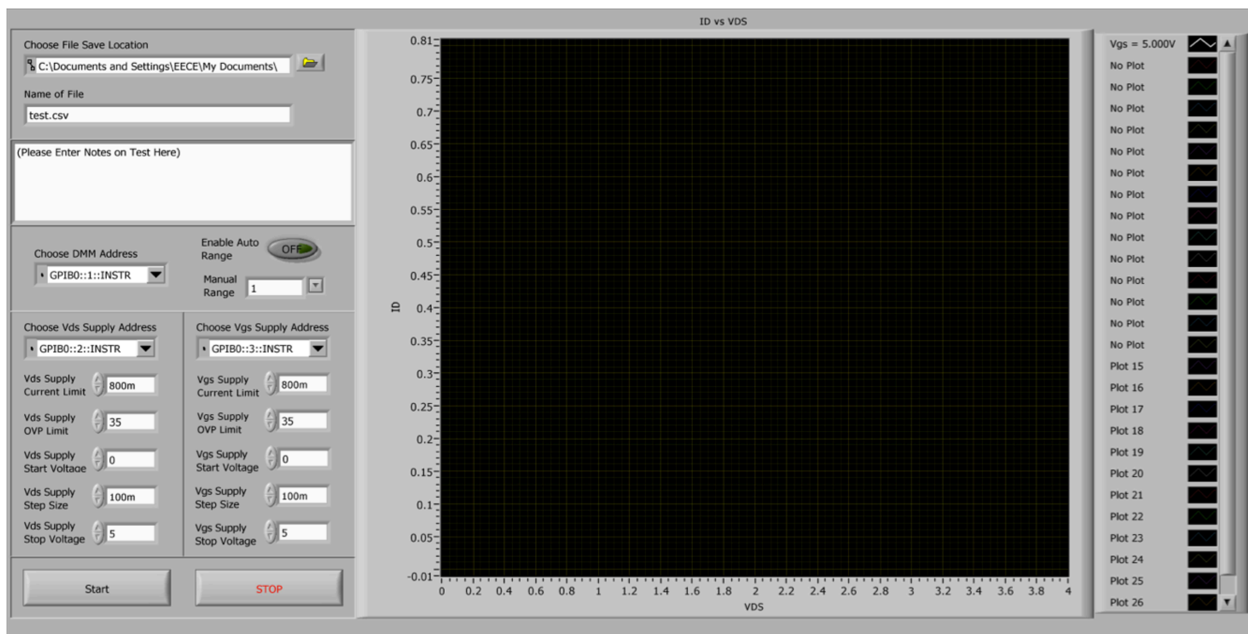


**Figure A.1: FET Curve Tracer F2012 Front Panel**

The first section on the front panel is the “Choose File Save Location.” Select the file image to the right of the text input box. In the window that appears select the folder you would like to have your data files saved in. When you have selected a folder click “Use Current Folder.”

Next, go to the input text box named “Name of File.” Name your file and be sure to include the desired extension of the file. **If you want to import into Microsoft Excel be sure**

**to use the .csv format.** You can also save the files as a .txt, if desired. The file save format is comma-separated values so saving as a .csv will automatically format when imported to Excel.

The next section is a text box where you can input various notes to help you identify your test. I recommend documenting the nature of the test and any initial conditions.

The next section is to set up the Agilent 34401A DMM GPIB address. If you are unsure of the assigned address, watch when starting up the DMM and wait for "addr #" to appear on screen. The number displayed is the GPIB address. You can change the DMM's GPIB address. Please refer to the user manual provided by Agilent for the instructions on how to do this.

If you want auto-range on the DMM to work you will have to flip the switch labeled "Enable Auto Range" so the green light is on. I do not recommend this since this will most likely skew your results.

The next section is the "Manual Range" setting. There are only 4 options here. The choices are 10, 1, 0.1 and 0.01 where the one represents the maximum place the expected data will reach. If you are measuring a device that will reach 800mA, you might want to set the manual range to 1.

Treat the power supply "GPIB Address" the same as with the DMM setting. You can also find the address of the power supply the same way as with the DMM.

The "Vds Supply Current Limit" and "Vgs Supply Current Limit" boxes set the current limit of the power supplies. I recommend setting this to a save value that will not destroy your device.

The "Vds Supply OVP Limit" and "Vgs Supply OVP Limit" sets the Over Voltage Protection limit for the supplies. I recommend setting to a limit that will ensure device integrity in case of a failure.

"Vds Supply Start Voltage" and "Vgs Supply Start Voltage" settings set the starting voltage of the voltage sweeps. Usually you will leave this at zero unless you know the device will not turn on until much later.

The "Vds Supply Step Voltage" and "Vgs Supply Step Voltage" sets the step size of the voltage sweep. Make sure the value is small enough to obtain good resolution on the data collected.

The “Vds Supply Stop Voltage” and “Vgs Supply Stop Voltage” sets the maximum sweep voltage the supplies will reach before the next loop begins and ending point for the measurements.

*****NOTE: Make sure** $\frac{(\boldsymbol{Stop\ Voltage})-(\boldsymbol{Start\ Voltage})}{(\boldsymbol{Step\ Voltage})}$ **is equal to a whole number or the voltage supplies will never reach the stop criteria in the program and will bypass the stop voltage you have set and loop indefinitely. *****

Once you have got all the settings above set you can hit the LabVIEW run button in the upper left of the LabVIEW Window. Do not use the “Run Continuously” option. Once you press the “START” button the program will begin to run. If you want to stop the program you can hit the “STOP” button and the power supplies should return to the off state. When the program finishes a pop-up window with a text box will appear. You can enter any interesting observations you would like to include in the data file.