BUILT-IN SELF-TEST IN INTEGRATED CIRCUITS – ESD EVENT MITIGATION AND DETECTION

by

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Abstract

When enough charges accumulate on two objects, the air dielectric between them breaks down to create a phenomenon known as electrostatic discharge (ESD). ESD is of great concern in the integrated circuit industry because of the damage it can cause to ICs. The problem will only become worse as process components become smaller.

The three main types of ESD experienced by an IC are the human body model (HBM), the charged device model (CDM), and the machine model (MM). HBM ESD has the highest voltage while CDM ESD has the highest bandwidth and current of the three ESD types.

Integrated circuits generally include ESD protection circuitry connected to their pads. Pads are the connection between the IC and the outside world, making them the required location for circuitry designed to route ESD events away from the IC's internal circuitry. The most basic protection pads use diodes connected from I/O to VDD and I/O to ground. A voltage clamp between VDD and ground is also necessary to protect against CDM and MM event types where the device may not yet have a low impedance supply path connected.

The purpose of this research is to investigate the performance of ESD circuits and to develop a method for detecting the occurrence of an ESD event in an integrated circuit by utilizing IC fuses. The combination of IC fuses and detection circuitry designed to sense a broken fuse allows the IC to perform a built-in self-test (BIST) for ESD to identify compromised ICs, preventing manufacturers from shipping damaged circuits.

Simulations are used to design an optimized protection circuit to complement the proposed ESD detection circuit. Optimization of an ESD pad circuit increases the turn-on speed of its voltage clamps and decreases the series resistance of its protection diodes. These improvements minimize the stress voltage placed on internal circuitry due to an ESD event. An ESD measurement setup is established and used to verify voltage clamp operation.

This research also proposes an ESD detection circuit based on IC fuses, which fail during an ESD event. A variety of IC fuses are tested using the ESD measurement setup as well as a TLP setup in order to determine the time and current needed for them to break. Suitable IC fuses have a resistance less than 5 Ω and consistently break during the first trial.

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Dedication

There have been so many influential people in my life, from family members to teachers to friends. This work is dedicated to all of them, especially if they have the patience to read all of these pages. I cannot please all of you all the time, but I do hope I have made you proud.

There's nothing you can do
If you're too scared to try

Chapter 1 - Electrostatic Discharge (ESD) Basics

1.1 ESD Introduction

When enough charges accumulate on two objects, the air dielectric between them breaks down to create a phenomenon known as electrostatic discharge (ESD). ESD is of great concern in the integrated circuit industry because of the damage it can cause to ICs. Hit with an ESD event, an IC experiences a sharp increase in voltage and temperature which can melt junctions, vaporize oxides, and melt/vaporize metals [1]. A material's tolerance to the rapid heating of an ESD event is proportional to its size. Large devices have a higher heat capacity; therefore they can tolerate a larger ESD shock.

Unfortunately for the ESD weary, IC processes continue to progress toward smaller and smaller devices in order to facilitate the higher operating speeds demanded by society. New processes invariably have thinner oxides, smaller PN junctions, narrower metal lines, and smaller vias [1]. Each of these features allows for smaller, faster devices at the cost of being more vulnerable to an ESD event. As a result, ESD event protection research continues to be crucial to the IC design process, increasing production yields and product longevity. The first part of this research focuses on the design and characterization of ESD protection elements and how they respond to an ESD event. The second aspect of this ESD research focuses on development of an effective method to detect an ESD event in an integrated circuit.

1.2 ESD Types

Depending on the source, there are three ways of modeling the ESD experienced by an IC. The human body model (HBM) emulates the ESD event that occurs when a charged human finger touches an IC. A second type of ESD is emulated by the charged device model (CDM) and is found in the electronics manufacturing process [2]. As an IC package moves down a track, for example, charge can accumulate on the IC. When the package then comes into contact with a conductor of a different potential, a rapid event occurs between the IC and the conductor. Finally, the machine model (MM) characterizes the discharge from a charged conductor to an IC, such as the discharge that occurs when a bonding machine makes contact with a bond pad [1].

1.2.1 The Human Body Model

Modeling a human body ESD event consists of charging a 100 pF capacitor to a high voltage then throwing a switch to discharge the cap through the series combination of a 1.5 kΩ resistors and the device under test (DUT). Figure 1.1 shows the test circuit schematic. Depending on the target ESD Association (ESDA) sensitivity classification, the high voltage supply (Vdc) varies. The human body model has six stress levels ranging from 250 V to 8 kV [3]. An HBM event has the highest voltage levels but the smallest current levels of the three ESD types. Due to the high voltages, however, HBM current levels can still reach the amp range.

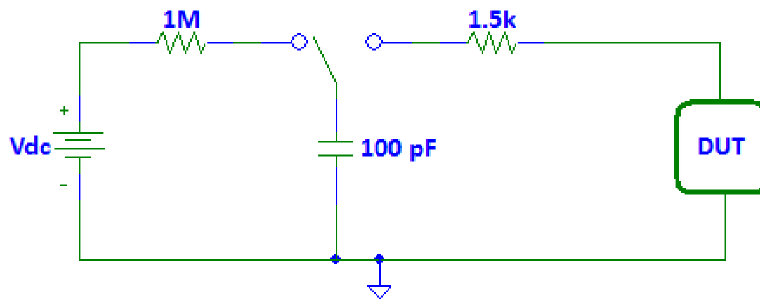

Figure 1.1 HBM Equivalent Schematic [4]

In a typical HBM case, the DUT experiences a sharp impulse of current that reaches 1 A by 10 ns. After reaching this peak, the current through the DUT decreases relatively slowly with a fall time of approximately 150 ns. Figure 1.2 shows this wave shape.

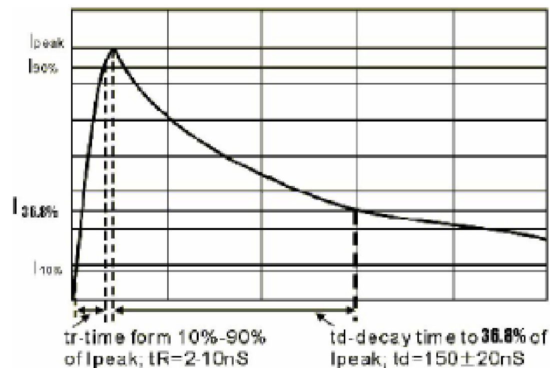

Figure 1.2 Current vs Time for a HBM Event (figure from [4])

1.2.2 The Charged Device Model

Establishing a model for a charged device ESD event is a difficult task. A CDM event discharges much larger currents (10 to 20 A) in a much smaller timeframe (2 to 4 ns) than the other two ESD types [1] [5]. As a result of being a high frequency event, device and test circuit parasitics largely determine the response of a CDM event. Figure 1.3 shows a simplified equivalent schematic for a CDM event, modeling a CDM event as an LCR circuit. In this simplified model, the capacitance consists of any parasitic capacitances and gate capacitances connected to the test pad as well as the package capacitance. Most of the resistance and inductance is from the arm of the wire bonder, which completes the circuit by touching the pad.

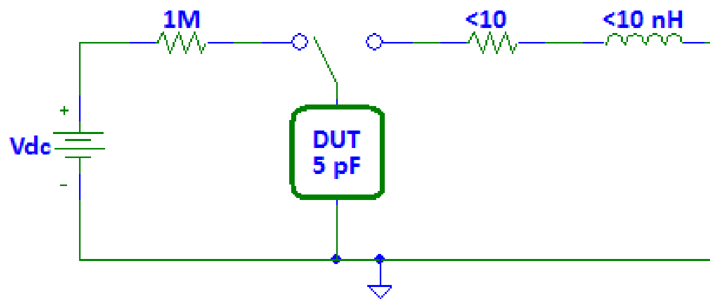

Figure 1.3 CDM Equivalent Schematic [1]

Figure 1.4 shows the LCR response of a CDM event compared to a HBM event, illustrating the dramatic difference between the two. The CDM event is over before an HBM event would have time to reach its peak. Due to the high current levels, a CDM event is the most destructive type of ESD event and the most difficult to protect against [1]. The charged device model has seven levels of sensitivity ranging from 125 V to 2 kV [6].

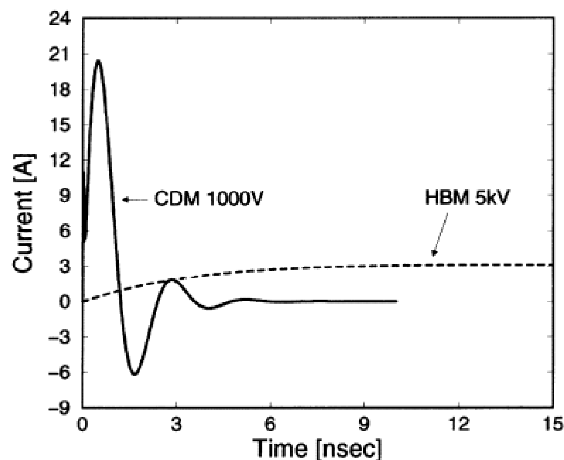

Figure 1.4 CDM Event Response vs. HBM Event Response (figure from [5])

1.2.3 The Machine Model

Shown in Figure 1.5, the machine model contains a charged capacitor in series with a 10 Ω resistor, a 700 nH inductor, and the DUT. The machine model has the lowest voltage levels of the three ESD types, with five stress levels ranging from 25 V to 400 V [7].

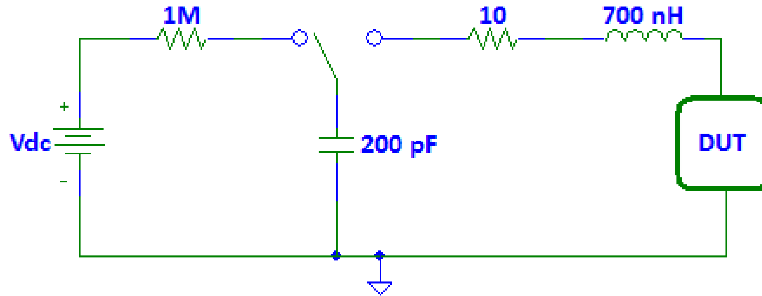

Figure 1.5 MM Equivalent Schematic [7]

DUT response to a MM event, like a CDM event, follows an LCR response as shown in Figure 1.6. However, the capacitances in this circuit are much larger, leading to a slower rise time of approximately 20 ns.

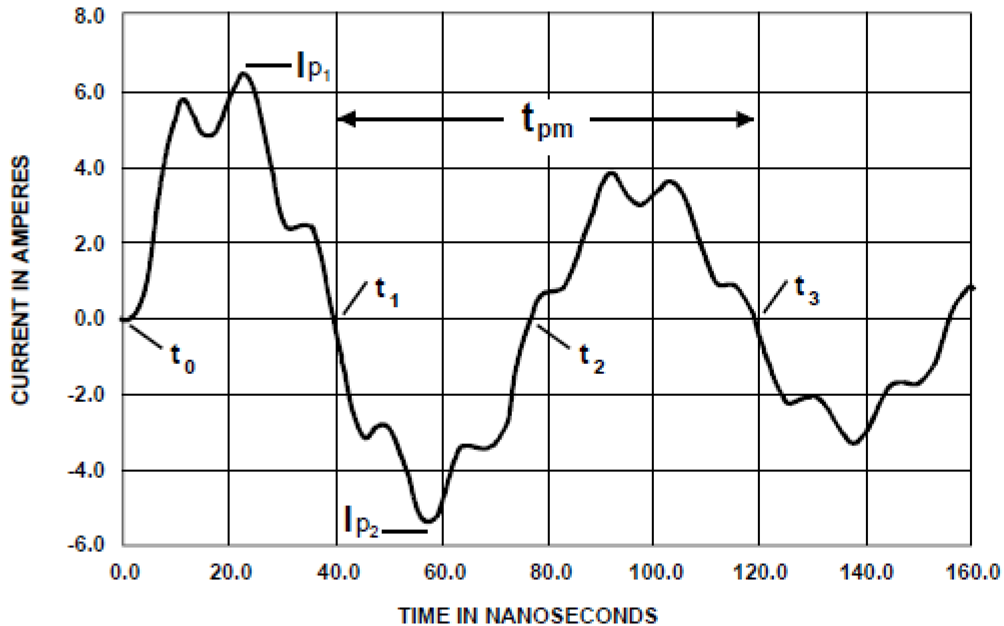

Figure 1.6 Current vs. Time for a MM Event (figure from [7])

Chapter 2 - ESD Pad Protection Techniques

2.1 Basic ESD Bond Pads

Bond pads provide the contacts between integrated circuits and the ESD-filled world outside the chip. Because they are the gateway to and from an IC, bond pads are directly in the discharge path of an ESD event. It follows, therefore, that defending against imminent electrical shock begins with placing protection circuitry in the immediate vicinity of an IC's bond pads. It is here, at the gateway, that dangerous discharging current rushing into the system must be channeled away before it can wreak havoc on critical circuitry.

In a CMOS process, two diodes provide perhaps the most basic form of ESD protection. As shown in Figure 2.1, a diode placed between an I/O pad and a Vdd pad turns on when the I/O pad rises above the supply voltage. A positively charged ESD event striking an I/O pad thus discharges back out of the chip through the positive supply line. A diode between an I/O pad and ground protects the I/O pad from negatively charged ESD events by turning on as the I/O voltage dips below ground.

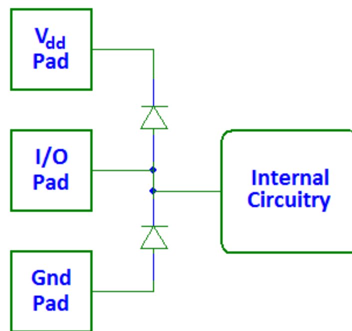

Figure 2.1 Basic ESD pad with two protection diodes

While effective in protecting against overvoltages on I/O pads, the two protection diodes do not protect against a supply line that reaches dangerous levels. For example, the supply line circuitry may not be able to absorb the event and Vdd could pulse to a dangerously high level. To solve this issue, a standard ESD pad adds a voltage clamp between the supply voltage line and ground. Figure 2.2 shows a common schematic for a complete ESD pad. If the supply line exceeds a specified voltage, the clamp turns on and shorts it to ground, protecting the internal circuitry from overvoltage. This style of clamp is typically implemented as a gate-grounded NMOS clamp [8].

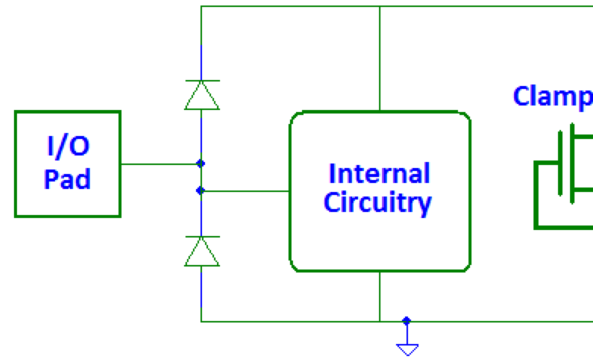

Figure 2.2 Typical ESD pad with protection diodes and clamp

2.2 Alternative ESD Protection Techniques

Concerns with any ESD protection scheme encompass several parameters. Because ESD protection circuitry plays no active role in the core function of the IC, it cannot consume too much area on the chip. Chip area is expensive and ESD protection must be economical. Another source of concern is the amount of added capacitance due to ESD protection circuitry. Additional capacitance decreases a circuit's frequency response and, depending on the function of the pad, can adversely affect both digital and analog signal performance. This section examines alternative ESD protection schemes and discusses their strengths and weaknesses.

2.2.1 ESD-Transient Triggered Clamp

Some protection circuits use an ESD-transient detection circuit to trigger the NMOS clamp transistor previously discussed. This design attempts to circumvent a basic flaw with the gate-grounded approach, which is easily understood by observing its I-V curve, shown in Figure 2.3. In a classic CMOS process, a voltage at the drain of a MOSFET operated in the saturation region can cause impact ionization. The impact ionization allows electrons to enter the drain, while pushing the holes into the substrate. The extra holes in the substrate create a voltage drop from source to substrate, creating a forward-biased junction, and completing an electron path from source to drain [9]. The voltage at which this path is created is known as the clamp's snapback voltage, marked as V_{t1} on Figure 2.3. Further snapbacks in the I-V curve occur as more conducting paths are created. As Figure 2.3 shows, the initial snapback voltage is quite high; higher than the supply voltage. Otherwise, the clamp would turn on under normal operating conditions.

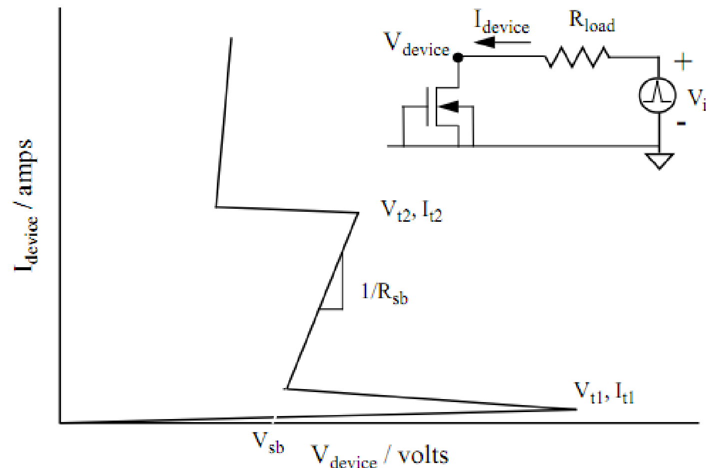

Figure 2.3 I-V plot for a gate-grounded clamp (figure from [10])

Figure 2.4 shows a basic ESD-transient detection circuit connected to the gate of an NMOS clamp to address this issue [8]. To decrease the clamp's turn on voltage, the ESD-transient triggered clamp remains off under DC conditions and only turns on when rapid changes in the supply voltage occur. Under DC operating conditions, the capacitor C is an open circuit, charging to VDD which keeps the inverter output low and the clamp off. With a sudden VDD spike, however, the capacitor becomes low impedance relative to the resistor. Voltage develops across the resistor, making V_x low relative to the spiked VDD. The voltage difference turns on M_p, pulling the inverter output high and activating the clamp. By detecting sudden changes to VDD, the ESD-transient triggered clamp can better protect minimum sized FETs [8].

There are other advantages to this approach. In contrast to the gate-grounded clamp, the NMOS clamp FET does not need to go into breakdown in order to function. Not only does this make the clamp more durable, it is easier to design. However, designing a gate-grounded clamp depends on the parameters of a process, meaning that changing to a new process requires a complete redesign of the clamp [1].

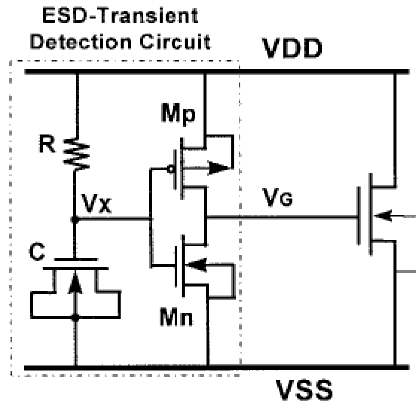

Figure 2.4 ESD-Transient Triggered Clamp (figure from [8])

The drawback of this approach is that because the triggering circuitry operates on rapid voltage changes, it does not protect against accidental DC overvoltage. An implementation of the ESD-transient triggered clamps would require additional gate-grounded clamps to protect against DC overvoltages. A well designed gate-grounded clamp, however, both protects against DC overvoltages and has the ability to turn on with enough speed to protect the IC's inner circuitry. Another drawback is the extra circuitry involved. The NMOS clamp already has to be large enough to survive high current levels. The detection circuitry, especially if it includes an exponential horn driver circuit for the NMOS clamp to improve turn-on speed, takes up even more chip real estate.

2.2.2 Resonant ESD Pad

Any ESD protection circuitry connected to a pad adds parasitic capacitance, which can decrease the circuit's frequency response. Circuits designed for operation in the gigahertz range cannot afford to lose frequency response. It is therefore important that pads connected to high frequency circuits, such as the input to an LNA, can effectively protect against ESD events as well as having a minimal effect on high frequency circuit performance. A design presented in [12] implements a resonant ESD pad at the input of an LNA to compensate for the added parasitic capacitance.

Figure 2.5 shows the design, which uses an inductor to resonate out the capacitance and a varactor for fine tuning the resonant circuit. This particular design employs a gate-grounded clamp from pad to ground. It could have just as easily used the diode protection shown in Figure 2.1.

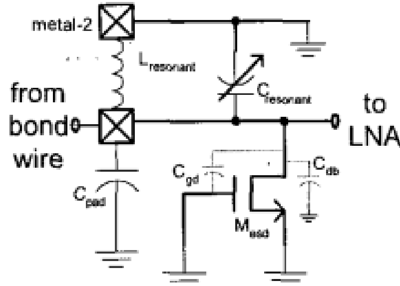

Figure 2.5 Resonant ESD Pad (figure from [12])

The designs in Figures 2.2 and 2.5 were created specifically for high frequency applications while the design in Figure 2.6 is used commonly in low frequency applications. A subtle but important distinction between Figure 2.2 and Figure 2.6 is the use of a series resistor between the pad and the inner circuitry in Figure 2.6. A high frequency ESD pad does not use a series resistor because it produces a voltage drop between the pad and the internal circuitry. With input sensitivity such an important parameter for high frequency circuits, such as an LNA circuit, removing the resistor prevents unnecessary signal loss and associated added noise.

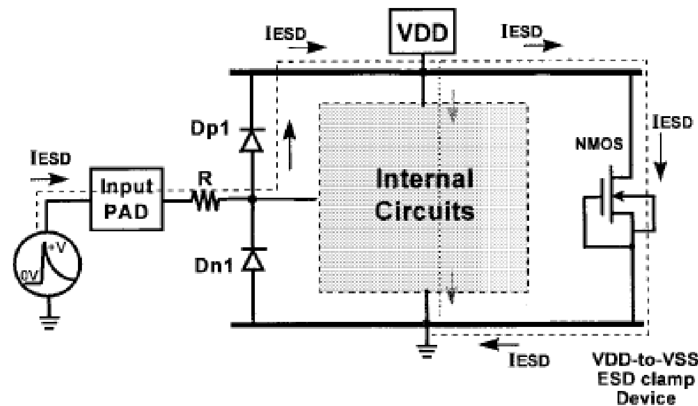

Figure 2.6 Common Low Frequency ESD Pad (adapted from a figure in [8])

There are no real drawbacks to using the resonant ESD pad protection circuit, though adding another inductor to an LNA circuit is not ideal. In practice, the LNA matching network and the resonant tank on the ESD pad should be combined to reduce the number of components needed.

Chapter 3 - ESD Pad Optimization

3.1 ESD Research Objective

One of the main goals of this research is to develop a method for detecting the occurrence of an ESD event in an integrated circuit by utilizing fuses built into the integrated circuit. Such IC fuses are designed to break when exposed to high current levels seen during an ESD event. Other ESD protection research focuses on improving the protection circuit's response to ESD events.

The combination of IC fuses and detection circuitry designed to sense a broken fuse allows for the identification of compromised ICs. This type of detection circuitry is important for companies seeking to reduce the number of returned products or for a company sending products into space. An ESD event can damage circuits in such a way that the circuit survives for several years before failing. Implementing an ESD protection scheme that includes ESD detection circuitry prevents companies from shipping products with latent defects.

While the ultimate goal is to implement an ESD detection scheme, this research must first establish an ESD pad design that protects against the three types of ESD described in Section 1.2. This section describes the process of designing an ESD pad.

3.2 ESD Protection Circuitry Simulation

The first step to establishing an effective ESD pad design is to simulate how the existing protection circuitry reacts to ESD events. Simulating these circuits in makes it easy to quickly change circuit parameters and observe how that change affects circuit performance. Simulating also verifies test circuit functionality before running an actual test that could, if designed improperly, damage components. Hence, it is helpful in minimizing the overall design cycle time.

This section establishes the first version of an ESD pad design, discusses simulation setups for each ESD type, and simulates the components of the first design, evaluating and explaining the results of each simulation.

3.2.1 Simple Protection Diode Simulations

Beginning with the ESD pad from Figure 2.1 which simply uses two protection diodes, simulations are run to obtain the protection diodes' response to each of the three ESD types. In this first design, each protection diode consists of six smaller 2 μm x 8.5 μm diodes connected in parallel.

HBM Simulation

For the HBM case, the circuit is assumed to be powered. Although it is possible for an IC to experience an HBM event when unconnected to a power supply, this exercise assumes a 2 V supply that has 3 nH of inductance and 0.2 Ω of resistance. To simplify the circuit for the simulator, parasitic inductance and resistance is included only on the power supply line and not on the ground line. The switch turns on at 1 ns, allowing the capacitor to discharge its initial 1 kV charge. Figure 3.1 shows the test circuit.

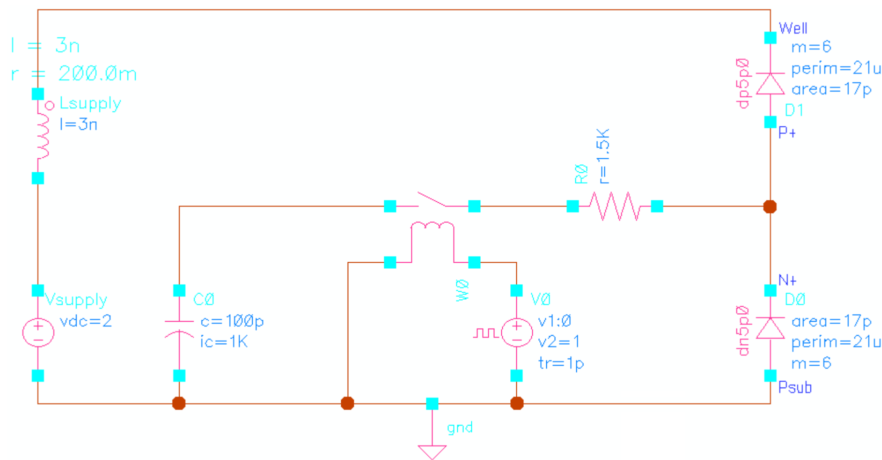

Figure 3.1 Simulating the response of protection diodes to an HBM event

Figure 3.2 shows the voltage across D0. When the ESD event occurs, D1 turns on and D0 turns off, creating a discharge path through D1, the inductor, the power supply, and then to ground. The path is essentially a series LCR circuit. Because the supply inductance resists changes in current, it is initially an open circuit that prevents the event from discharging. Instead, a 190 V pulse develops at the very node the circuit attempts to protect. A similarly large negative spike would have been seen had the simulation accounted for inductance along the ground line.

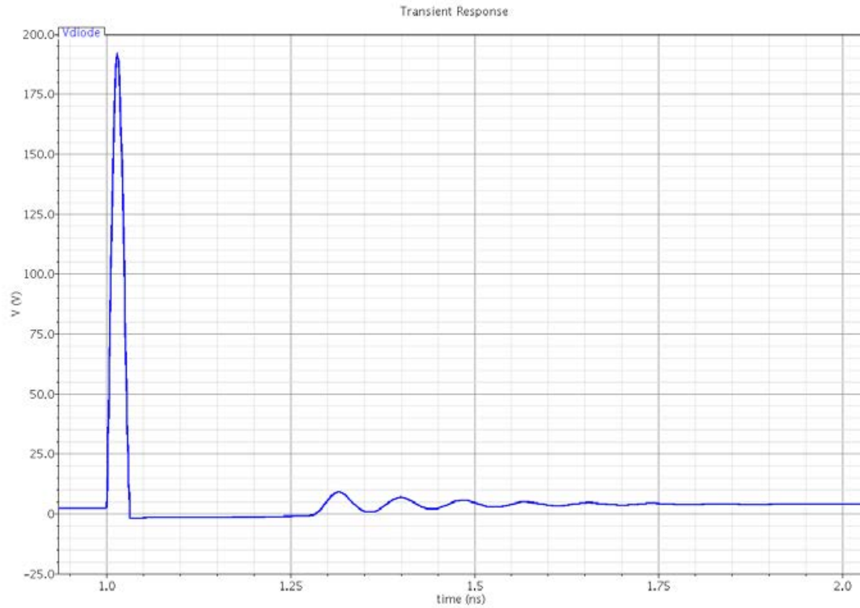

Figure 3.2 Protection diode voltage response to an HBM event

CDM Simulation

While the HBM scenario included a power supply, CDM events occur when, for example, an IC builds up charge and is subsequently discharged through a pad during bonding. If a chip experiences a CDM event, it will happen before connecting the chip to a power supply. The diode between I/O and VDD therefore remains unconnected during a CDM event. Using a combination of the simplified CDM circuit model presented in Figure 1.3 and the physical diagram shown in Figure 3.3 allows the simulation circuit shown in Figure 3.4 to be obtained.

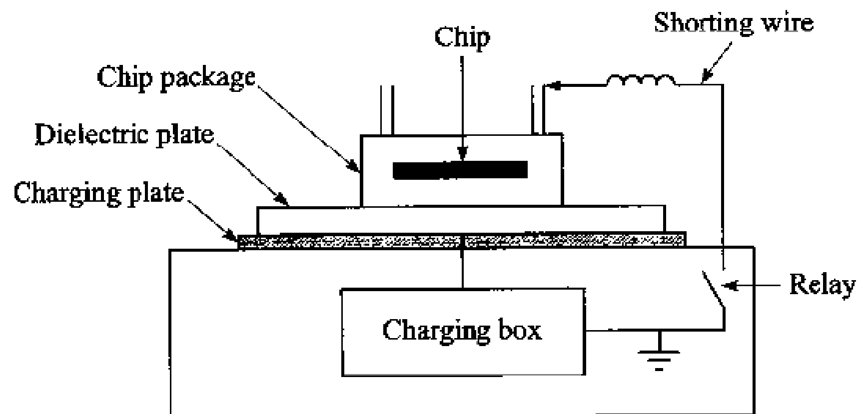

Figure 3.3 Physical model for a CDM event simulator circuit (figure from [1])

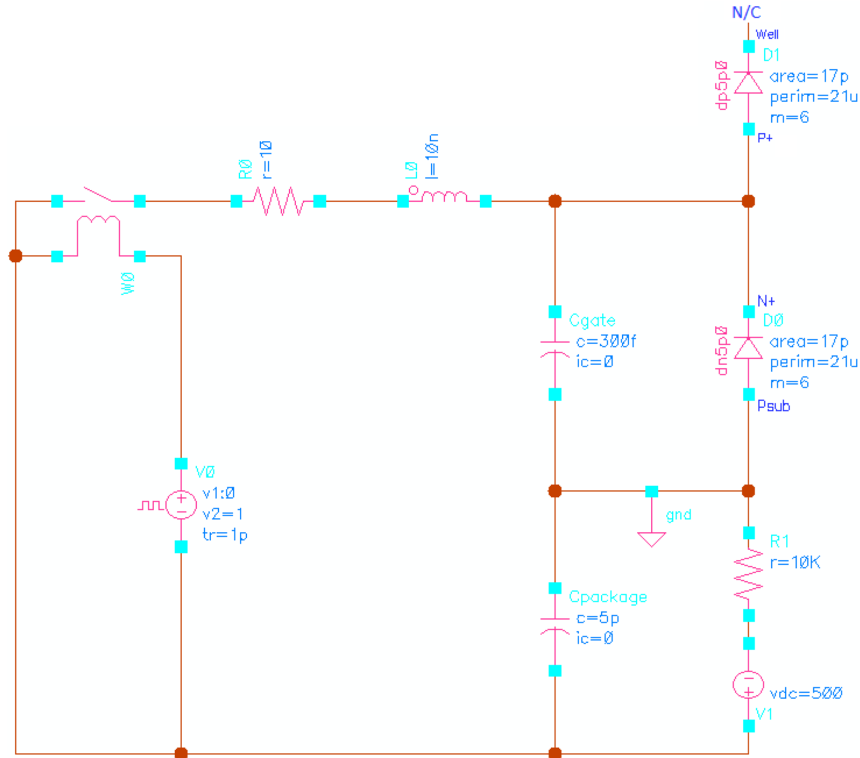

Figure 3.4 Simulating the response of protection diodes to a CDM event

The physical model in Figure 3.3 shows the chip placed into a package then placed onto a charging plate. In Figure 3.4, a 500 V DC supply with a 10 kΩ resistor simulates the charging box and the 5 pF capacitor represents the capacitance between the package and the charging plate. The 300 fF Cgate capacitor represents an at-risk MOSFET gate connected to the I/O pad at the junction of the two diodes. Note the upper protection diode left open-circuited in this simulation. This is because it may not yet be bonded and is also not interfaced to any PC board supply as it was in the HBM simulation described previously.

The circuit does not switch until 300 ns to allow Cpackage to charge to 500 V. Note that the 10 kΩ resistor value is arbitrary and sets the charging time for the simulation. Figure 3.5 shows the results. The voltage across the diode and gate experience spikes up to 900 V and settle at a constant value near 500 V.

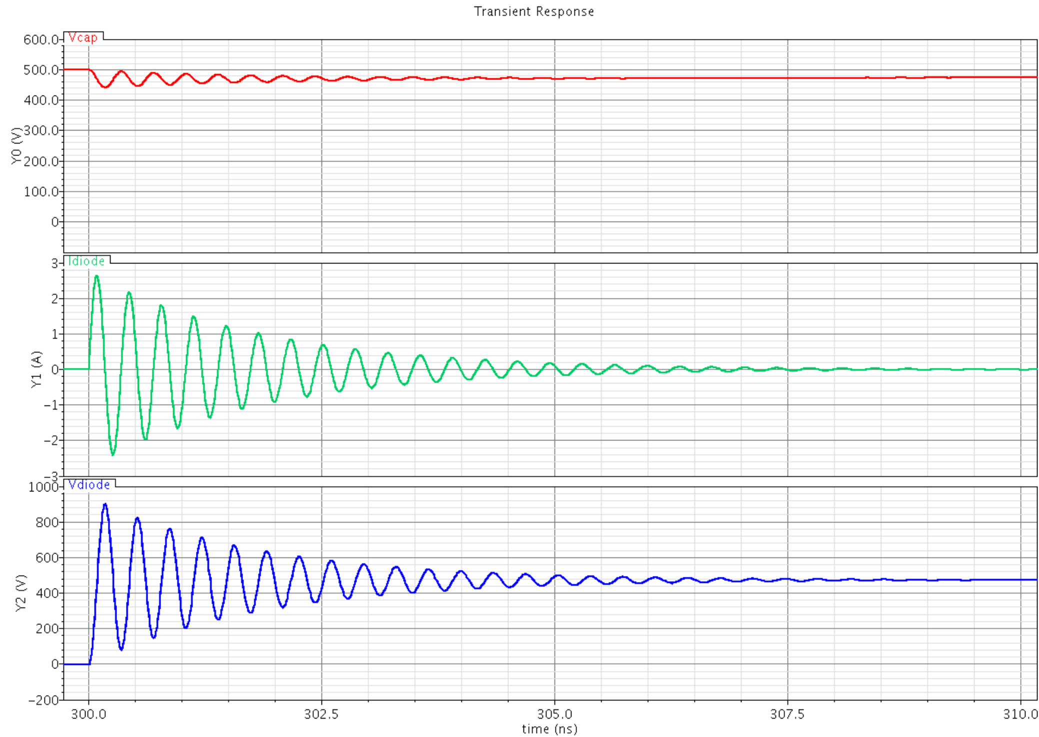

Figure 3.5 Transient response for Figure 3.4. Top to bottom: voltage on the 5 pF capacitor, diode current, and voltage at the I/O pad

Whereas the HBM scenario had a path through the power supply to ground, the lack of a discharge path to ground allows charge to accumulate at the I/O pad, supposedly staying there until another conductor touches that pad. In reality this charge does not simply bounce between nodes during a CDM event with no damage done to the circuit. Rather, a CDM event occurs because the IC package has come into contact with a ground conductor. Any charge accumulated at the I/O pad will find its way to ground. In this case, it discharges through the diode connected to the VDD line, through the internal circuitry, and then to ground. As shown in Figure 3.6, this discharge path entirely defeats the purpose of having protection circuitry.

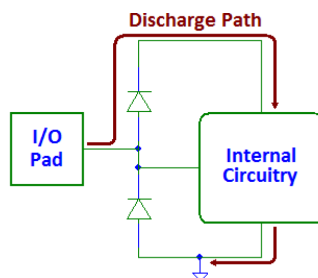

Figure 3.6 Discharge path for an unpowered circuit

MM Simulation

A simple diode-only ESD circuit struck with an MM event experiences a similar problem. When handled by a machine such as a wire bonder, the IC remains unconnected to a power supply. As in the CDM scenario, only the diode between I/O and ground remains in the simulation circuit, shown in Figure 3.7. The capacitor has an initial charge of 100 V which discharges when the switch closes at 1 ns.

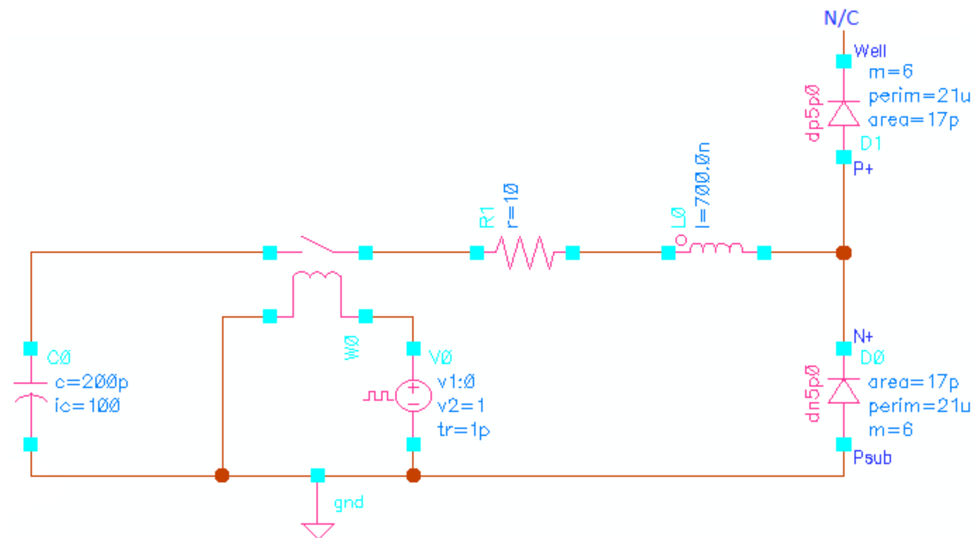

Figure 3.7 Simulating the response of protection diodes to an MM event

The results shown in Figure 3.8 reinforce the idea that protection diodes by themselves are not enough to protect the internal circuitry from a CDM or MM type event. Because there is no supply to provide a discharge path, the event once again discharges through the internal circuitry.

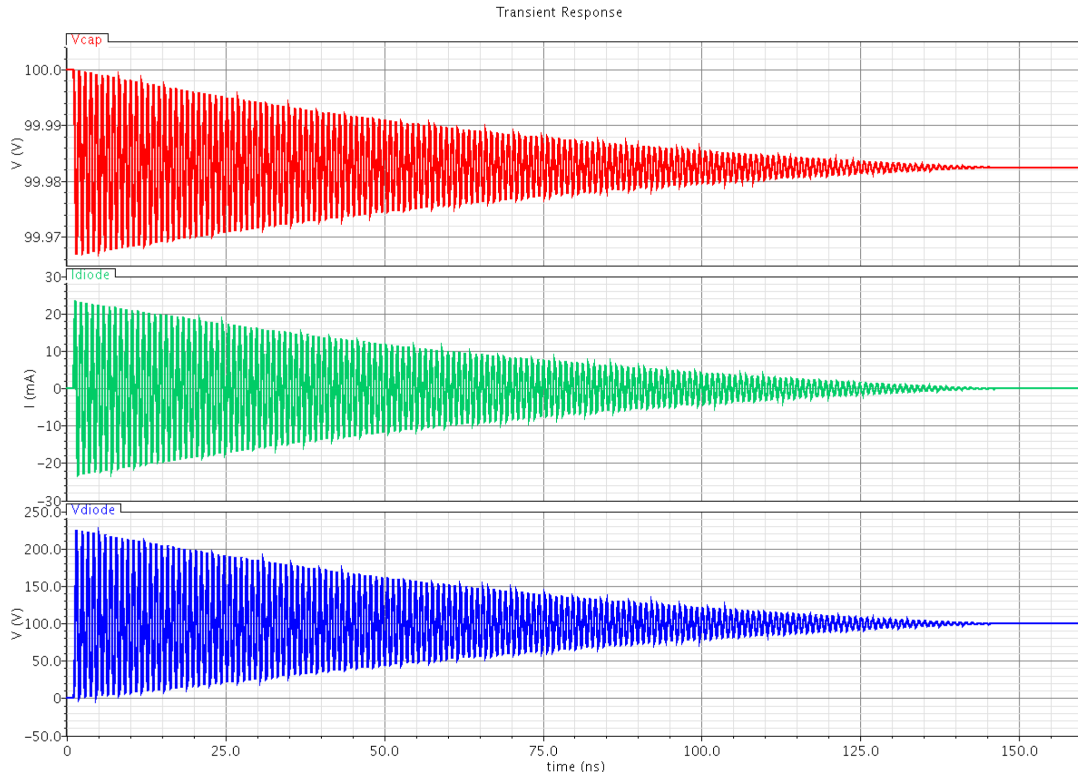

Figure 3.8 Transient response for Figure 3.7. Top to bottom: voltage on the 200 pF capacitor, diode current, and voltage at the I/O pad.

3.2.2 Voltage Clamp Simulations

Voltage clamps provide the necessary connection between VDD and ground missing in a simple protection diode scheme. Even when not connected to a power supply, a voltage clamp offers a discharge path to ground capable of handling the high currents associated with ESD events.

The first voltage clamp design is shown in Figure 3.9. This circuit is design to closely match the performance of the clamp used throughout the clamp measurements in Section 5.2. This measurement clamp was fabricated previously and its design values are unavailable, requiring a redesign. While the primary goal was to simply match performance, two main clamp design guidelines were followed. M0 needs to be very large in order to handle the large currents discharged by an ESD event. M1 is always on because its gate is always at VDD potential. It therefore needs to have a high impedance to allow M0 to turn on when M2 turns on. Hence it has an extremely low width-to-length ratio.

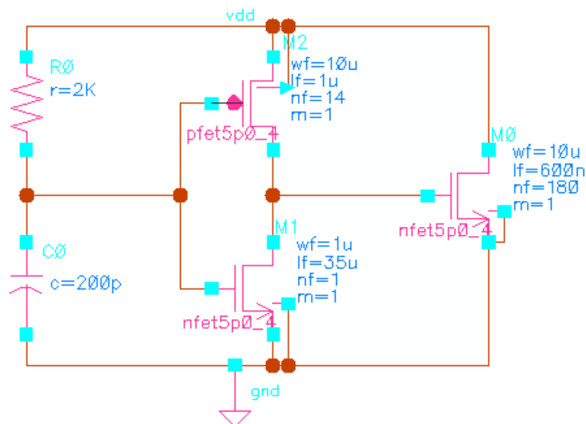

Figure 3.9 First voltage clamp design used for simulations

HBM Simulation

The ESD simulations were performed again, but this time the voltage clamp becomes the DUT. Figure 3.10 shows the HBM test circuit with results shown in Figures 3.11 and 3.12. Due to the small capacitance of the clamp relative to C1, the pulse rises much faster than the 10 ns quoted in section 1.2.1. A real circuit contains more capacitances that will significantly decrease the rise time. However, the fast rise time reveals the limits of the clamp. After a sharp rise up to 8 V, the clamp becomes effective 400 ps after the switch closes, clamping at 4 V.

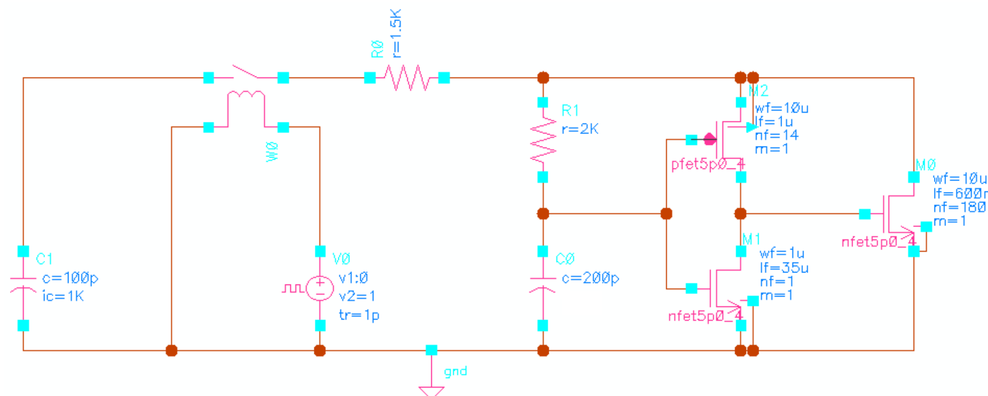

Figure 3.10 Simulating the HBM event response of a clamp

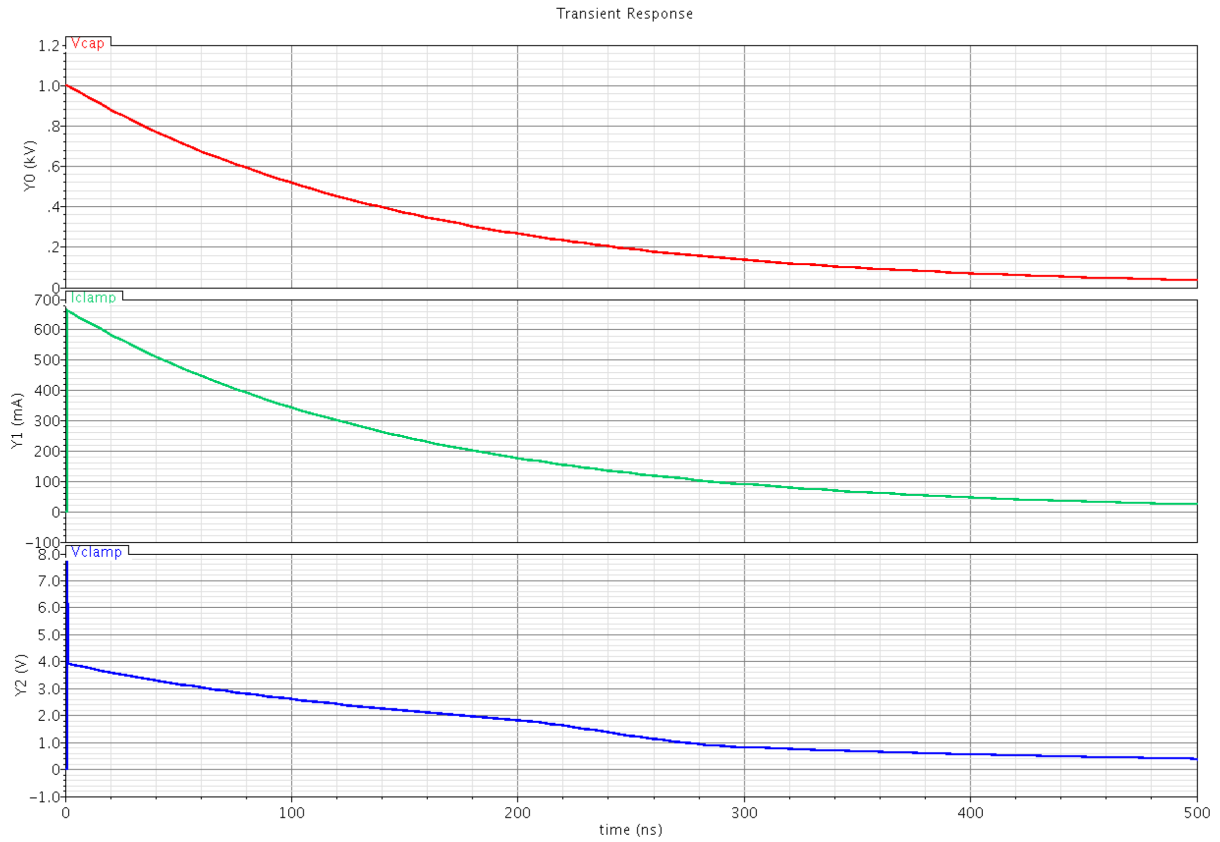

Figure 3.11 Transient response for Figure 3.10. Top to bottom: voltage on the 100 pF capacitor, clamp current, and clamp voltage.

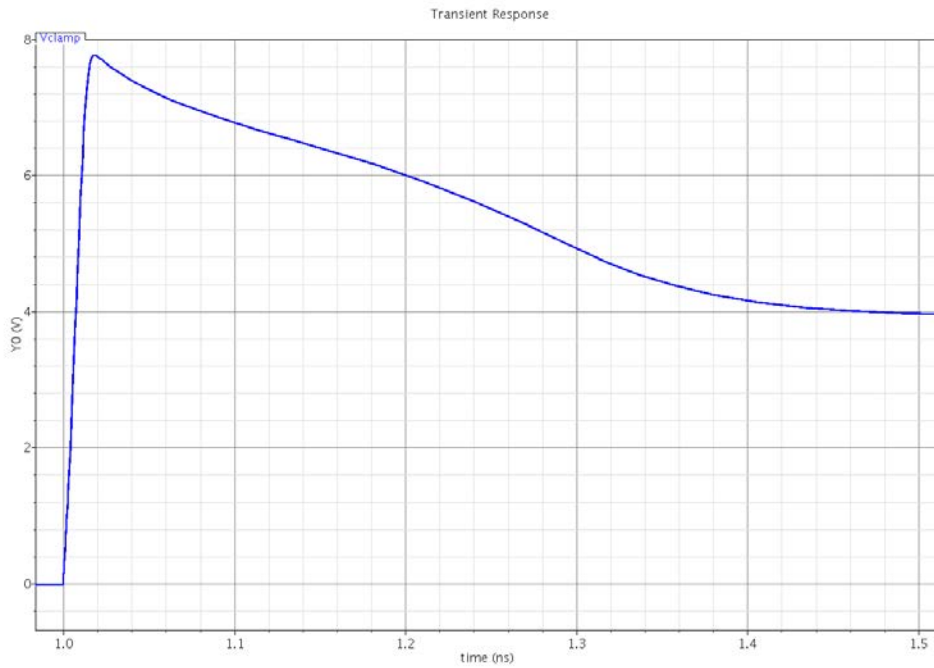

Figure 3.12 Voltage spike across the clamp as it receives the ESD event

CDM Simulation

Previously, with a reverse-biased diode between ground and the I/O pad, the circuit in Figure 3.4 was unable to discharge the voltage on that node to ground. The clamp in Figure 3.13 does not have this problem and the results in Figure 3.14 display the clamp's ability to effectively minimize the effect of the CDM event. The pad sees a maximum 10 V pulse for approximately 380 ps.

For a general ESD event, it is unknown whether the device has a positive or negative charge relative to the grounded conductor that triggers the event. It is therefore important to test this scenario with both a positive and negatively charged capacitor. Figure 3.15 shows the response for a negatively charged capacitor. The polarity of the capacitor makes little difference to the transient response. The major difference is that the maximum voltage seen by the pad is less for the negatively charged capacitor because the largest pulse swings negative. For negative swings, the clamp still operates, but the drains of the FETs become sources and the sources become drains. In this configuration, M0 and M2 act like cascaded source follower amplifiers. The negative voltage needed to turn on these two FETs is equal to two threshold voltage drops. The plots below reflect this; the voltage needs only to reach approximately -1 V to activate the clamp.

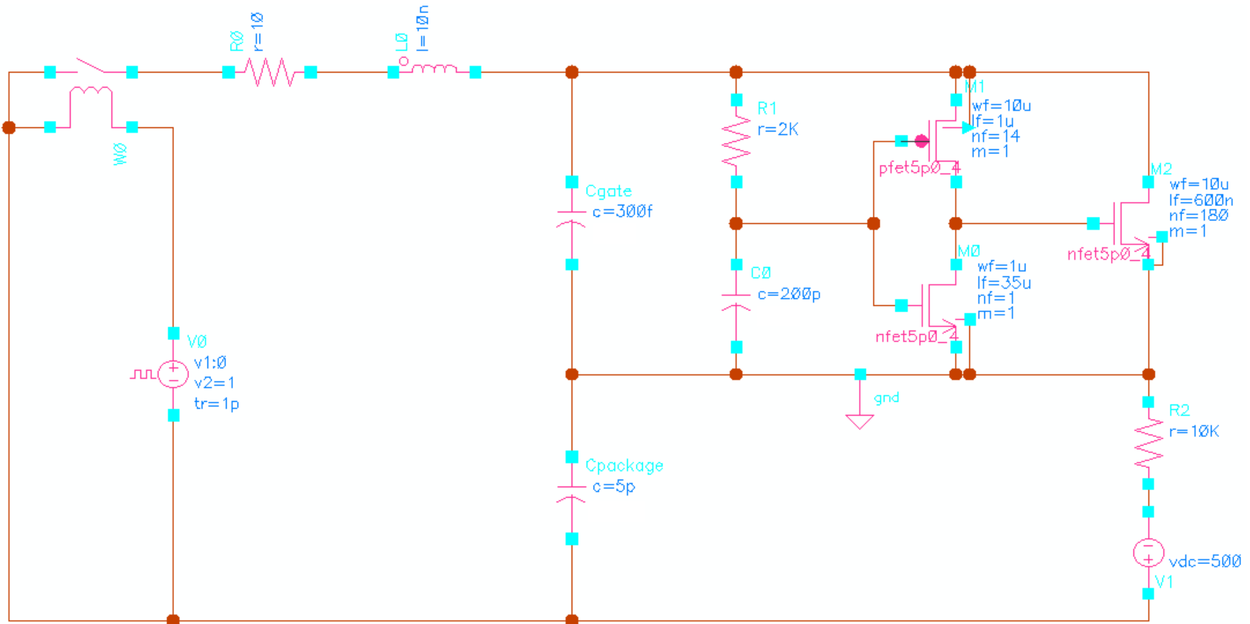

Figure 3.13 Simulating the CDM event response of a clamp

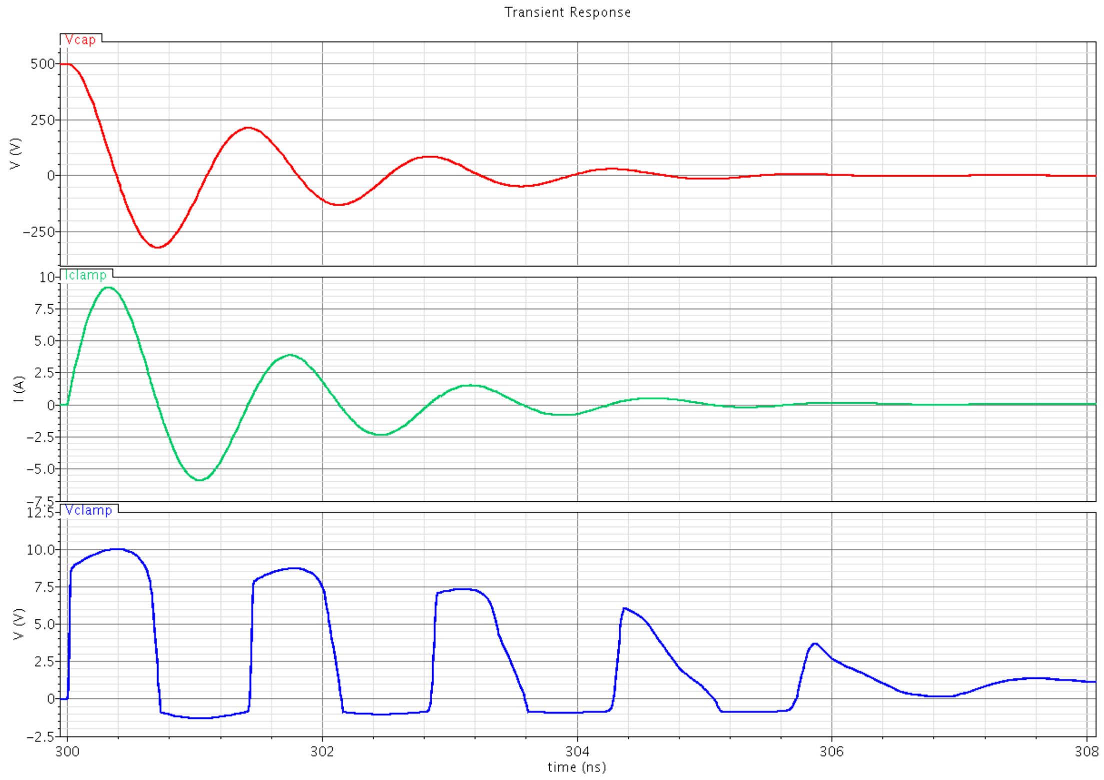

Figure 3.14 Transient response for Figure 3.13.

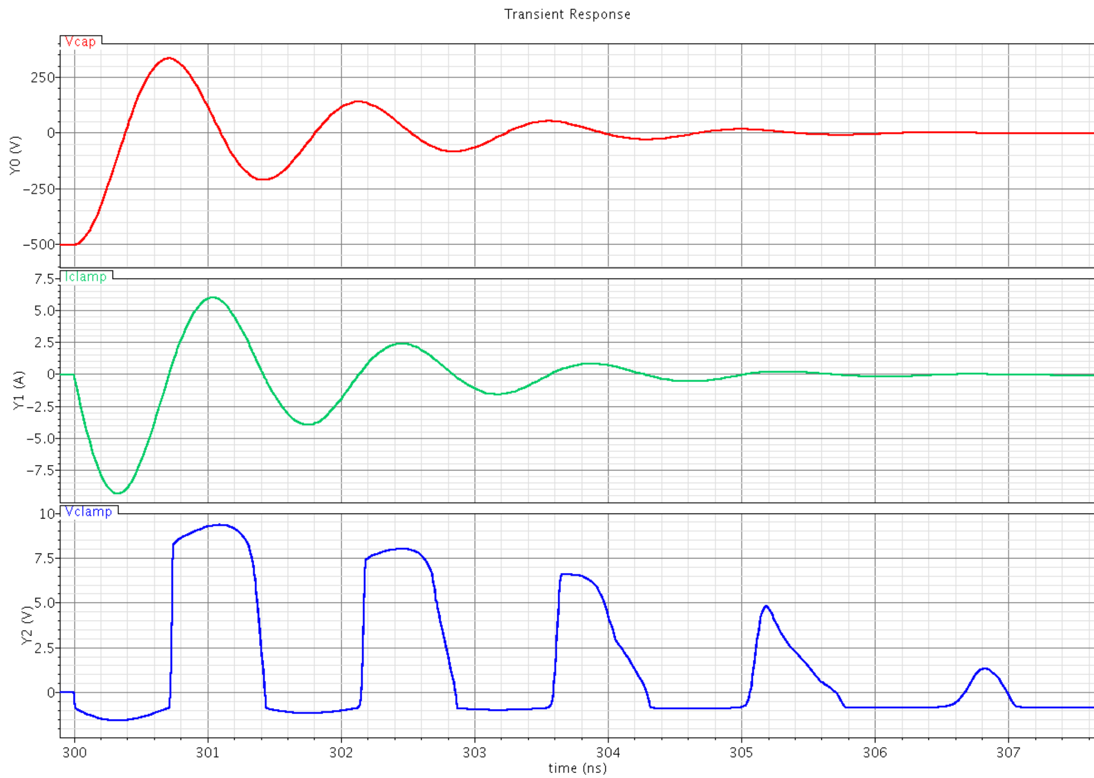

Figure 3.15 Transient response for a negatively charged Cpackage in Figure 3.13

MM Simulation

MM and CDM events both behave as LCR circuits. The simulation results for each therefore produce similar results. The primary differences between the two are the voltage and current levels as well as the frequency of oscillation. An MM event is at a lower voltage and current level, but its lower frequency of oscillation results in longer pulses. With longer pulses, the circuit, while not reaching CDM levels of current, is stressed for longer periods of time. In these simulations, the clamp remains on 50 times longer than for a CDM event yet the voltage seen by the pad is only 3.5 V less.

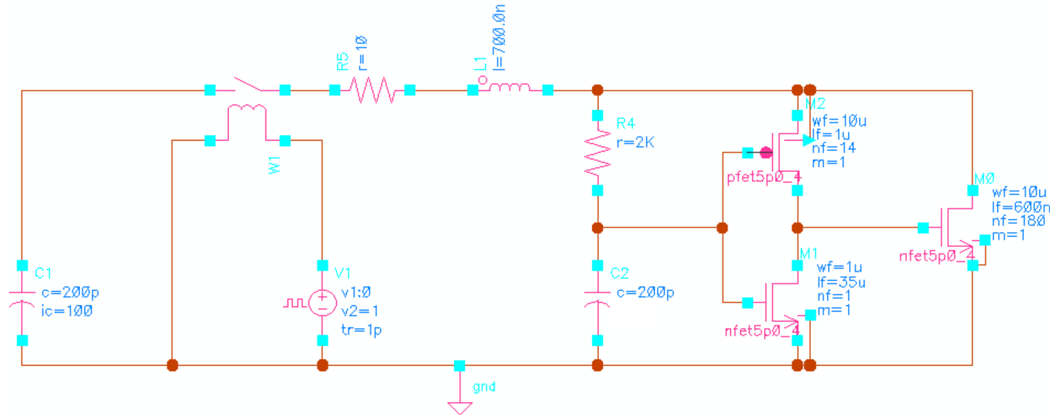

Figure 3.16 Simulating the MM event response of a clamp

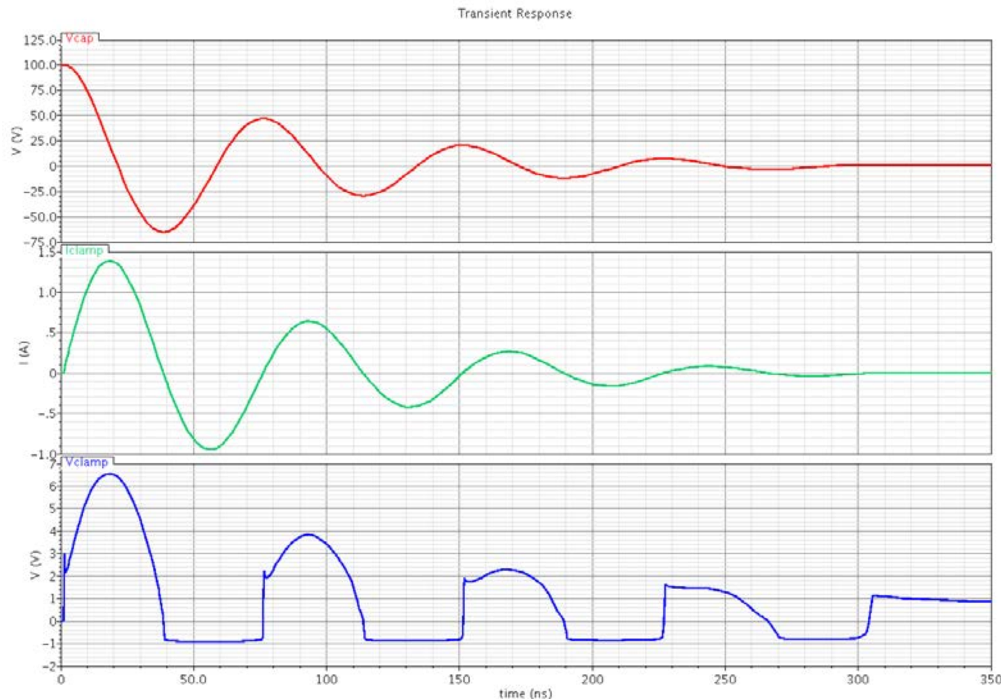

Figure 3.17 Transient response for Figure 3.16

3.2.3 ESD Pad Simulations

As discussed in Section 2.1, combining a voltage clamp with protection diodes offers protection for any pad, be it a VDD, ground, or I/O pad. The following simulations show that adding a voltage clamp between VDD and ground not only protects against events occurring at a VDD pad, but also protects the I/O pad from ESD events. Even if the chip is unconnected from a power supply, as in the CDM and MM scenarios, the clamp remains a safe discharge path for an ESD event. Figure 3.18 shows how the event discharges through the clamp instead of the sensitive internal circuitry.

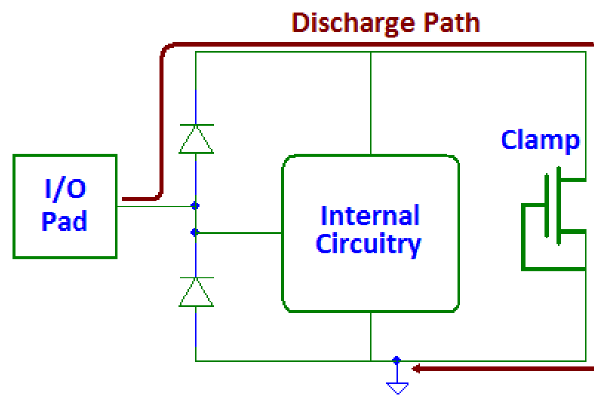

Figure 3.18 A clamp offers protection to a circuit unconnected to a power supply

Combining the clamp with the protection diodes should dramatically improve the performance over the pads simulated in Section 3.2.1. Figure 3.19 shows the preliminary ESD pad design placed in an HBM simulation circuit. A few rudimentary goals were in place for the first ESD pad design. Besides matching the performance of the measurement clamp, the primary goal for the first design was simple: ensure the clamp can flow a large amount of current by using a very large NFET. Due to the large area of the clamp, the goal when sizing the diodes was to keep them as small as possible to minimize the amount of valuable chip area consumed by ESD protection circuitry.

HBM Simulation

The pad's performance in an HBM simulation is shown in Figure 3.20. These results are in stark contrast to those presented in Figure 3.2 where the pad voltage spiked to 190 V while the inductor charged. Then LC components created oscillations that produced pulses as high as 10 V. With the clamp-enhanced ESD pad, the power supply line still provides a discharge path, but the clamp is now available to absorb the initial pulse while the inductor charges and dampen any oscillations due to LC components. The pad now has a spike of just 10.5 V. This is higher than the clamp-only spike seen in Figures 3.11 and 3.12, due to the additional voltage drop across D1.

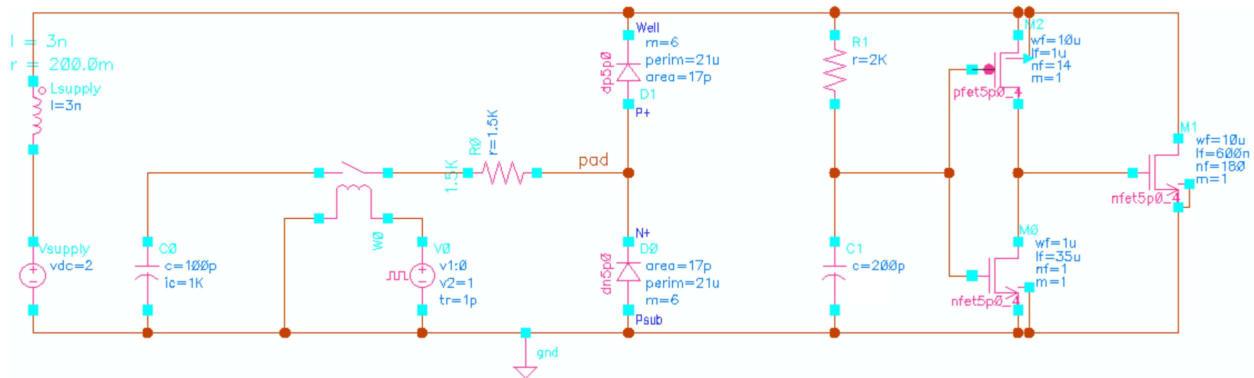

Figure 3.19 Simulating the HBM event response of an ESD pad

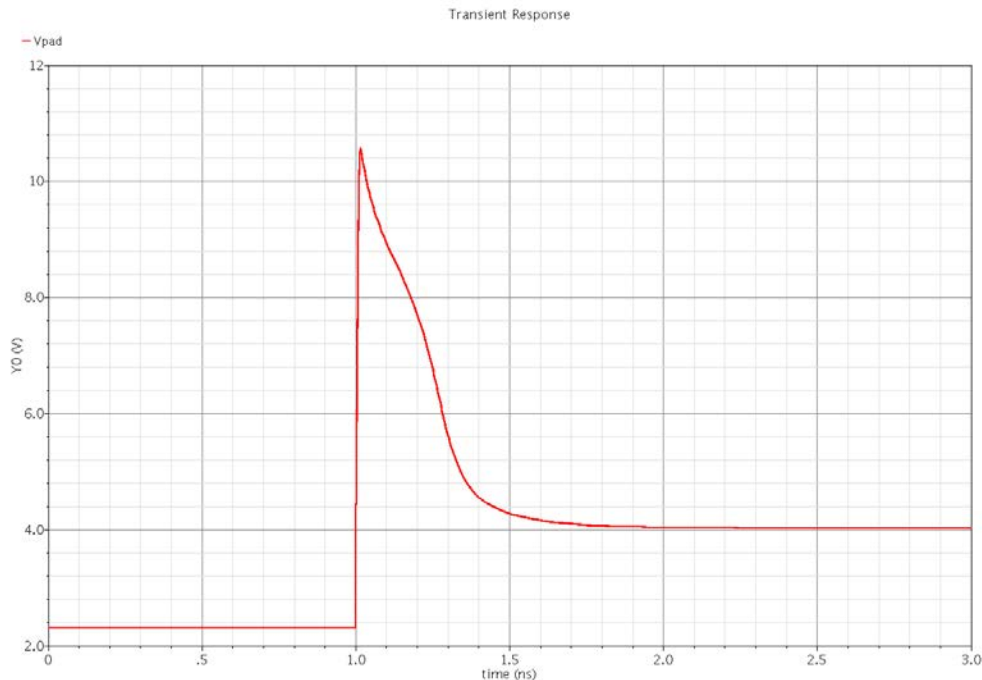

Figure 3.20 Transient response for Figure 3.19

CDM Simulation

Once again, neither a CDM nor MM event occurs with a power supply connected, meaning the protection circuitry relies solely on the clamp to discharge overvoltages on the VDD line to ground. In contrast to the circuit in Figure 3.4 containing a single protection diode, the ESD pad shown in Figure 3.21 has a protection diode in series with a voltage clamp to discharge events occurring on the I/O pad. The result in Figure 3.22 is that the protection circuitry has the ability to drive the voltage towards zero which helps prevent damage to the internal circuitry. The 24 V maximum pad voltage remains a concern, but as discussed later in Section 3.3.1, its short duration mitigates the stress placed on the I/O pad.

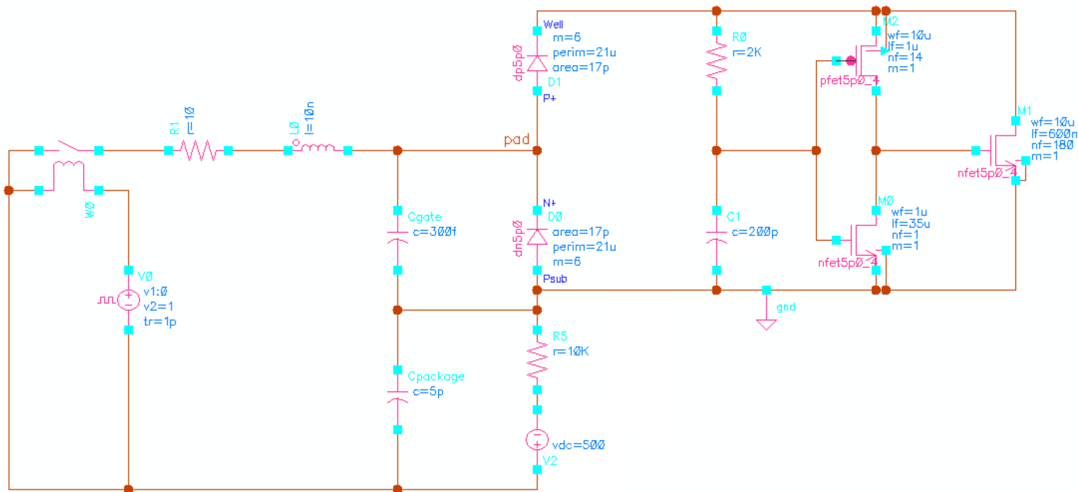

Figure 3.21 Simulating the CDM event response of an ESD pad

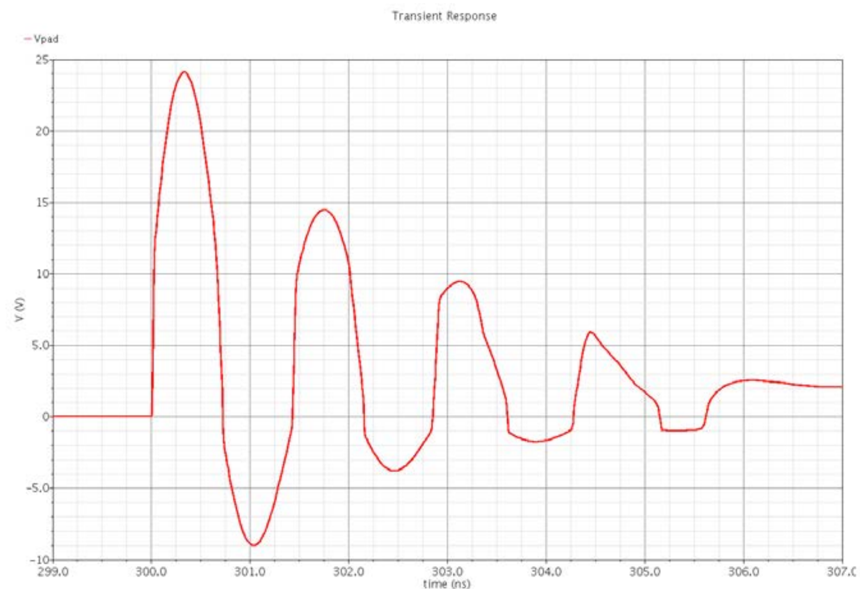

Figure 3.22 Transient response for Figure 3.21

MM Simulation

The MM event simulation circuit and resulting plot are shown below in Figures 3.23 and 3.24, respectively. Here, the voltage is limited to a maximum of 9.5 V. The 24 V pulse for 1.4 ns seen in the CDM case and the 9.5 V pulse for 40 ns seen here are dramatic improvements over the ESD pads using protection diodes, but the results – especially the 24 V seen in the CDM simulation – are less than desirable. The next section analyzes different ways to improve this design.

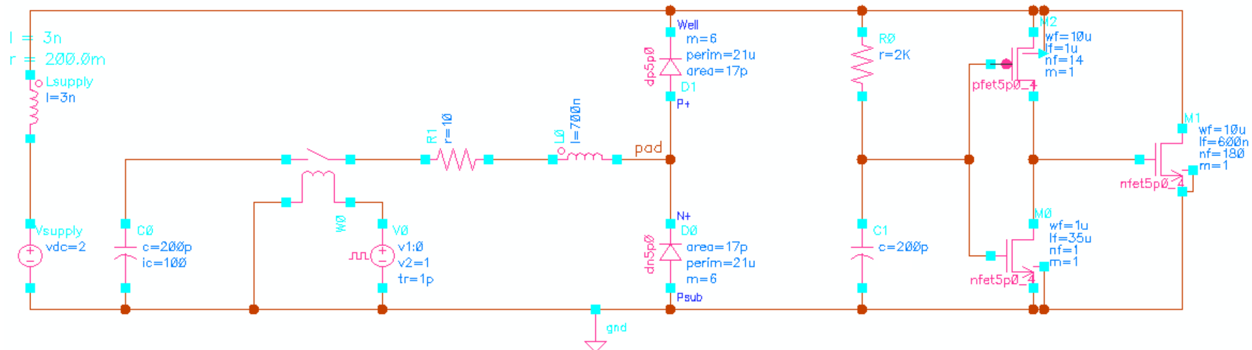

Figure 3.23 Simulating the MM event response of an ESD pad

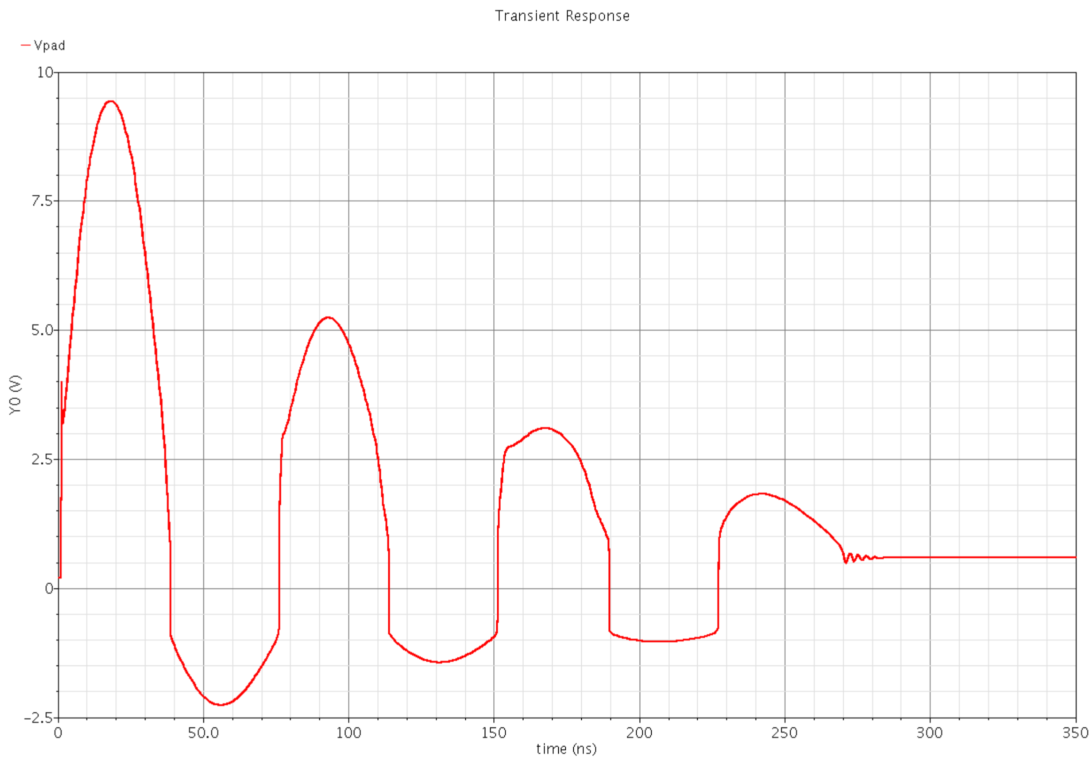

Figure 3.24 Transient response for Figure 3.23

3.3 Optimization

The previous section concludes that while the design presented in Section 3.2.3 provides substantial improvement over the protection diode scheme in Section 3.2.1, it does not provide an acceptable amount of protection. This section establishes a standard level of protection that the design must meet in order to qualify as acceptable. This standard is then used as a basis for evaluating the performance of the ESD pads.

3.3.1 Time-Dependent Dielectric Breakdown

A useful method for establishing a working standard is to use a time-dependent dielectric breakdown (TDDB) plot. TDDB is a measure of voltage tolerance versus time for a specific gate oxide thickness. The plots are made by applying an array of voltages across a gate oxide and measuring the time to breakdown for each voltage level. The plot shown in Figure 3.25 plots the TDDB for several gate oxide thicknesses. The 5.2 nm plot is of special importance because it is closest to the gate oxide thickness of the process used in this research. The TDDB points were determined by the Weibull distribution, where $T_{63\%}$ represents the time when 63.2% of the samples have failed [13]. Best-fit lines were then estimated down to a stress time of 1 ns. For the 5.2 nm gate oxide, the paper estimates it can survive a 14 V pulse for 1 ns. Using the 5.2 nm line as a guide, this research establishes a slightly lower stress voltage limit of 13 V when designing the new ESD pad design.

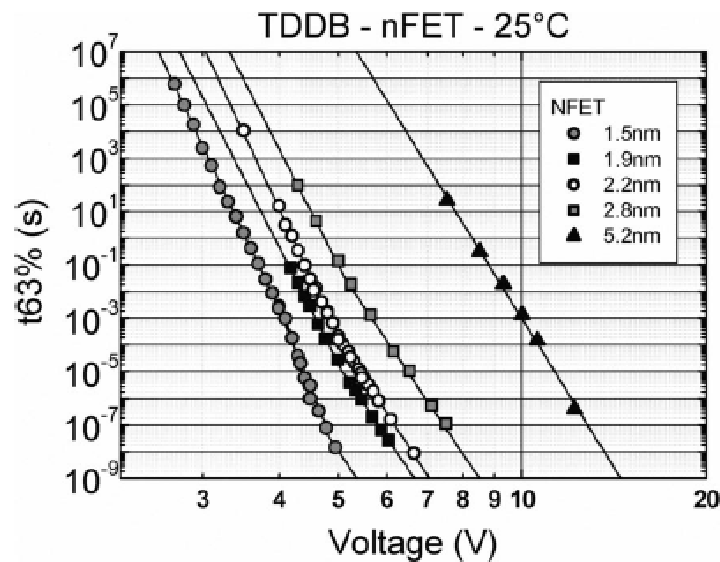

Figure 3.25 TDDB for gate oxide thicknesses ranging from 1.5 nm to 5.2 nm (figure from [12])

3.3.2 Protection Diode Optimization

The only difference between the discharge path for the ESD pad in Section 3.2.3 and that of the voltage clamp in Section 3.2.2 is the extra voltage drop across the protection diode between I/O and VDD. For the first pulse in the ESD pad CDM simulation (Figure 3.22), the diode accounts for an alarming 14 of the 24 V seen at the I/O pad. This section examines how to reduce the diode voltage by increasing the size of the diodes.

As Figures 3.26, 3.27, and 3.28 demonstrate, increasing the size of the protection diodes yields better performance by the ESD pad. The maximum voltage drop seen by the pad decreased in each of the three scenarios as the diode size was doubled and then tripled. For the CDM scenario in Figure 3.27, the maximum pad voltage decreased from 24 V using the 1x diodes to 15 V using the 3x diodes.

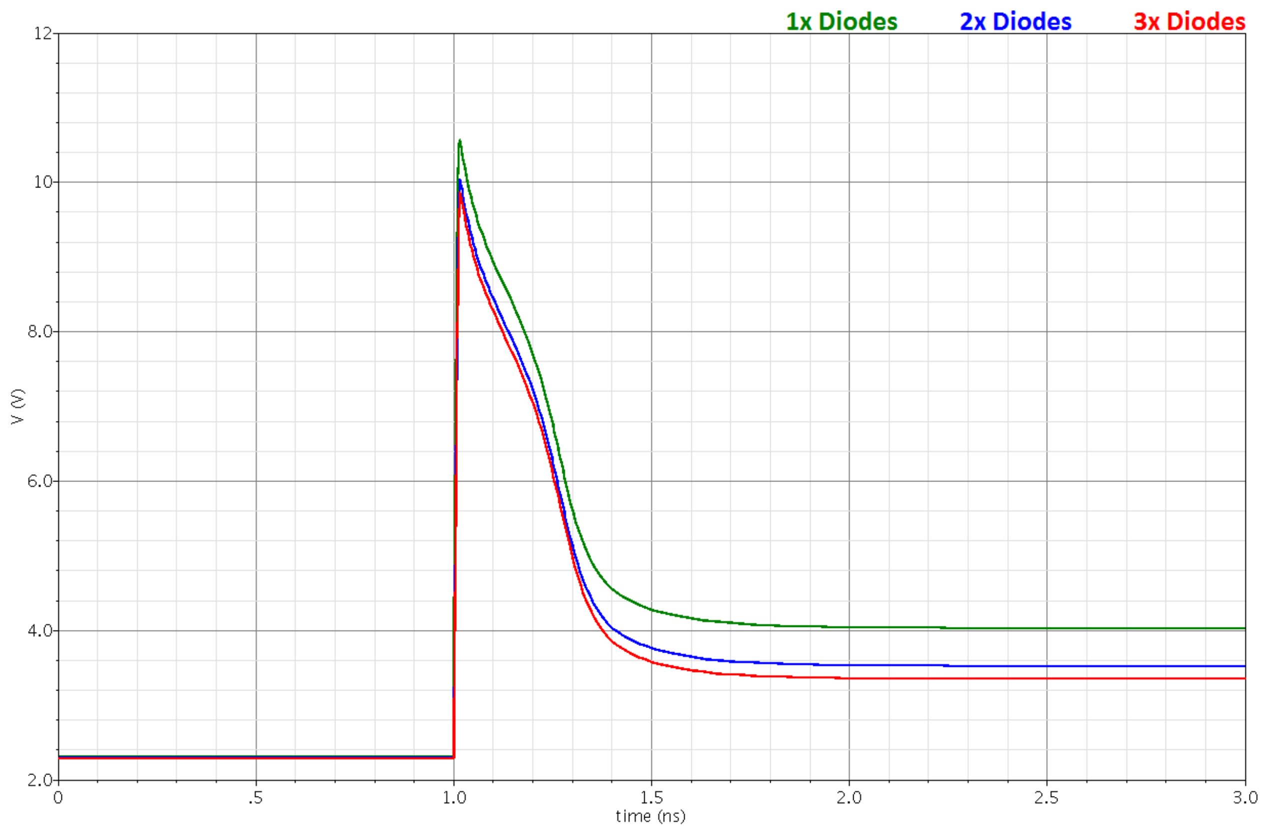

Figure 3.26 Comparison of ESD pad HBM performance, varying protection diode size

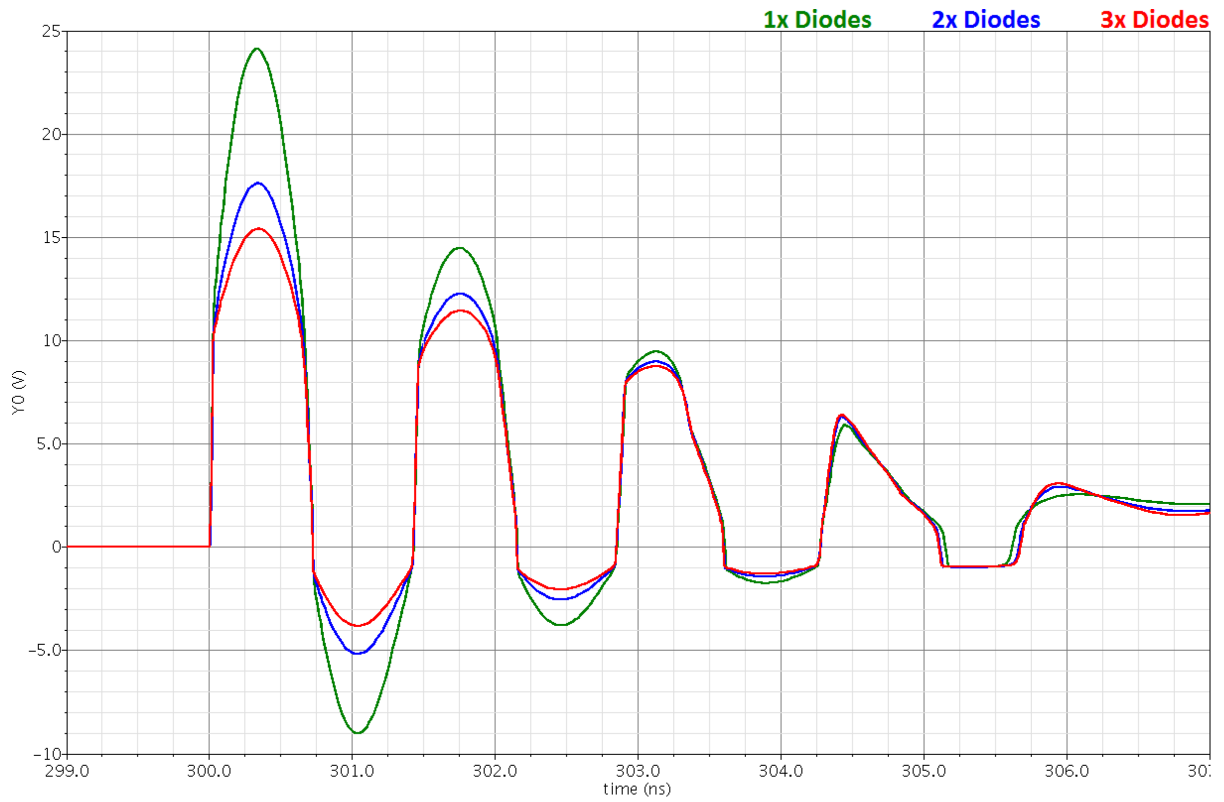

Figure 3.27 Comparison of ESD pad CDM performance, varying protection diode size

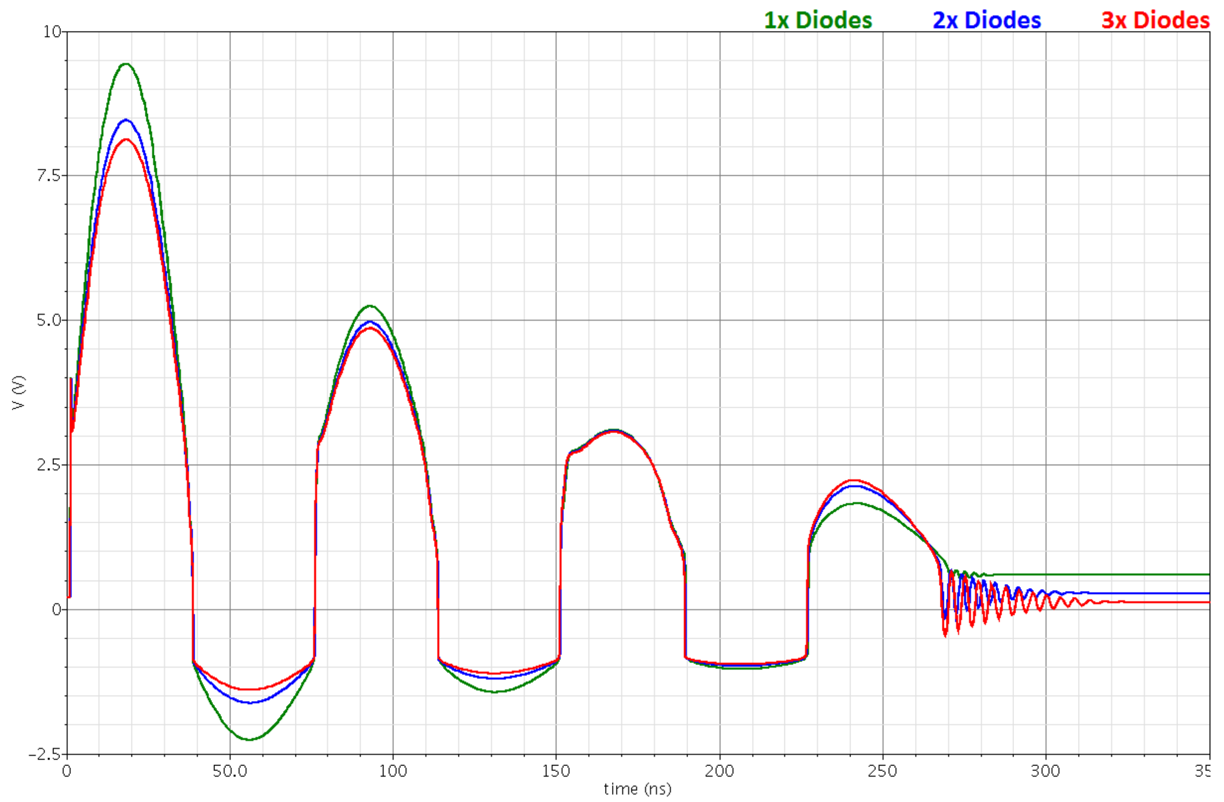

Figure 3.28 Comparison of ESD pad MM performance, varying protection diode size

The 15 V seen in the CDM simulation using the 3x diodes still does not meet the 13 V limit on stress voltage. However, further increases in diode size produce progressively smaller voltage drops. To drop the voltage from 15 V to 13 V requires a 150% increase in the size of the 3x diodes. The relatively small performance increase provided by these diodes would not justify the chip area and extra parasitic capacitance they require. The 3x diodes represent a compromise between performance and chip area. Using similarly sized diodes, the new pad design can still qualify for a reasonably high CDM classification.

Neither the HBM nor the MM scenarios were likely to cause failures using the small diode. Even with little risk of failure, increasing the size of the diodes still benefits the IC by placing lower stress levels on any devices connected to the I/O pad. Furthermore, more robust ESD protection qualifies the IC for higher HBM and MM ESD classifications.

3.3.3 Chip Area Considerations

From the simulations performed in this section, it is clear the new pad design needs larger protection diodes capable of passing large amounts of current. The 3x diode design consists of 18 parallel 2 µm x 8.5 µm diodes. For the new design, the number of parallel diodes is increased to 80 while the dimensions of each diode are reduced to 2 µm x 2 µm. A decrease in diode dimensions with an increase in the number of parallel diodes effectively increases the total junction perimeter from 378 µm to 640 µm. Die area, meanwhile, increases from 674 μm^2 to 818 μm^2. Put differently, a 21% increase in die area yields a 69% increase in junction area. With greater junction area, the diode junction resistance is lower, which should allow it to handle the higher currents associated with an ESD event.

To determine the relationship between junction area and junction resistance, the test circuit in Figure 3.29 was constructed. Because junction depth is a constant process parameter, the junction area is varied by adjusting each diode's total junction perimeter while keeping total diode sizes equal. The three perimeters chosen for this simulation are 160 µm, 320 µm, and the proposed diode's 640 µm. The simulation varies the DC source while plotting the voltage across each diode. As shown in the result in Figure 3.30, the diode with a junction perimeter of 640 µm has the lowest voltage across it, though the difference between the three is insignificant.

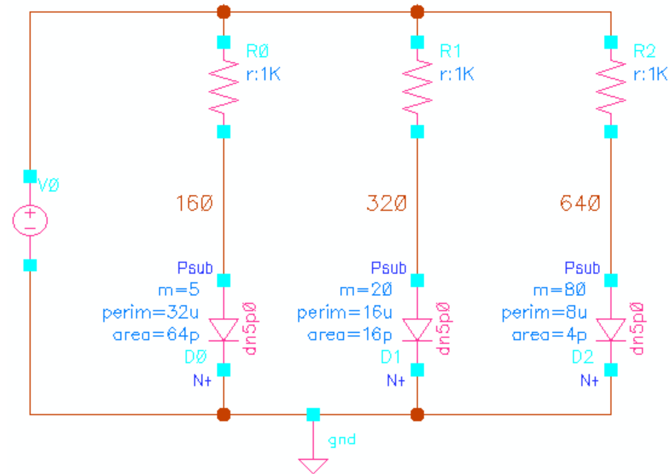

Figure 3.29 Test circuit to compare different diode perimeters

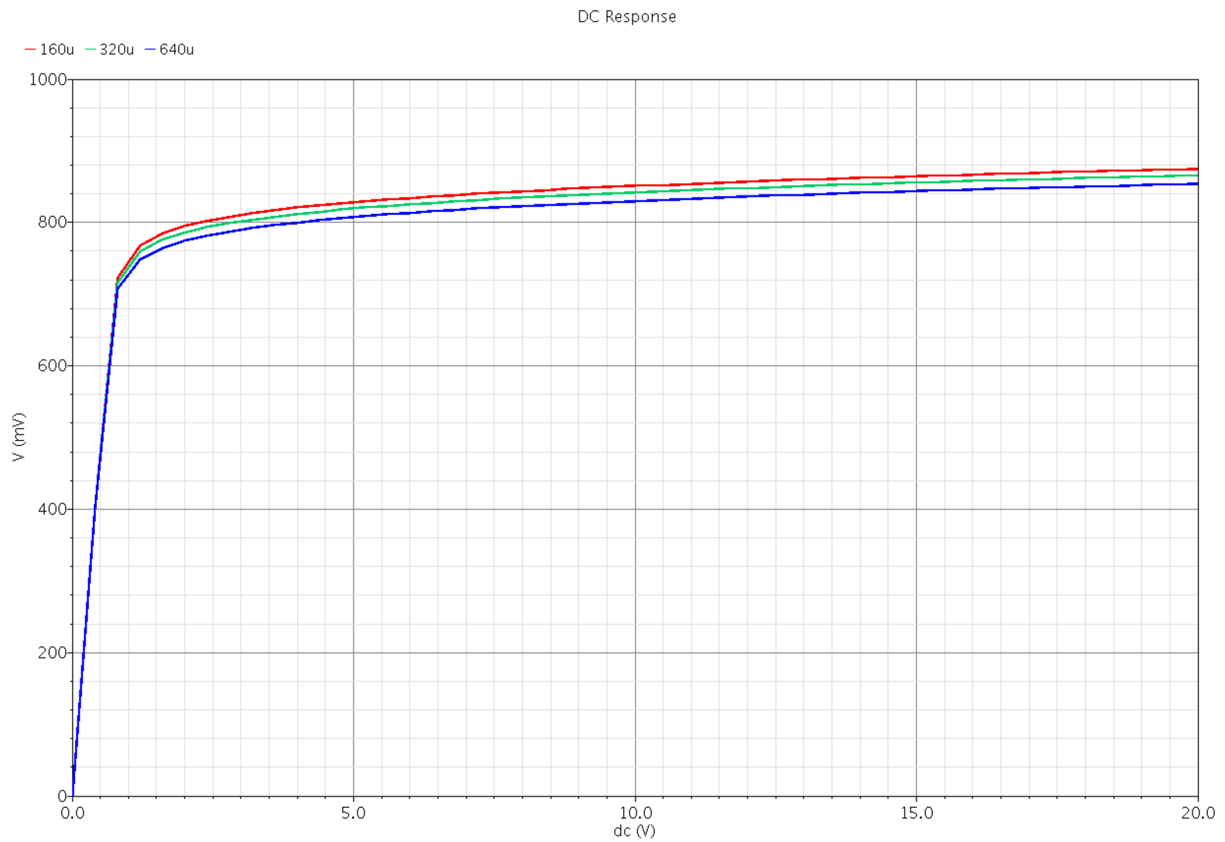

Figure 3.30 Voltage across a diode as junction perimeter is varied

A performance comparison of an ESD pad using the proposed diodes to an ESD pad using the 3x diodes is then made in Figure 3.31. Using the proposed diodes, the ESD pad displays slightly improved performance against a CDM event with the peak voltage dropping 300 mV from 15.65 V to 15.35 V. Subtracting the clamp voltage peak of 10 V seen in Figure 3.14 from the two plots in this simulation, the 300 mV drop represents a 5% decrease in peak voltage due to the diode. The performance increase is very small; a 21% increase in die area may not justify a 5% decrease in maximum voltage.

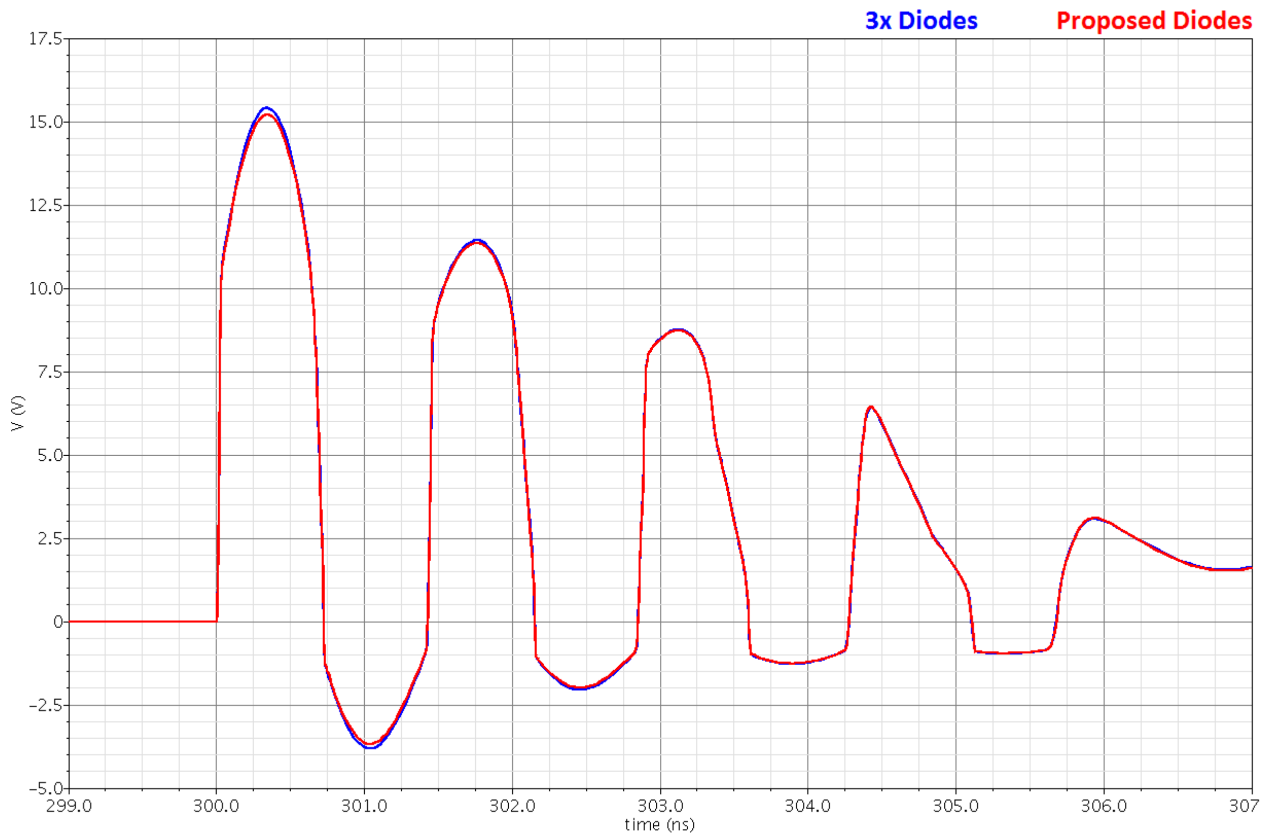

Figure 3.31 Comparison of ESD pad CDM performance using the 3x diodes design or the proposed diode design

3.3.4 Diode Parasitic Capacitance Considerations

An important consideration when sizing protection diodes is accounting for their parasitic capacitance. Careful consideration of diode size is especially crucial when designing ESD pads for RF applications, such as for a radio receiver. In a radio receiver, incoming signals are received by an antenna and sent to a low noise amplifier (LNA). Between the antenna and the LNA is an I/O pad, which is connected to the two protection diodes in an ESD pad circuit. Figure 3.32 illustrates this example and shows its equivalent AC circuit model. The antenna is represented by a voltage source in series with a 50 Ω resistor. The diodes, meanwhile, have a small amount of parasitic capacitance represented by a single capacitor to ground.

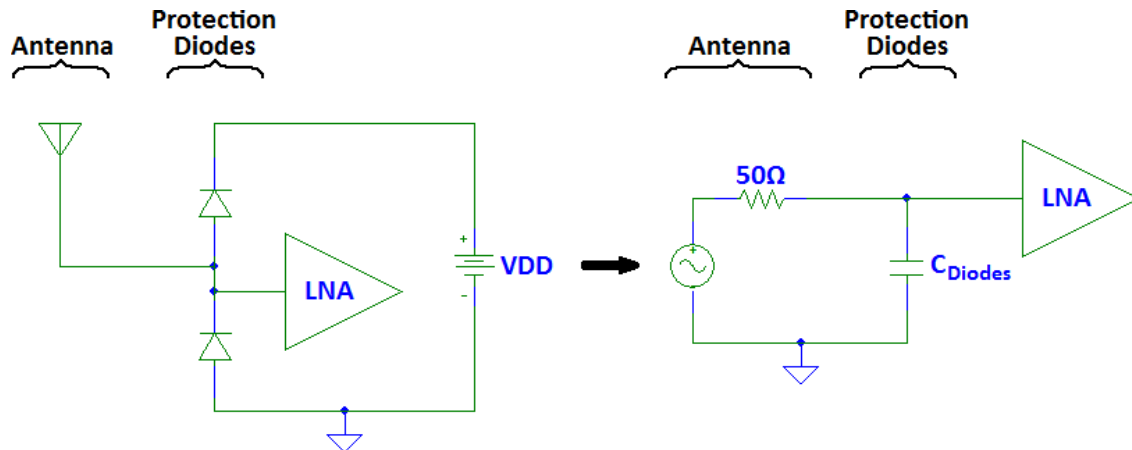

Figure 3.32 Front-end of a radio receiver and its AC circuit model

The model shown in Figure 3.32 reveals a low-pass filter formed by the antenna and ESD pad combination. At high frequencies, the protection diodes become low impedance circuits to ground due to parasitic capacitance. Making the protection diodes larger, as proposed in the most robust designs, runs the risk of filtering out the desired RF signals before they reach the internal circuitry. To simulate this scenario, the test circuit in Figure 3.33 was devised to obtain the frequency response of three ESD pads, each using different diodes.

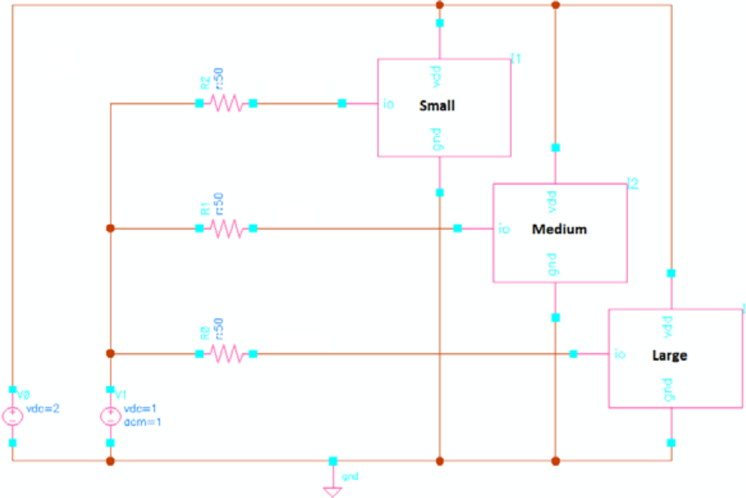

Figure 3.33 Test circuit to obtain diode capacitance

Because the capacitance of a diode alters depending on its bias voltage, the test circuit uses 2 V for the VDD line and 1 V for the I/O pad. The three sets of diodes simulated include those proposed in this section (large), those used in the first design (medium), and a set of diodes designed specifically for high frequency applications (small). Figure 3.34 shows the frequency response for each set of diodes.

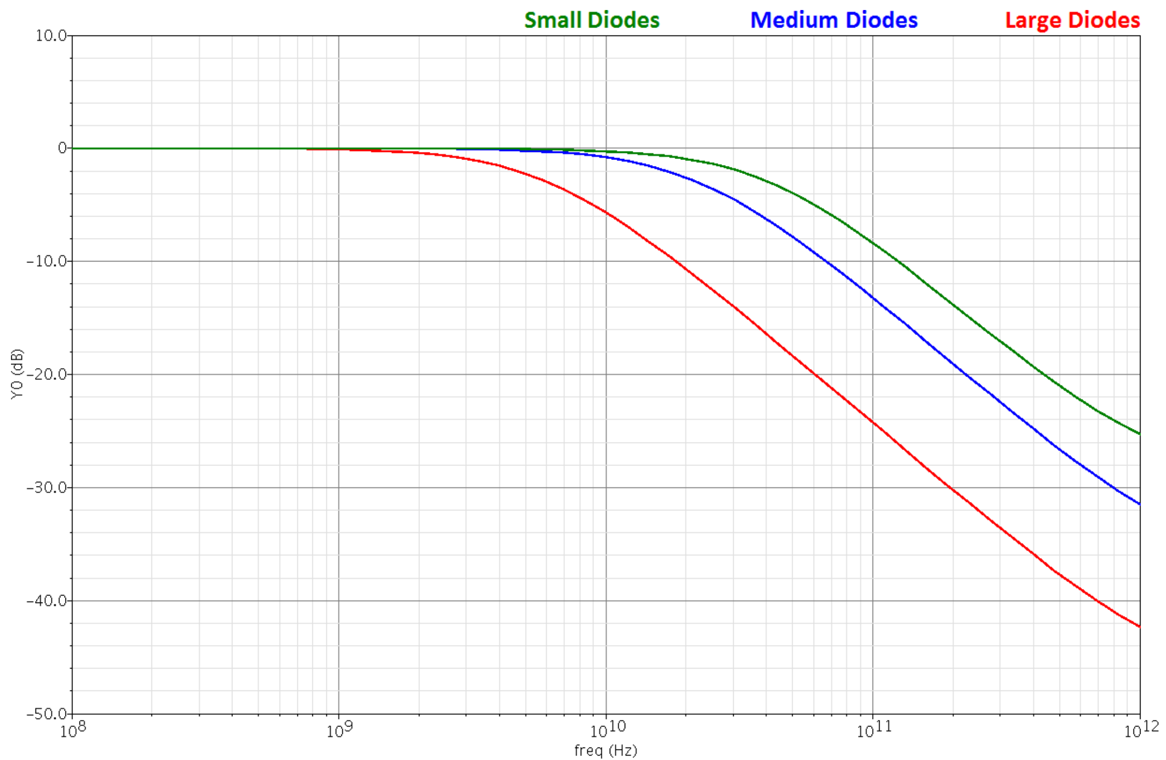

Figure 3.34 Frequency responses for the diodes in Figure 3.34

Using the corner frequencies from Figure 3.34, the capacitances for the large, medium, and small diodes were determined to be 520, 141, and 75 fF, respectively. Combined with a 50 Ω antenna, an ESD pad using the large diodes would have a 6.1 GHz corner frequency. A 2.4 GHz signal would experience an attenuation of just 0.6 dB, meaning an RF ESD pad design can use the large diodes to receive a high level of protection without sacrificing high frequency performance. The small diodes have an excellent frequency response with a 42 GHz corner frequency and virtually no attenuation at 2.4 GHz. As Figure 3.35 shows, however, they suffer from being too small to protect the pad from large ESD events. The large currents from a 500 V CDM event allow an alarmingly high voltage of 43 V to develop at the I/O pad.

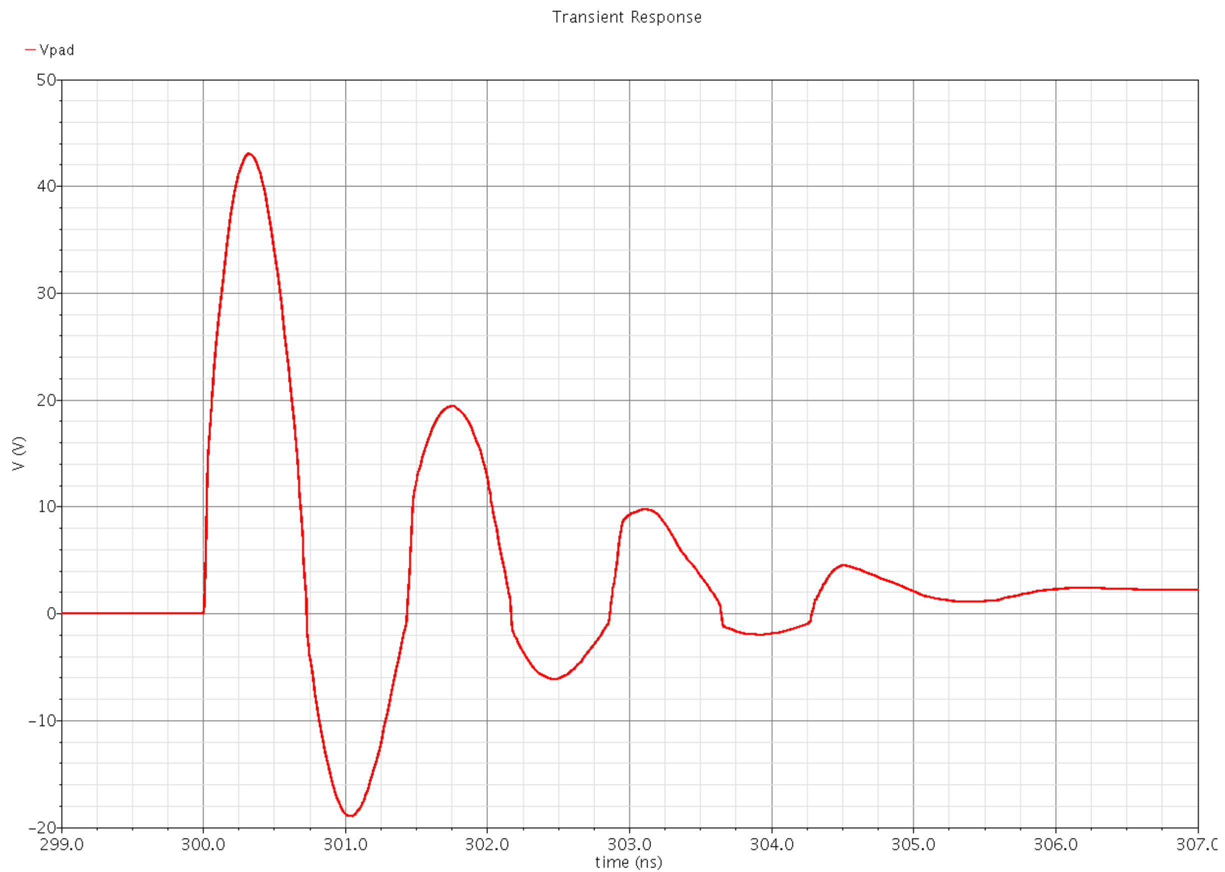

Figure 3.35 CDM response using the small diodes in an ESD pad

3.3.5 Voltage Clamp Optimization

The first clamp design shown previously in Figure 3.9 worked well during the first run through the different simulation scenarios, but its implementation in an IC is unrealistic. Specifically, a 200 pF capacitor takes up far too much die area for the clamp to have any practical value. The first step towards a new design is to replace the ideal resistor and capacitor with a PFET and an NFET, respectively. Figure 3.36 shows the new circuit topology.

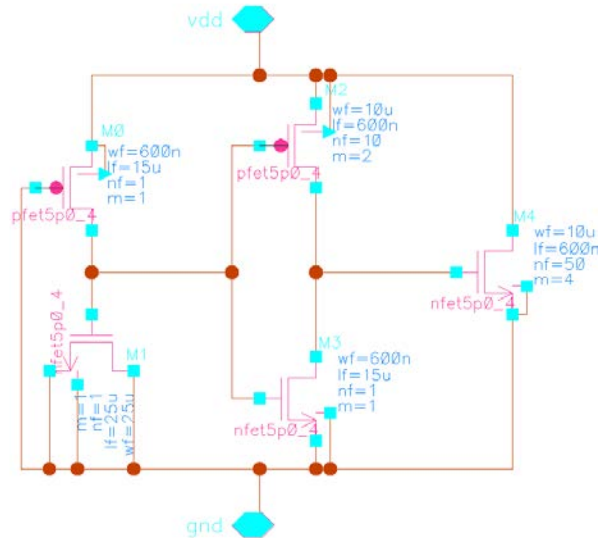

Figure 3.36 Proposed voltage clamp design

The NFET (M1) is connected as a MOS cap and, at approximately 2 pF, has far less capacitance than the design in Figure 3.9. The gate of the PFET (M0) is connected to ground, keeping the FET on at all times and essentially acting as a resistor. To compensate for the drop in capacitance by switching to the MOS cap, the resistance value of the M0 must be greatly increased. By making its length 25 times larger than the width, its channel becomes highly resistive – approaching the MΩ range.

Clamps have two main performance parameters: clamp resistance and turn-on speed. Lowering the clamp resistance mitigates the stress voltages seen by the IC circuitry during a high current event. The clamp resistance is determined by the size of M4. Unfortunately, increasing the size of M4 lowers the clamp's turn-on speed. As M4 is the largest component in the circuit, its gate-to-source capacitance determines the clamp's time constant. To counteract the increase in capacitance and lower the gate's time constant, the design decreases the channel resistance of M2 by increasing M2's W/L ratio from 140 to 333.

Increasing the size of M2 and M4 improves the performance of the clamp at the cost of taking up more space on the IC. These size increases were somewhat offset by decreasing the size of the other three FETs. The new design decreases both the width and length of M3. M3 still has very high resistance with the new sizing and reducing its size has no effect on the clamp's performance provided it can overcome any leakage through the normally-off M2 device. The same is true of M0, which is a copy of M3. Changing M1 does have an effect on the clamp's performance. Making it smaller decreases the maximum voltages seen during a CDM event, but increases the voltage spike at the beginning of a HBM event. As a CDM event is more dangerous to an IC, M1 was decreased during the design process. Finally, the length of M2 was decreased to minimum size to help offset the increase in its width.

An ESD pad employing the large diodes was used to analyze the performance of the proposed clamp compared to the performance of the first clamp design. Figure 3.37 compares their HBM responses. The faster turn-on speed reflects the increase in the size of M2, as the new design has a maximum voltage 400 mV lower than the clamp used in the first design. Making the clamp faster reduces both the magnitude and width of the initial voltage pulse.

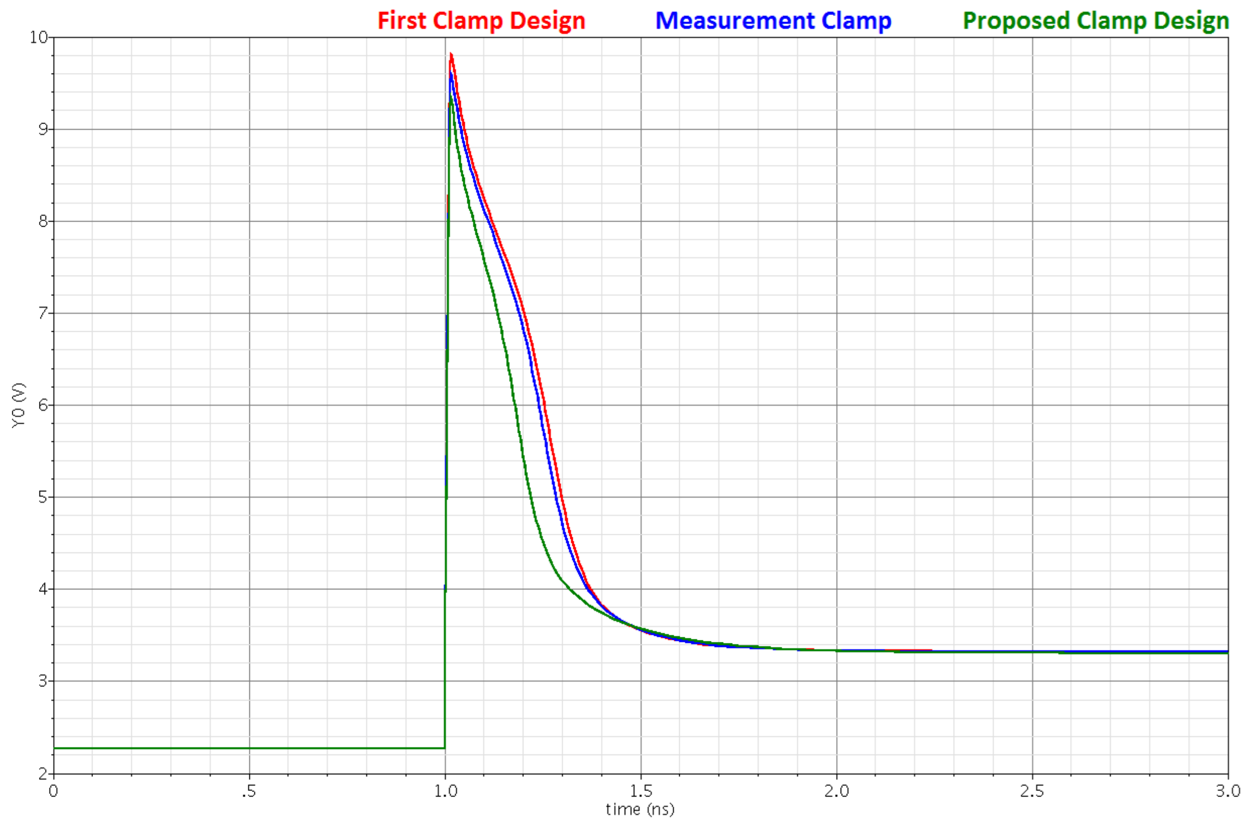

Figure 3.37 Comparison of ESD pad HBM performance, varying clamp design

CDM performance comparisons for each clamp are shown in Figure 3.38. The proposed clamp actually has a higher initial peak than the first design, rising 200 mV to 15.4 V. Except for the first pulse, the new clamp outperforms the other two clamps for every CDM pulse.

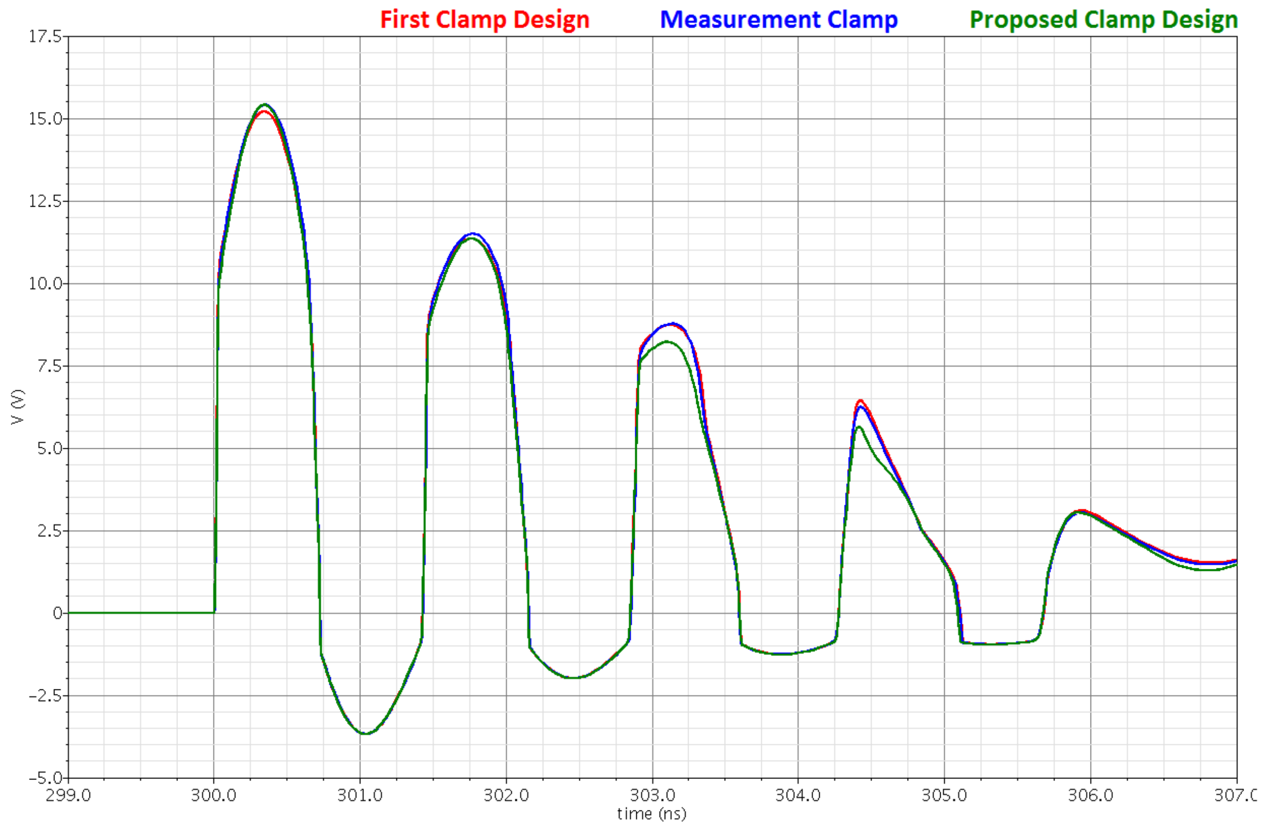

Figure 3.38 Comparison of ESD pad CDM performance, varying clamp design

Figure 3.39 shows the results for the MM scenario, where the new design outperforms each of the other clamp designs. The maximum voltage drops 400 mV to 7.6 V using the new design. Theses simulations show that increasing the size of M2 and M4 play the largest role in improving clamp performance. Reducing the size of the other three FETs saves some space without hurting performance. Up to a certain point, reducing the size of the MOS cap actually helps improves clamp performance.

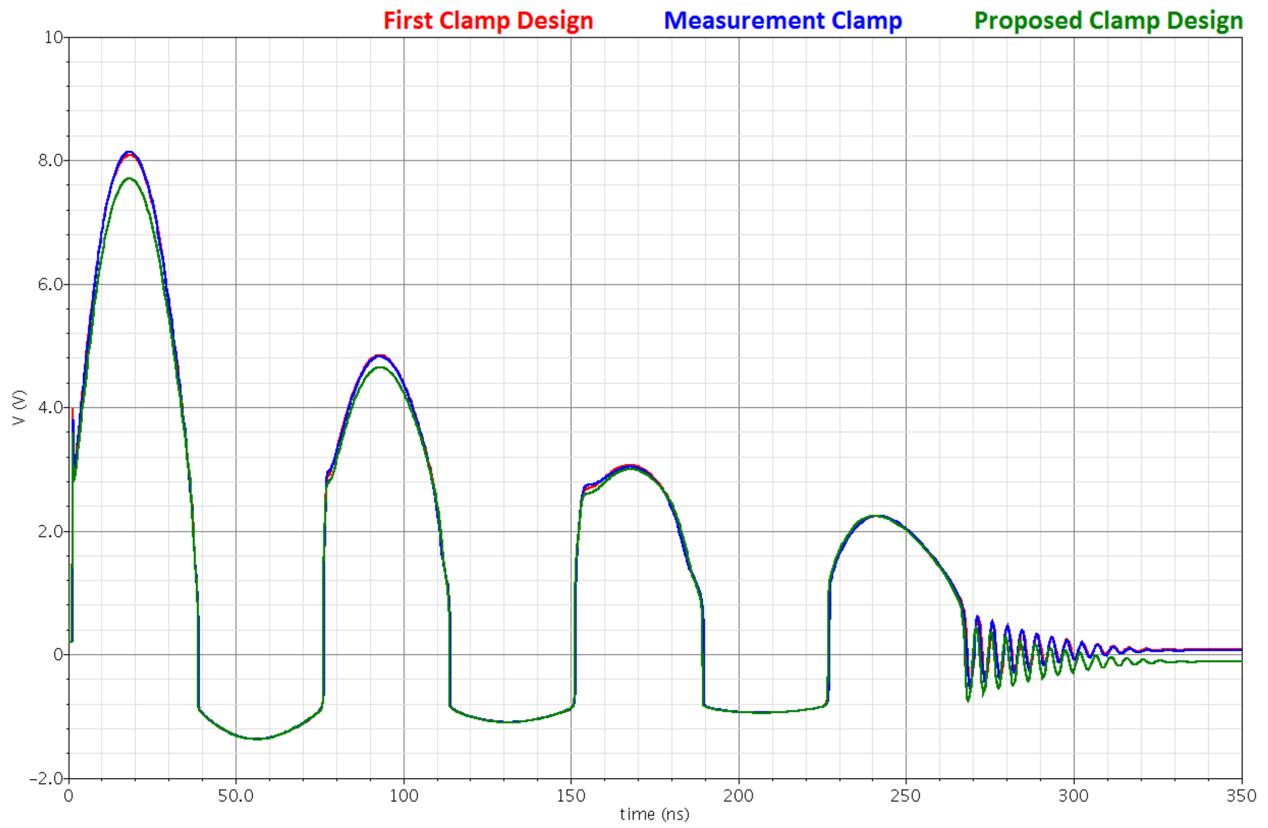

Figure 3.39 Comparison of ESD pad MM performance, varying clamp design

3.4 Proposed ESD Pad Design Analysis

The previous sections demonstrate the effectiveness of the changes made to elements within the ESD pad design. Combining all of these elements, Figure 3.40 shows the proposed ESD pad design.

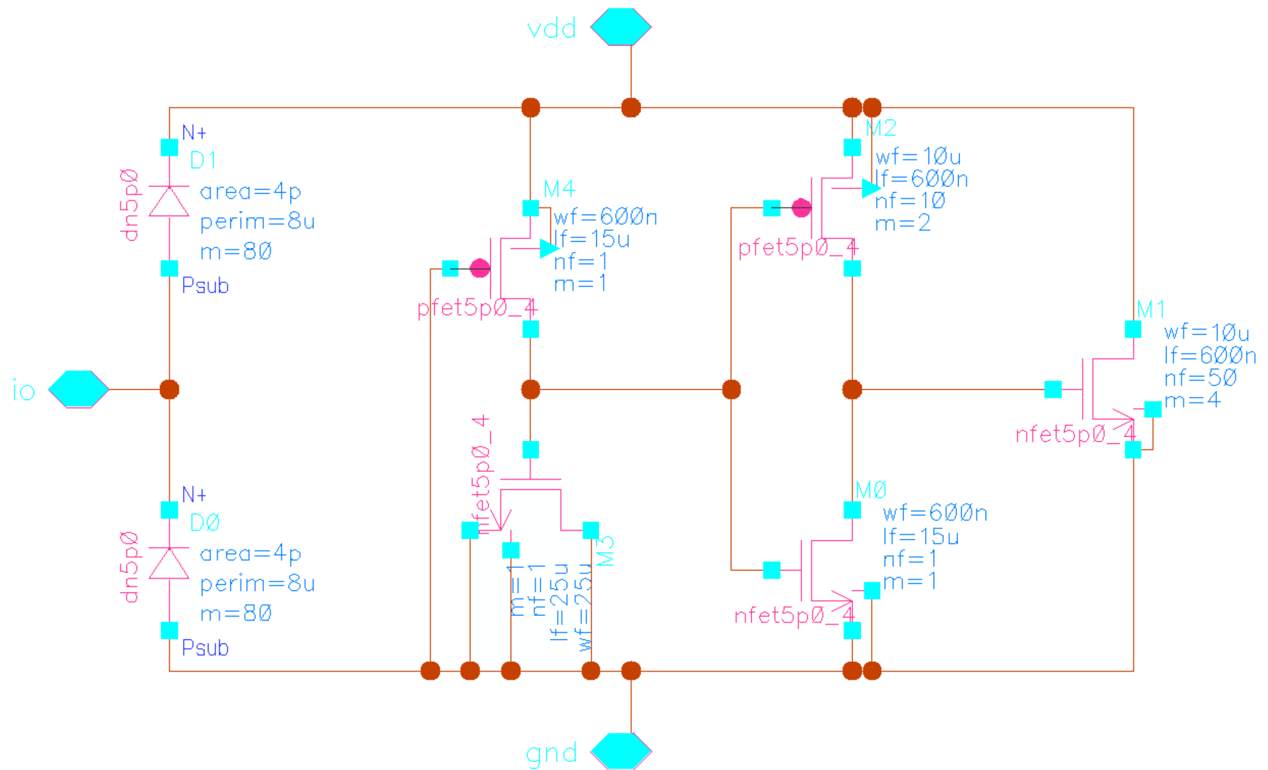

Figure 3.40 Proposed ESD pad design

Figures 3.41, 3.42, and 3.43 compare the new design to the first design presented in Section 3.2 and the high frequency design using the small diodes presented in Section 3.3.4. Maximum voltages for the ESD pad are 9.2 V, 15.4 V, and 7.6 V for the HBM, CDM, and MM scenarios, respectively. The proposed design performs much better than the first design, largely due to increased protective diode size. The high frequency design serves a specific purpose, offering extremely high frequency response with marginal protection against HBM and MM events and very little protection against a CDM event.

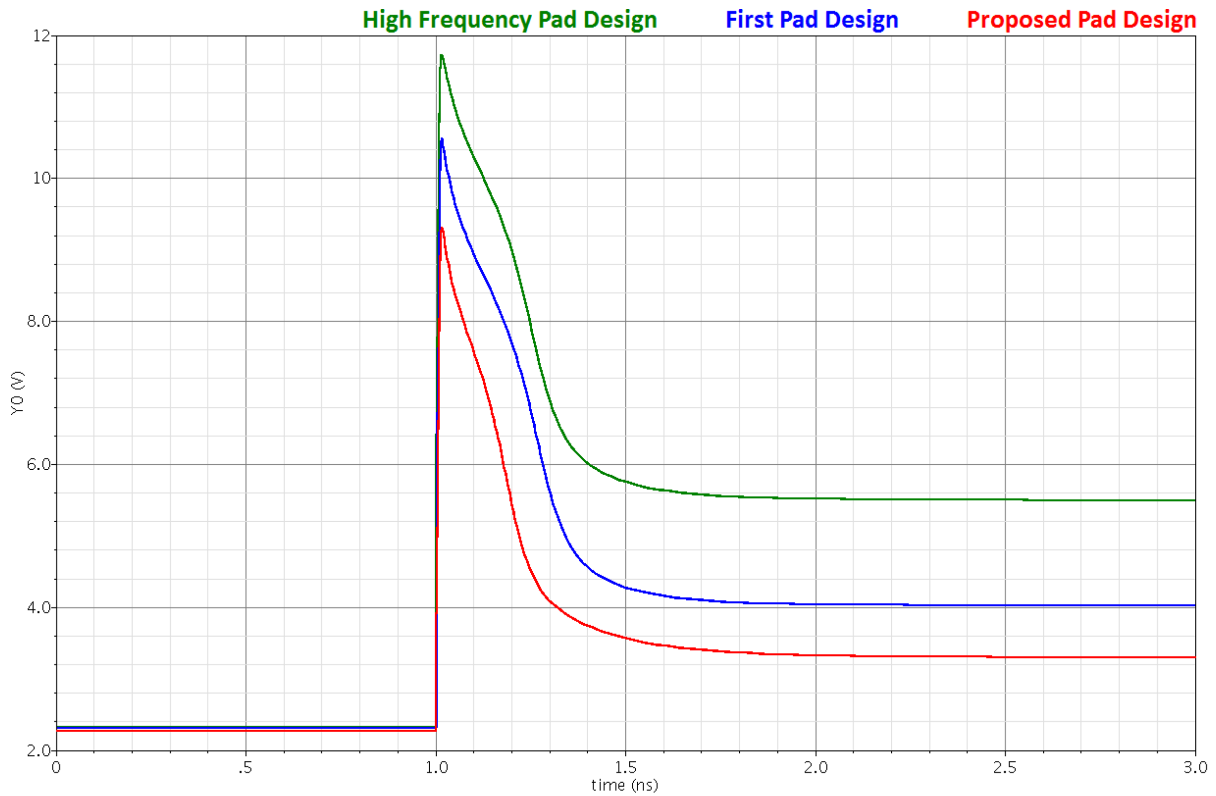

Figure 3.41 HBM response of the proposed ESD pad compared to two other designs

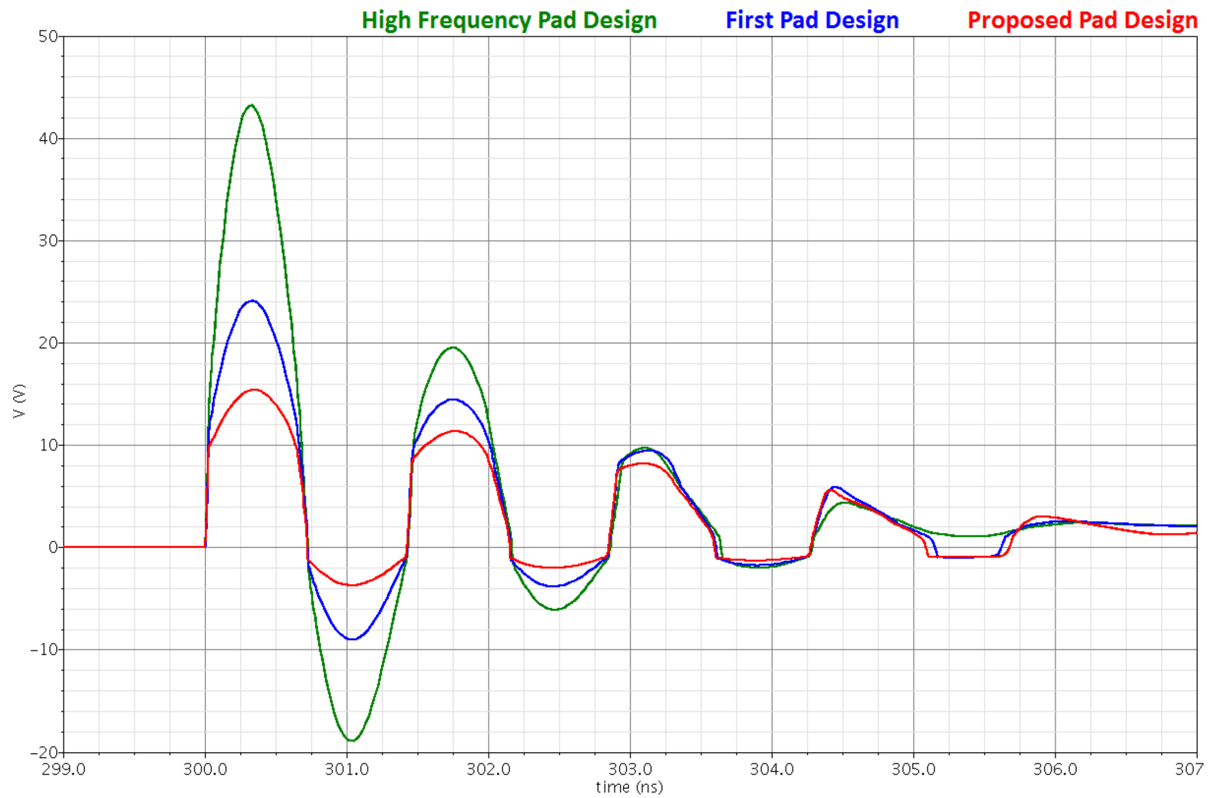

Figure 3.42 CDM response of the proposed ESD pad compared to two other designs

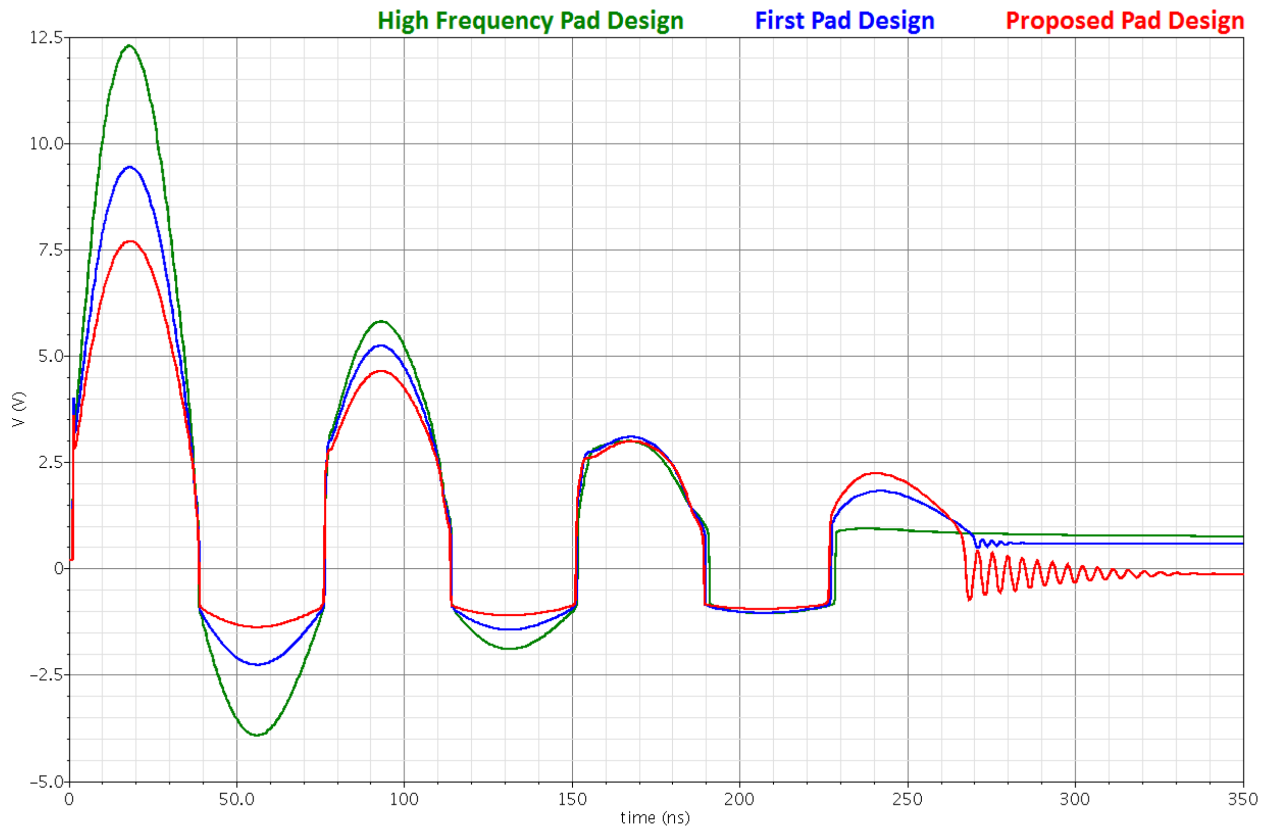

Figure 3.43 MM response of the proposed ESD pad compared to two other designs

Revisiting the 13 V limit established in 3.3.1, the ESD classifications are found for each ESD type. This is accomplished for the HBM and CDM scenarios by adjusting the initial voltage charge for each scenario until the pad registers a 13 V maximum stress voltage. The MM pulses last much longer than the other two, forcing the voltage limit to be set lower. Using Figure 3.25, it is estimated that a 40 ns pulse should be no higher than 11 V. While it is true that an HBM event lasts roughly the same amount of time as an MM event, the HBM event simulation has a faster rise time than an MM event. Because there is no inductance in the simulation, the HBM event simulation shows a dangerous voltage spike not seen in MM events. Fortunately, this is largely an artifact of the classic model, which does not truly mimic an actual HBM rise time seen in the real world.

Based on the criteria described above, the ESD pad design offers excellent protection against HBM ESD, able to protect the inner circuitry from a 5.3 kV HBM event. This grants the pad a 3A HBM classification; the second highest classification [4]. The ESD pad performs moderately well against CDM ESD, able to protect against a 325 V CDM event. This places the

ESD pad in the C3 CDM class, which is the fourth out of seven classification levels [6]. The ESD provides excellent protection against MM ESD, protecting against a 230 V MM event. This qualifies the pad for the M3 MM class, which is the second highest classification level [7]. Figures 3.44, 3.45, and 3.46 show how the pad responds to each event limit.

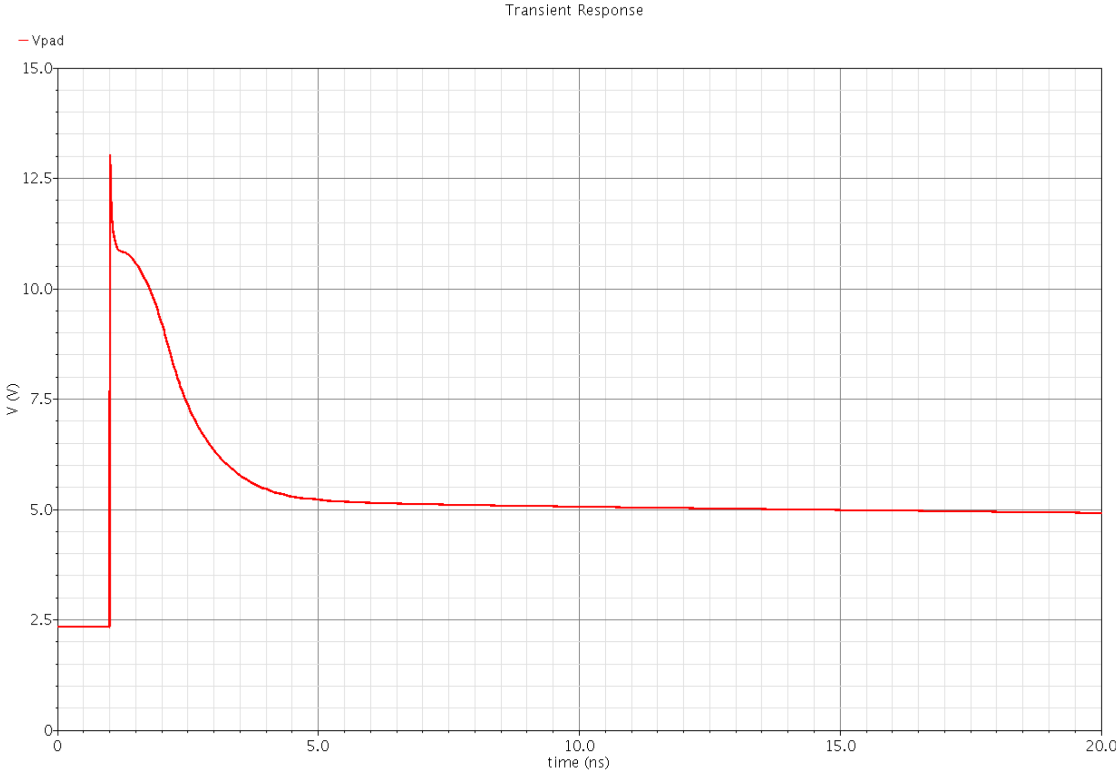

Figure 3.44 Response of the proposed ESD pad to its maximum HBM voltage: 5.3 kV

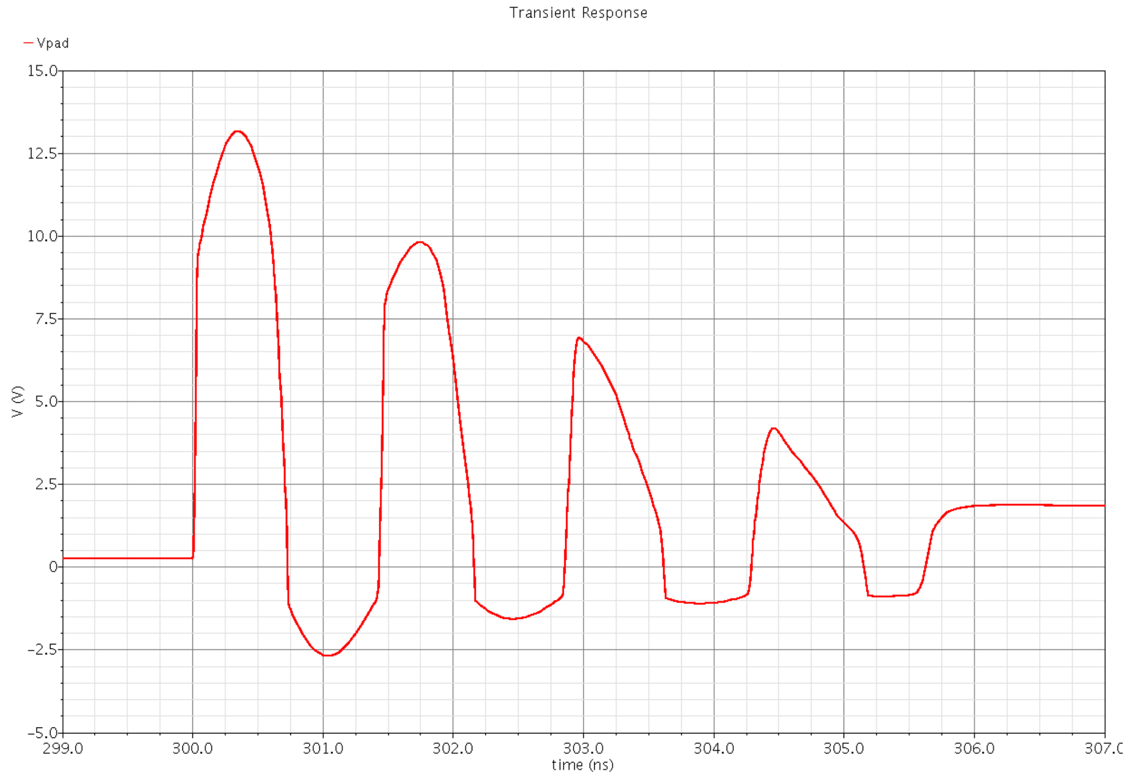

Figure 3.45 Response of the proposed ESD pad to its maximum CDM voltage: 325 V

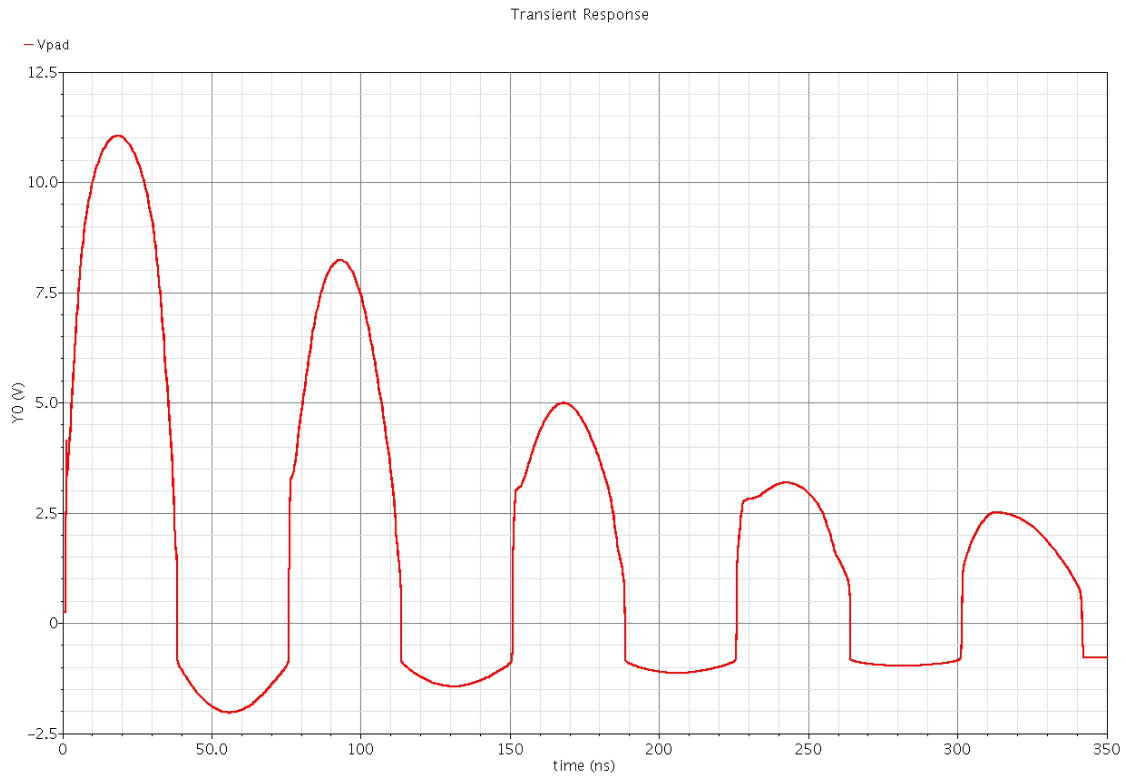

Figure 3.46 Response of the proposed ESD pad to its maximum MM voltage: 230 V

Chapter 4 - ESD Detection Circuits

4.1 Prior Art ESD Detection Circuit

Chapter 3 established an ESD pad design capable of protecting against various levels of each ESD event type while still allowing an I/O pad to operate at 2.4 GHz. The next goal of this research is to combine a high level of ESD protection with an effective method of detecting the occurrence of an ESD event. The proposed detection method is based on IC fuses. Prior to presenting an IC fuse-based approach, this section analyzes another approach.

This other approach is a CR-based ESD detection circuit and is shown in Figure 4.1 [14]. It operates similarly to the ESD-transient triggered voltage clamp used in Chapter 3, using a capacitor and a resistor – hence, CR-based – as an AC voltage divider. In contrast to the voltage clamp, the resistor and capacitor are flipped, meaning V_X stays low under normal DC operating conditions. Operating the detection circuit requires the reset pad to be connected to VDD in order to turn on M_{nr}, which forces V_A and V_{OUT} high. During an ESD event, the capacitor holds its voltage, but the voltage across R increases, turning on M_{n1}. With M_{n1} on, V_A goes low and triggers the chain of inverters to also set V_{OUT} low. The output continues to hold this value until the circuit is reset.

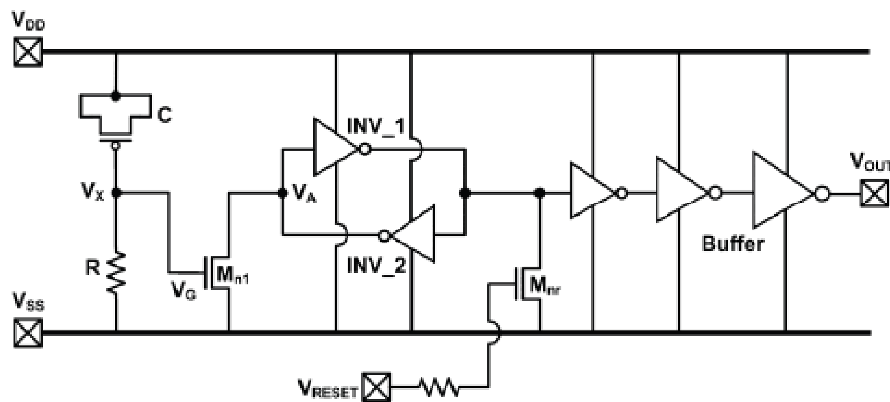

Figure 4.1 CR-based ESD detection circuit (figure from [14])

This circuit is effective at detecting ESD events. The main drawback, however, is that the circuit requires a power supply in order to function. CDM and MM type events occur well before the IC is powered. If an IC is going to detect these types of events, it must operate without a power supply.

4.2 Proposed Built-In Self-Test for ESD Events

Detecting all types of ESD events is important for high reliability systems. An IC compromised during production, either by a CDM or MM pulse, must be identified before being placed in such a system. This research proposes an IC fuse-based ESD detection circuit, shown in Figure 4.2. This circuit utilizes IC fuses, allowing CDM and MM events to be detected without requiring the IC to be powered at the time of the event.

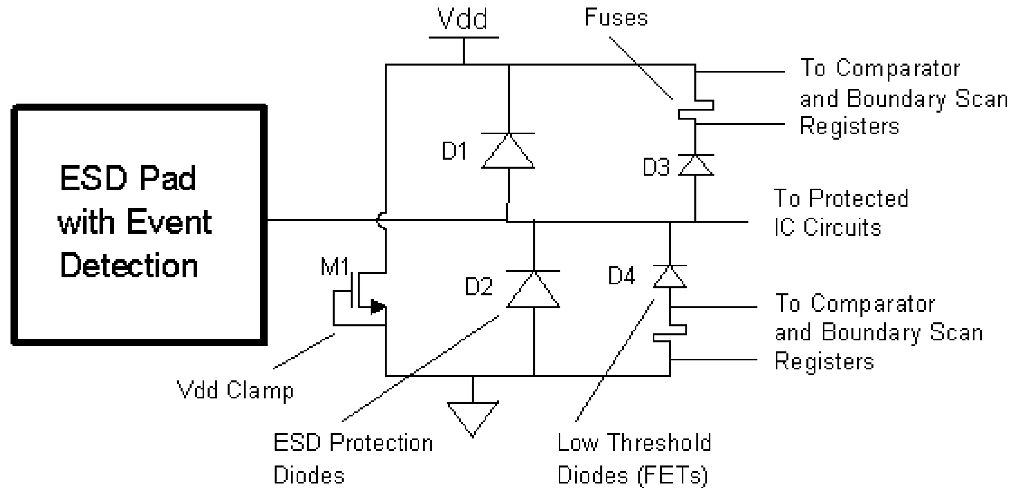

Figure 4.2 Proposed ESD Pad with IC Fuse-Based ESD Detection Circuit

Briefly mentioned in Chapter 3, IC fuses are metal traces in an integrated circuit designed to fail during an ESD event. Each metal layer in a process has a maximum current allowable per trace width, making narrower traces more likely to fail. Using an extremely narrow metal trace section, or IC fuse, the circuit designer designates that section as a fail point. Knowing where the circuit will fail during an ESD event allows for the proper placement of ESD detection circuitry.

As shown in Figure 4.2, fuses are placed near each pad. A pad hit with an ESD event activates a low threshold diode before a protection diode, forcing a high amount of current to flow through the fuse. Designed properly, the fuse breaks, creating an open circuit at that point. Once the circuit is powered, a comparator with each input connected to either side of the fuse detects the open circuit. Boundary scan registers then query each pad to determine which pads have been compromised and feed that data back to the user. This built-in self-test (BIST) for ESD events allows manufacturers to select the best ICs to use when reliability is a must.

Chapter 5 - ESD Measurements and IC Fuses

5.1 ESD Measurement Setup

The simulations presented in Chapter 3 provide a convenient way to test ESD protection circuitry under a wide variety of settings. Measurements performed in a lab, however, offer real-world evidence of a circuit's functionality. The collection of simulation and measurement results complement each other. When measurements closely resemble simulations, it lends credibility to the simulation models.

The simulations performed in Chapter 3 did not model circuit failures due to stress voltages. Protection diode or voltage clamp failure is entirely possible and basing design solely on simulations is risky at best. More importantly, the simulator cannot simulate IC fuse operation. An effective measurement setup must therefore be established capable of overcoming several challenges that arise when measuring ESD events. Some of these problems include isolating test equipment from the ESD events, detecting high frequency events, and preventing the corruption of measurements due to ringing.

The test circuits closely resemble those used in simulations. Each simulation circuit included a switch controlled by a voltage source. For the measurement circuits, the switch is replaced by a DPST 12 VDC armature relay powered by a Hewlett Packard E3616A DC supply. While some supplies include switches capable of disabling the DC output without cutting power to the unit itself, this supply has no such feature. During initial testing, it was felt that the supply's power switch prevented the relay from making a clean switch due to the supply's turn-on transients. Adding a SPST switch between the supply and relay removes the supply's turn-on transients as a potential switching problem. Figure 5.1 shows the test setup for an HBM measurement.

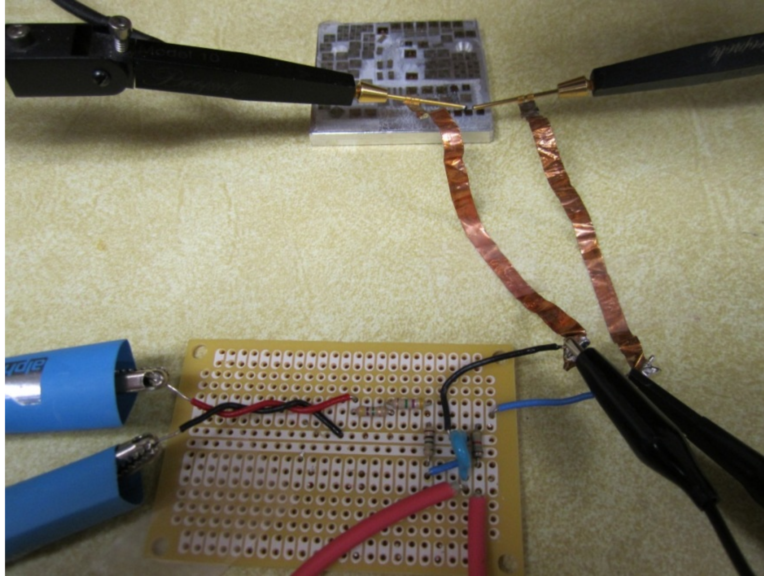

Figure 5.1 Measurement setup for ESD Measurements (second probe not shown)

As in the simulation schematics, the relay toggles the capacitor's connection between the charging circuit and the discharging circuit. The charging circuit charges the capacitor using a high voltage supply in series with a current-limiting 1 MΩ resistor. A PS350 high voltage supply from Stanford Research Systems, Inc. was used and is capable of outputting 5 kV. A probing station allows access to the DUTs on the ICs. Each probe has a center and ground lead. In an attempt to reduce the wire length and coax capacitance and delay effects between the discharging circuit and the probing circuit, short ribbons of copper were used between the probe's outer ground conductor and the discharging circuit. Only the needles connected to the grounds were used, preventing the coax transmission from being a factor during the measurements. Figure 5.2 shows the outer conductors of each probe making contact with two pads on an IC.

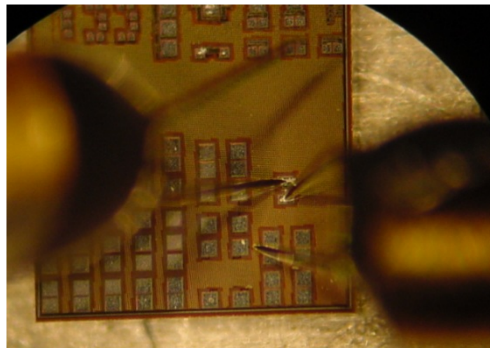

Figure 5.2 Probe tips making contact with an IC

A Tektronix TDS 724D 500 MHz oscilloscope capable of 2 GS/s was used to take measurements. Precautions were taken to protect the scope's inputs from ESD events. A 100:1 probe protects channel 1, which measures the voltage across the DUT. In addition to its high attenuation ratio, the probe is rated for 1.2 kV. This unfortunately falls well below the 5 kV limit of the high voltage supply, but it does allow for all three ESD types to be tested, even if not to their highest levels. The 1.2 kV rating of this probe is the reason for performing all HBM simulations at 1 kV rather than the more conventional 1.5 kV charge.

Channel 2 measures the voltage across the capacitor to observe the full ESD event and, more importantly, provide a predictable voltage pulse from which the scope can trigger. Protecting Channel 2 is a 10:1 probe supplemented by an approximate 10:1 voltage divider consisting of two 47 kΩ resistors and a 10 kΩ resistor. The composite 100:1 voltage division keeps Channel 2 safe from ESD events. A test was run on an HBM circuit to determine the effectiveness of the second probe. The DUT was replaced by a short circuit and both probes were connected to measure the voltage across the 1.5 kΩ resistor. The results are displayed in Figure 5.3. While channel 2 registers more noise, it is sufficient for providing a predictable trigger pulse.

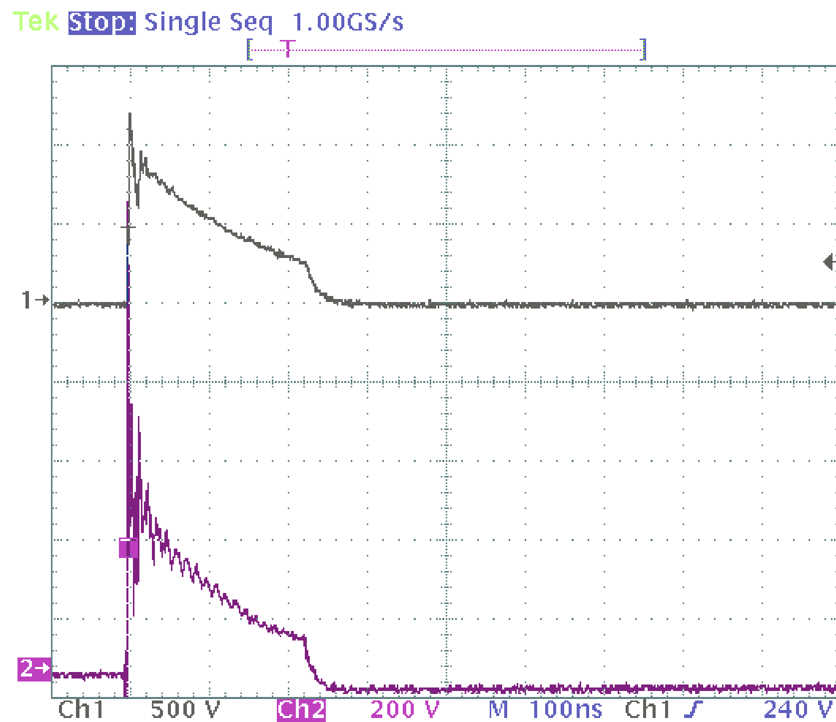

Figure 5.3 Measurement of an HBM event, using the test setup described

5.2 ESD Protection Circuitry Measurements

This section reports measurements of the ESD response of an existing voltage clamp circuit. Section 3.3.5 shows the simulation results for this clamp. The proposed ESD pad design presented in Section 3.3 was designed after the fabrication of the test ICs, making these measurements mainly an attempt to confirm ESD protection circuitry functionality and establish a working ESD measurement setup. Though these measurements cannot be used to compare one design to another, they can legitimize the simulations performed in Chapter 3.

Figure 5.4 shows the clamp's response to an HBM event, which reveals the main problem encountered during measurements: the current setup exhibits oscillatory behavior. The source of this ringing is unclear. Every wire within the setup has been minimized in an attempt to eliminate any parasitic inductance. The probing stations have coax cables approximately three long to connect the probe's inner and outer conductors. The inductance from this coax cable was believed to be the source of the ringing, but attaching copper ribbon as in Figure 5.2 did not help alleviate the problem.

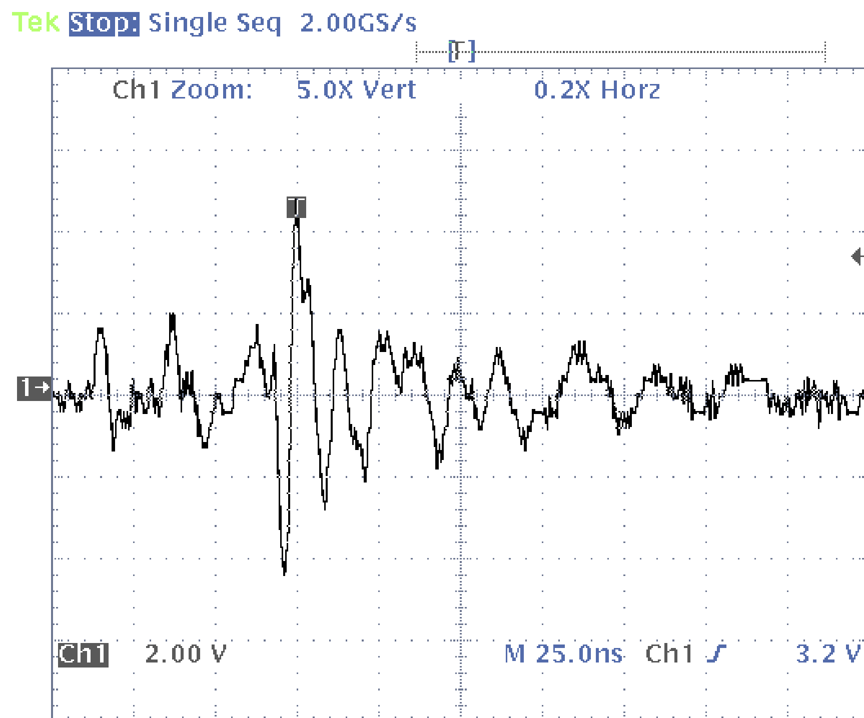

Figure 5.4 Voltage across a clamp hit with a 1 kV HBM event

The source of the problem is believed to be either the use of an armature relay or, once again, the probing stations. Even though the coax cables are not being directly used, they are still connected to the two outer conductors. These two conductors could be acting as an antenna transmitting a signal at a frequency and level that interferes with the measurements.

Several attempts were made to eliminate the ringing. The coax cables were coiled to minimize any transmissions. The armature relay was then replaced with a manual SPST switch, connected such that the high voltage supply is never removed from the circuit. To reduce the current drawn by this setup, the 1 MΩ current-limiting resistor was increased above 10 MΩ. Finally, the manual switch was replaced with a reed relay. It was believed that perhaps the ringing problem was related to the open-air contacts creating a plasma arc. In a reed relay, the contacts are sealed in a vacuum tube, thus avoiding the plasma arcing. Unfortunately, none of these attempts could rid the setup of the ringing.

As it is, Figure 5.4 shows that the clamp functions, even if the measurement setup is less than ideal. The clamp is effective at limiting the voltage, with the maximum voltage seen at an acceptable 4.5 V. Even if the current measurement setup does not allow for confirmation of the simulation models, it does confirm that the clamp design works.

5.3 IC Fuse Calculations

Built-in self-test for ESD events requires the use of IC fuses, making it important to determine the requirements for breaking a fuse. Fuse design is crucial to the proper functioning of the proposed circuit in Chapter 4. The fuse should have low enough resistance to make it the preferred path taken by the ESD event discharge. Both the resistance and mass of the fuse factor into the energy in a fuse during an ESD event. The mass of the fuse should therefore be kept to a minimum to prevent the fuse from being able to dissipate the power of an ESD event. Using a wide variety of levels for each type of ESD, this section determines which ESD levels have enough energy to break a 0.31 Ω aluminum fuse of dimensions 5 µm x 1 µm x 0.5 µm (mass of 7.02 pg). Figure 5.5 shows a visualization of the fuse used in the calculations.

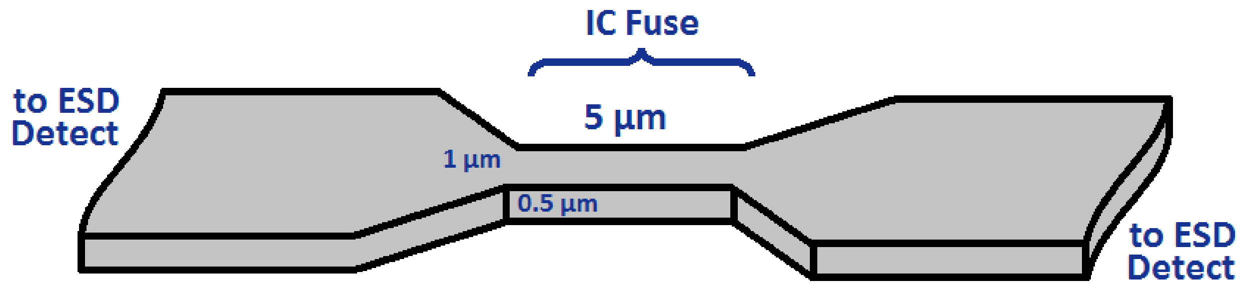

Figure 5.5 IC fuse dimensions used in calculations

5.3.1 Current through a Fuse during an ESD Event

Calculations were performed in MATLAB, first constructing current pulse matrices for each ESD type. Each matrix contained six current pulses; calculated using a range of voltage ranges customized for each ESD type: 500 V to 3 kV for the HBM pulse, 125 V to 750 V for the CDM pulses, and 50 V to 300 V for the MM pulses. Figures 5.6, 5.7, and 5.8 show the current pulses for each ESD type.

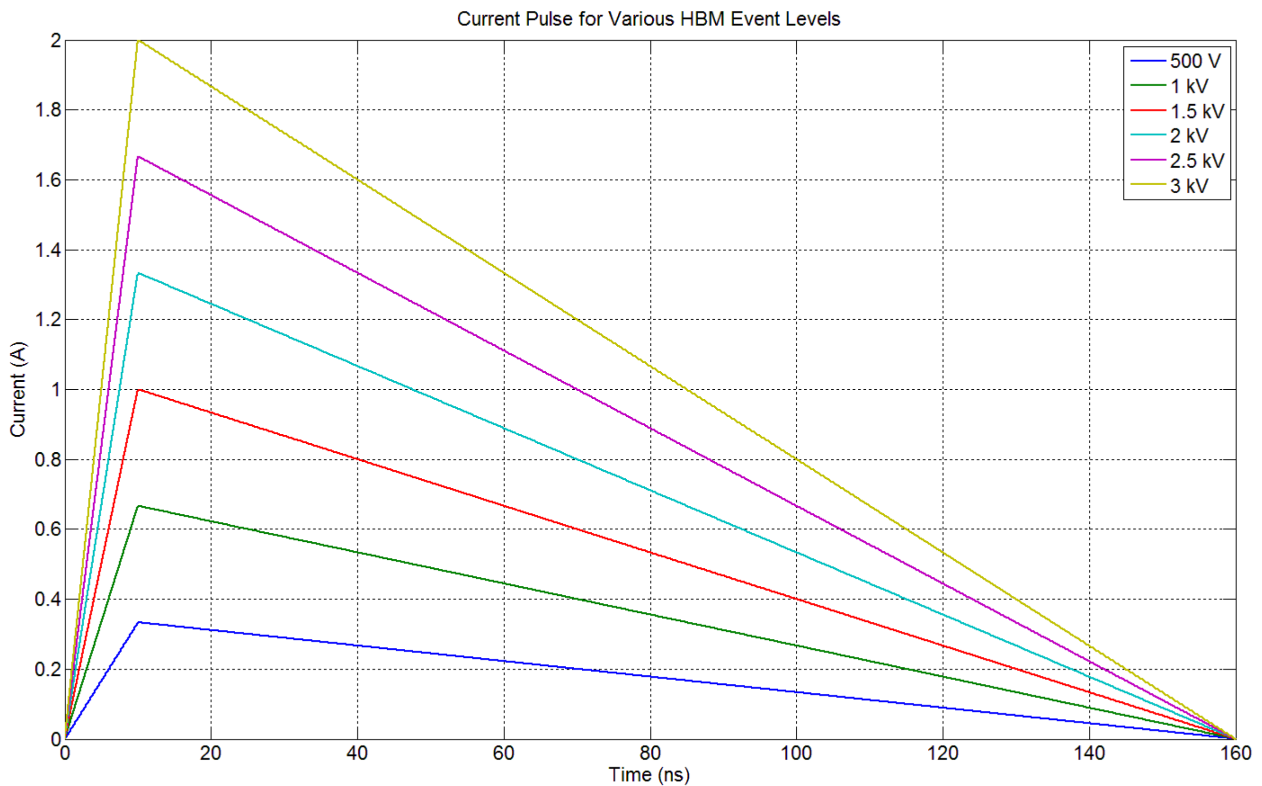

Figure 5.6 HBM current pulses

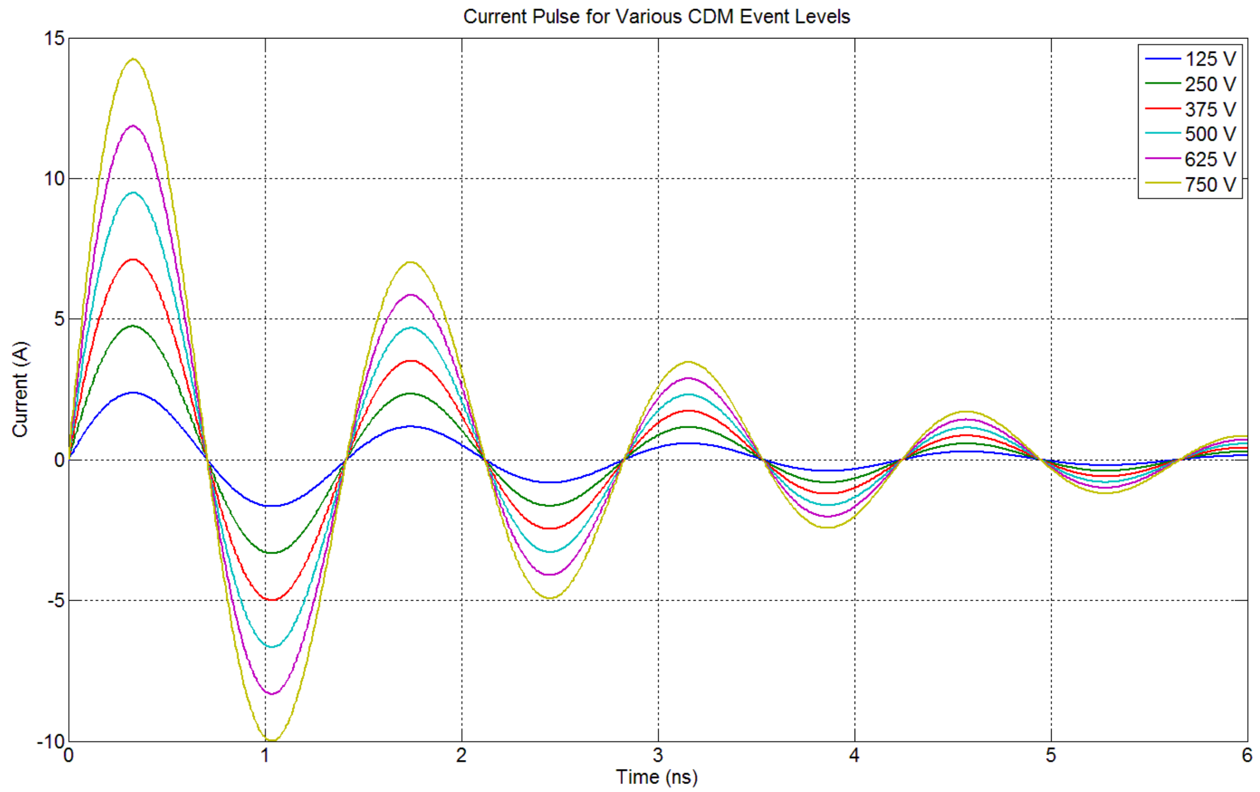

Figure 5.7 CDM current pulses

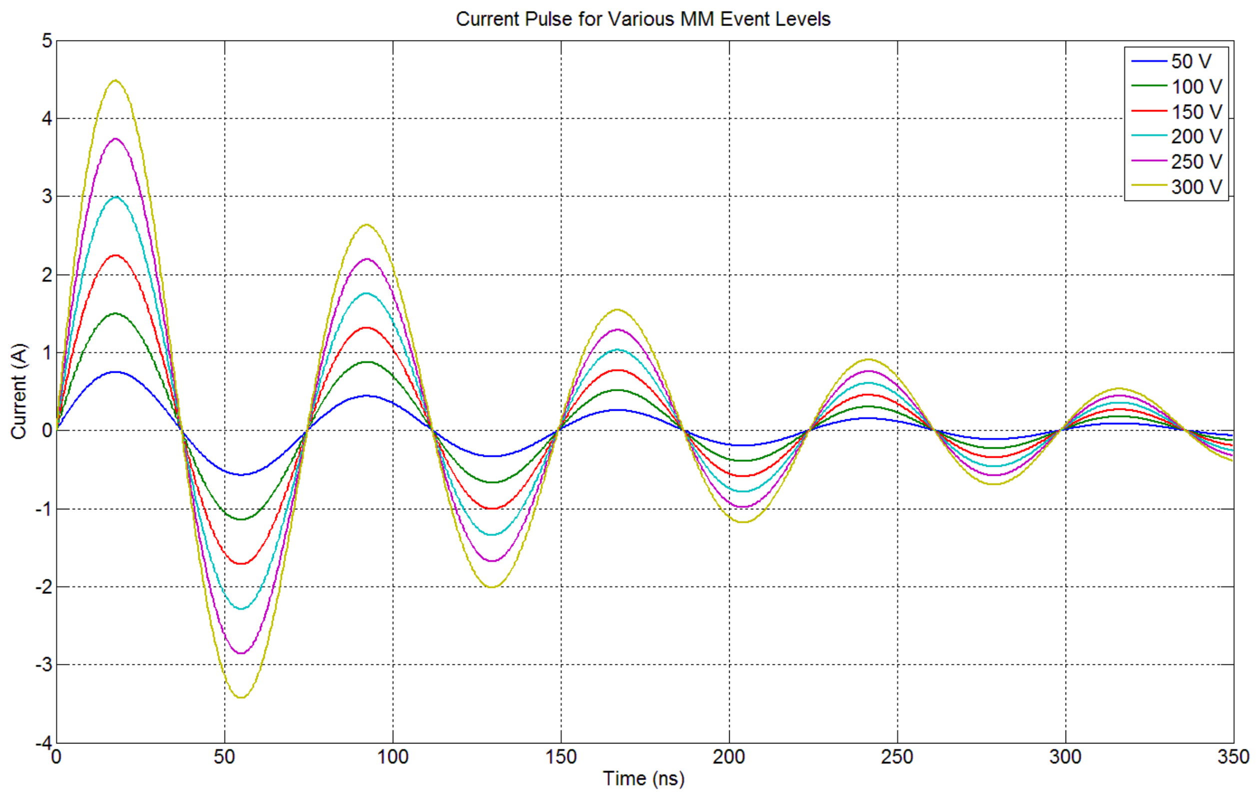

Figure 5.8 MM current pulses

5.3.2 Power Dissipated by a Fuse during an ESD Event

To calculate energy from current, the current pulses must be expressed as power pulses. Obtaining power from current requires a resistance. For these calculations, the fuse is assumed to be made entirely from aluminum with a resistance of 0.31 Ω. Figures 5.9, 5.10, and 5.11 show the power dissipated by the fuse during each ESD event.

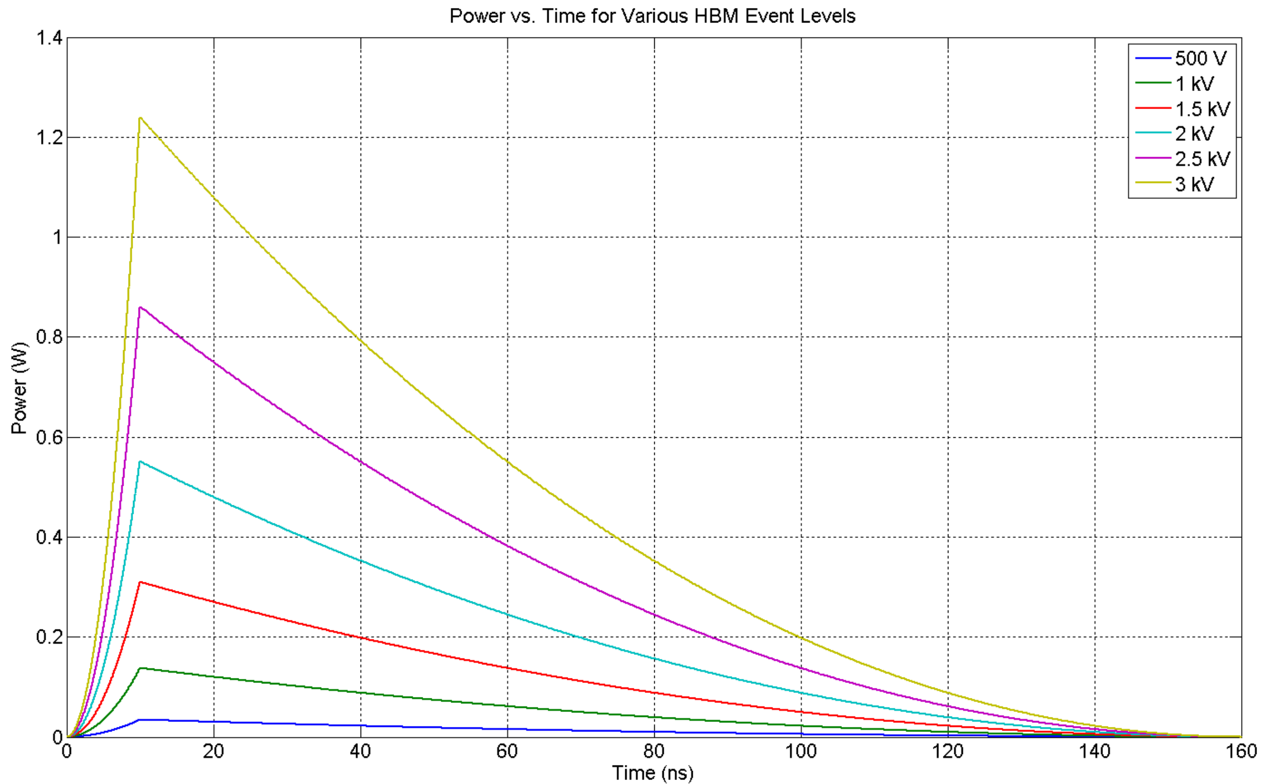

Figure 5.9 HBM power vs. time

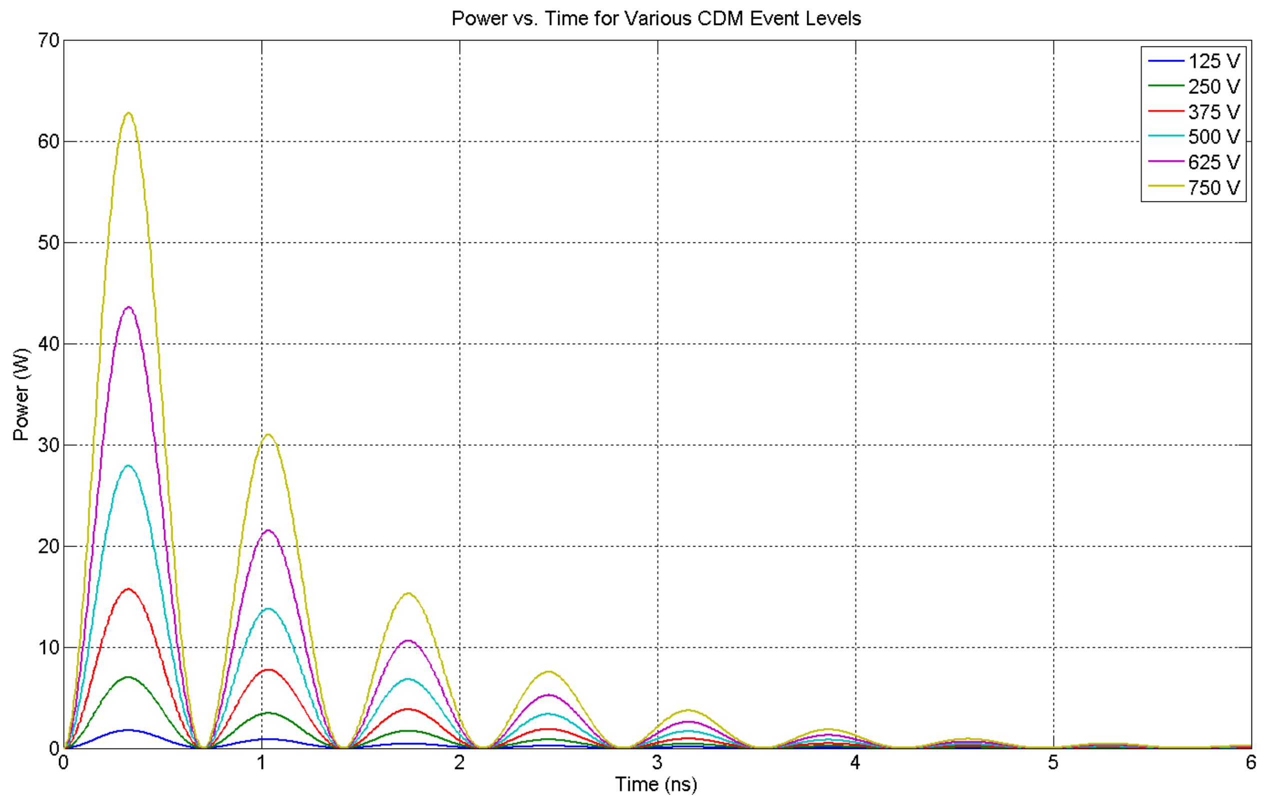

Figure 5.10 CDM power vs. time

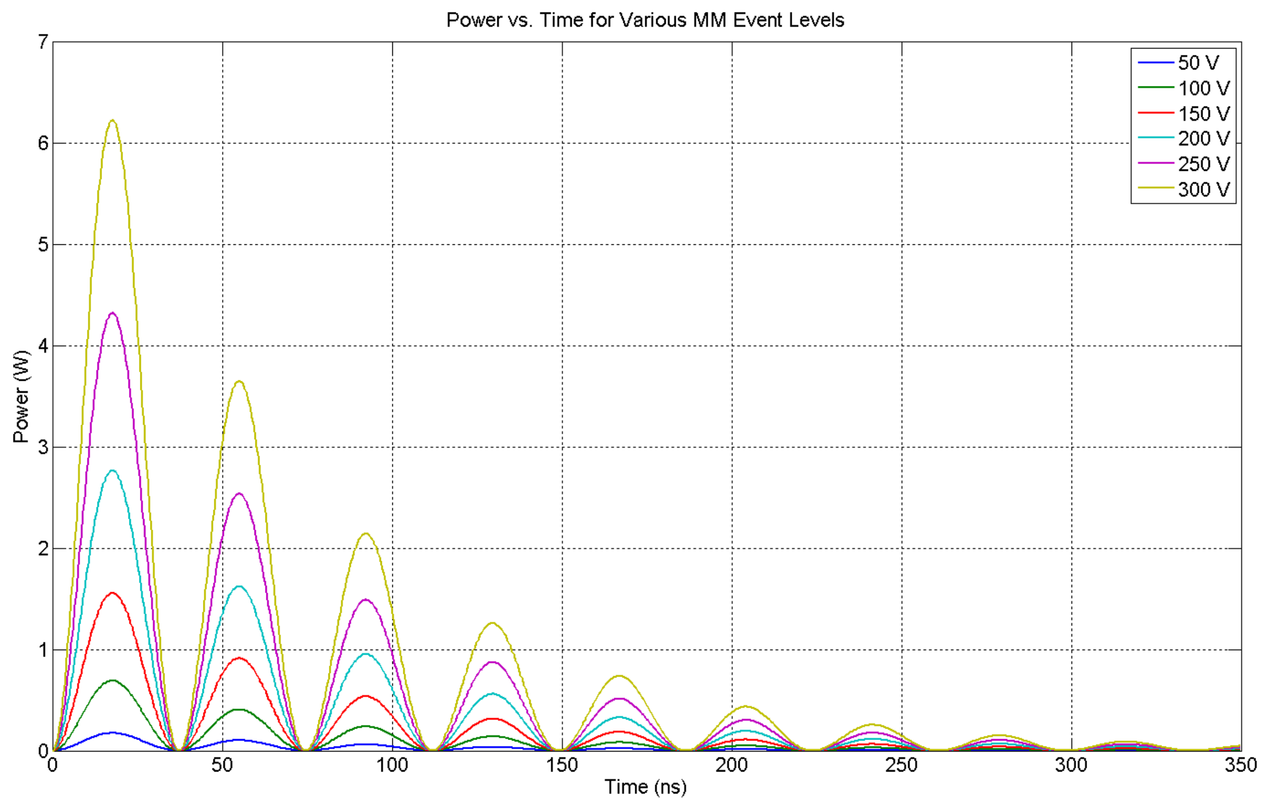

Figure 5.11 HBM power vs. time

5.3.3 Energy Transferred to a Fuse during an ESD Event

The energy plots in Figures 5.12, 5.13, and 5.14 are then calculated by integrating the power of each ESD event. One issue encountered when performing these calculations was determining how to handle the resistance of the fuse. At the ESD event's onset, the fuse has a resistance of 0.31 Ω. As the event's high current rapidly heats the fuse, it dramatically increases the resistance of the fuse, even creating an open circuit if the fuse breaks. However, an increasing resistance produces larger power dissipation as time progresses, possibly decreasing the current through the fuse if the fuse voltage is limited by other circuitry. Though these discrepancies keep the power and energy graphs from being entirely accurate, using a constant resistance for power and energy calculations provides a reasonable estimate of the energy transferred by each ESD event. Furthermore, it is believed to produce a conservative estimate of the total event energy into the fuse.

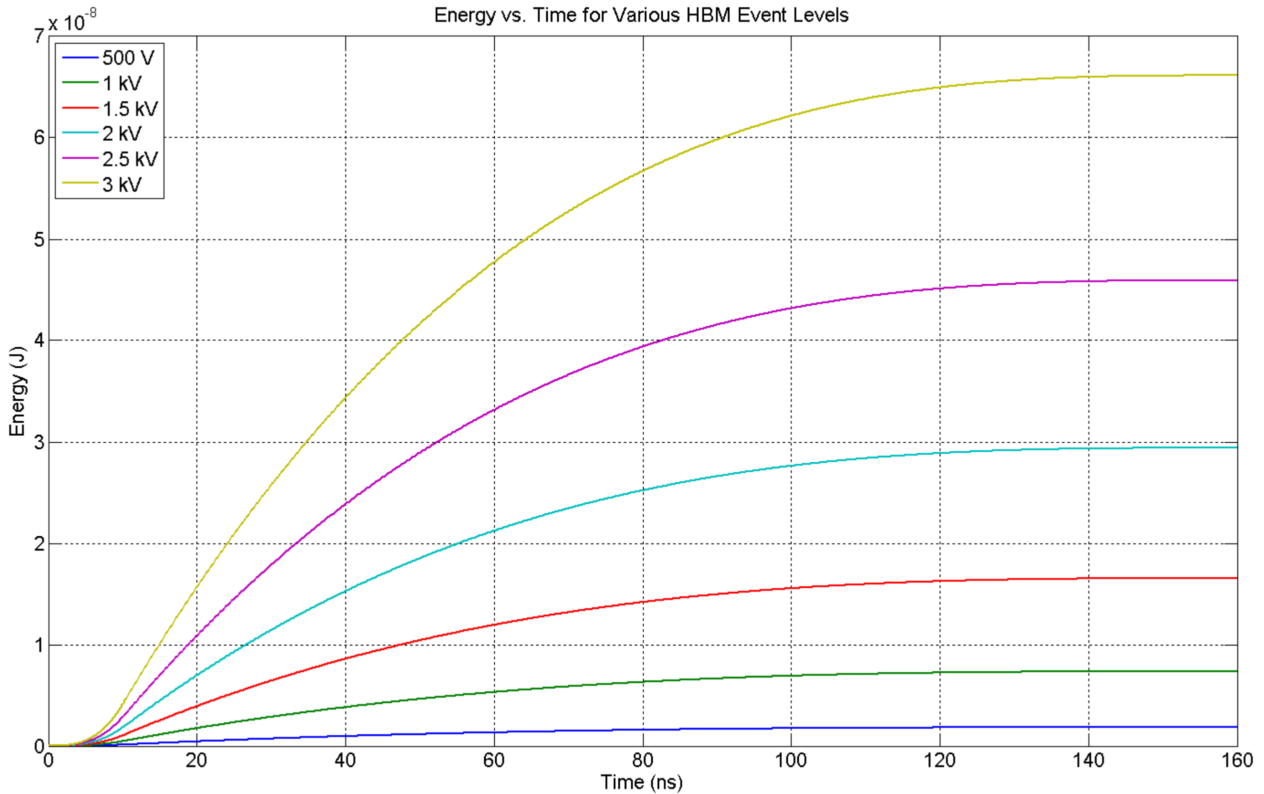

Figure 5.12 HBM evergy vs. time

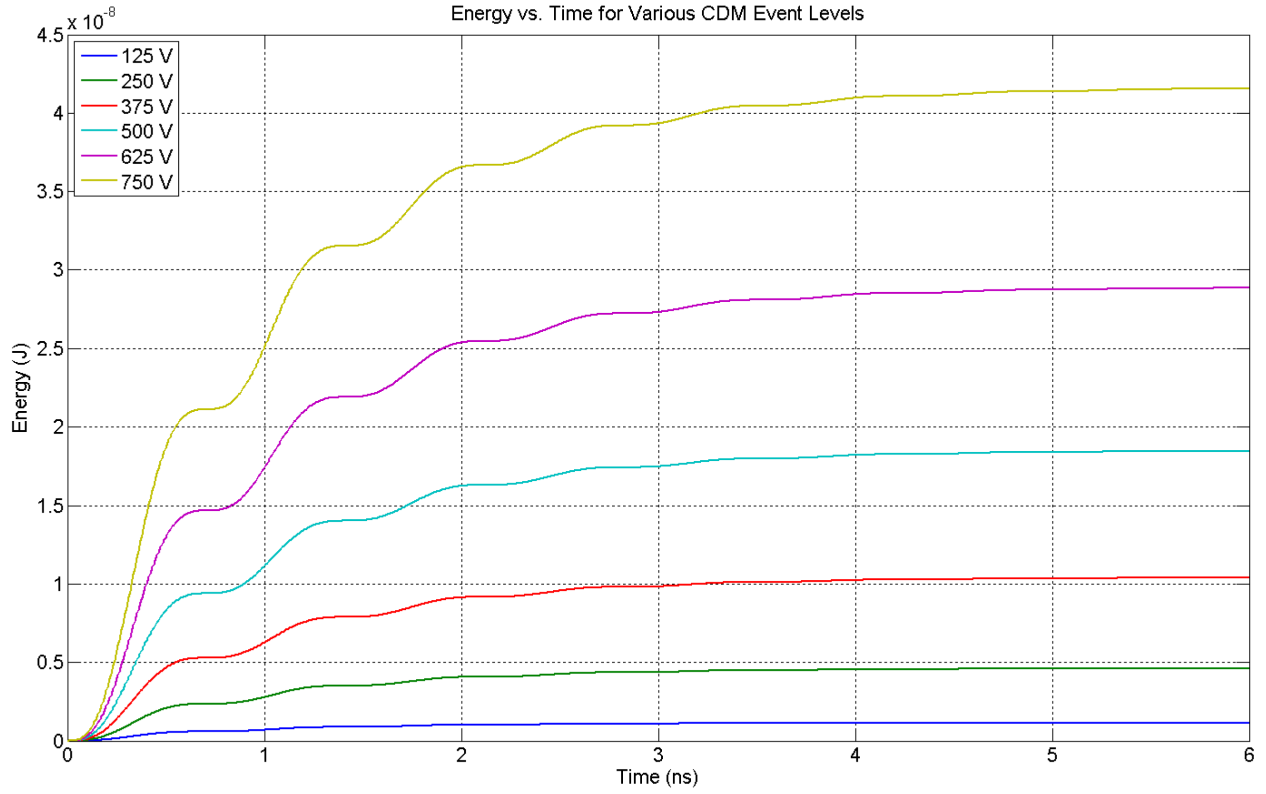

Figure 5.13 CDM energy vs. time

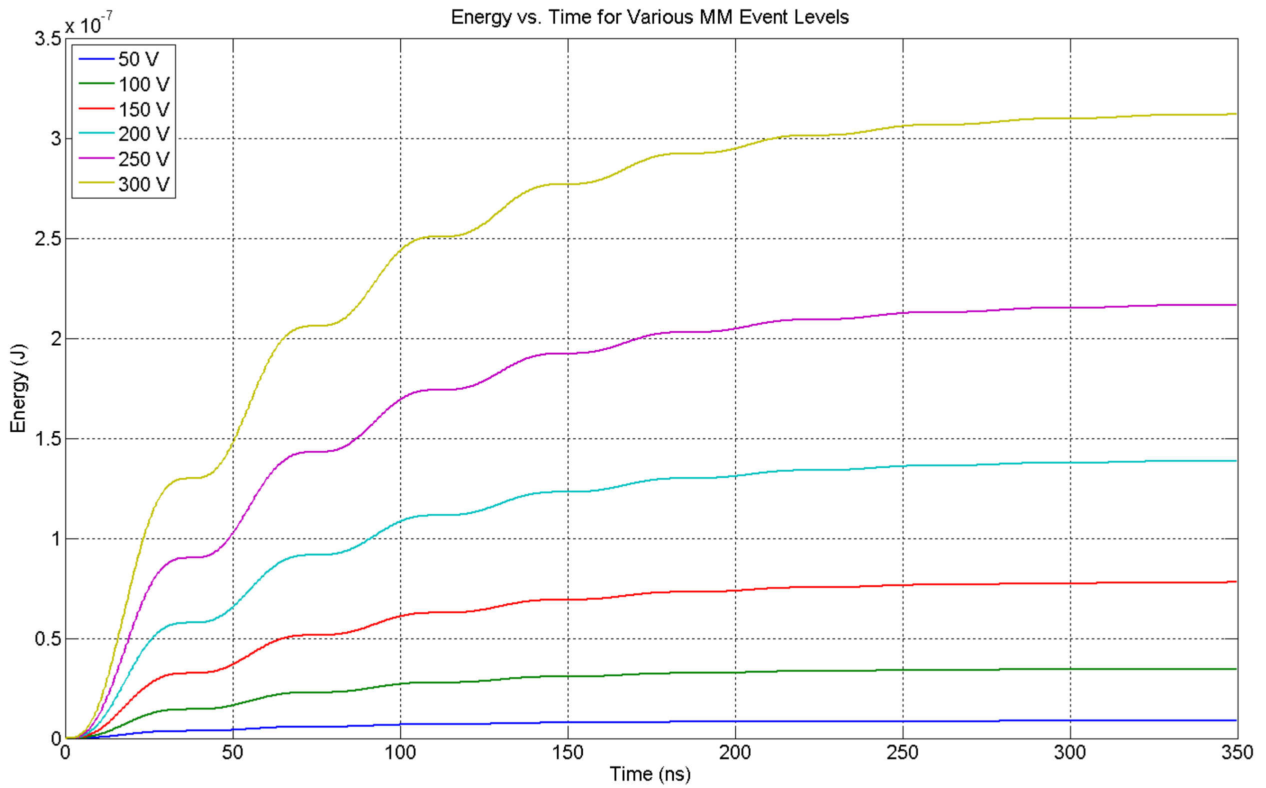

Figure 5.14 MM energy vs. time

5.3.4 Fuse State Changes during an ESD Event

In the proposed BIST for ESD system presented in Figure 4.2, the fuse is integrated with the ESD protection scheme. When the IC is hit by an ESD event, the fuse offers the path of least resistance and initially takes the full brunt of the event. The energy from the event heats up the fuse, breaking the fuse and creating an open circuit. After the break, the ESD protection circuitry becomes the primary discharge path for the remaining event current.

ESD detection circuitry is useful and reliable as long as an ESD event has enough energy to break the fuse. Figures 5.15, 5.16, and 5.17 show fuse state change plots for each ESD type, constructed by dividing the energy plots by the weight of the 7.02 pg fuse. The state change plots can be used to predict the circumstances under which a fuse breaks. In order for the fuse to fail, it should at least reach its melting point, marked in the plots by a blue dashed line. The red dashed line indicates the vaporization point of the fuse.

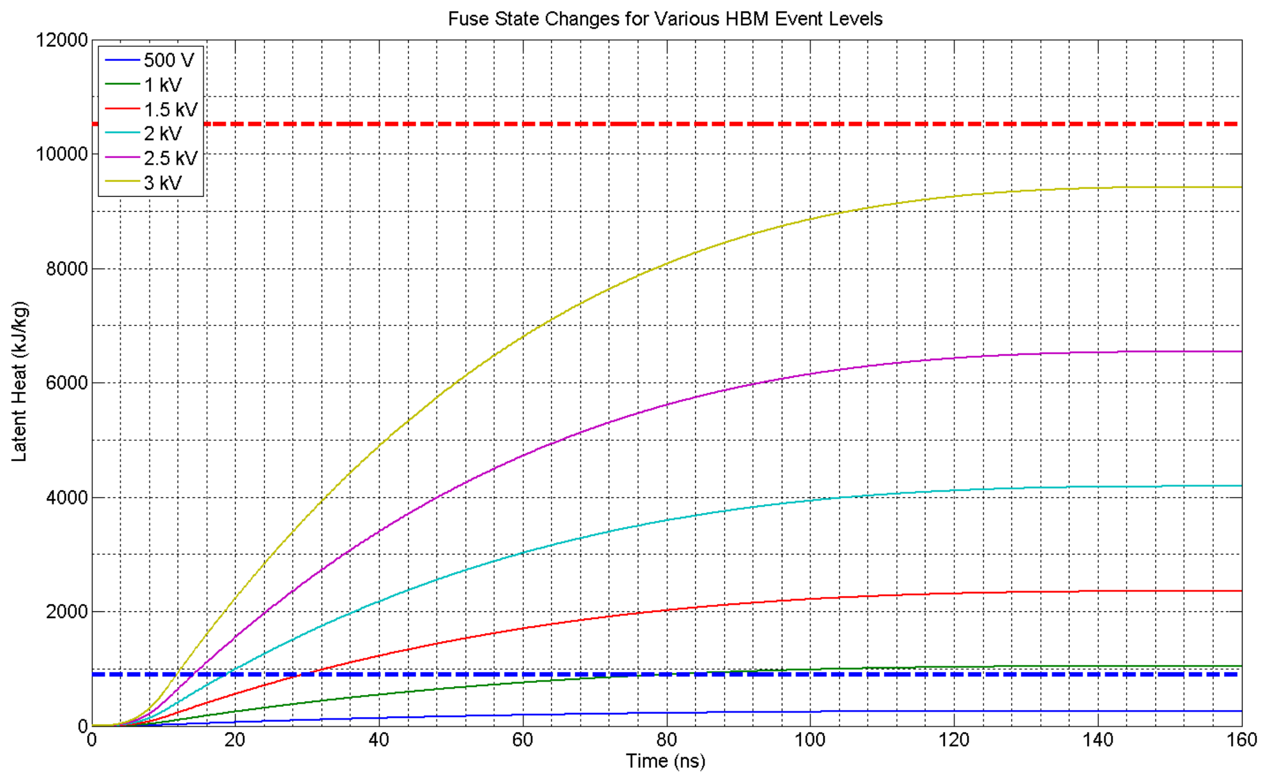

Figure 5.15 Fuse state changes during an HBM event

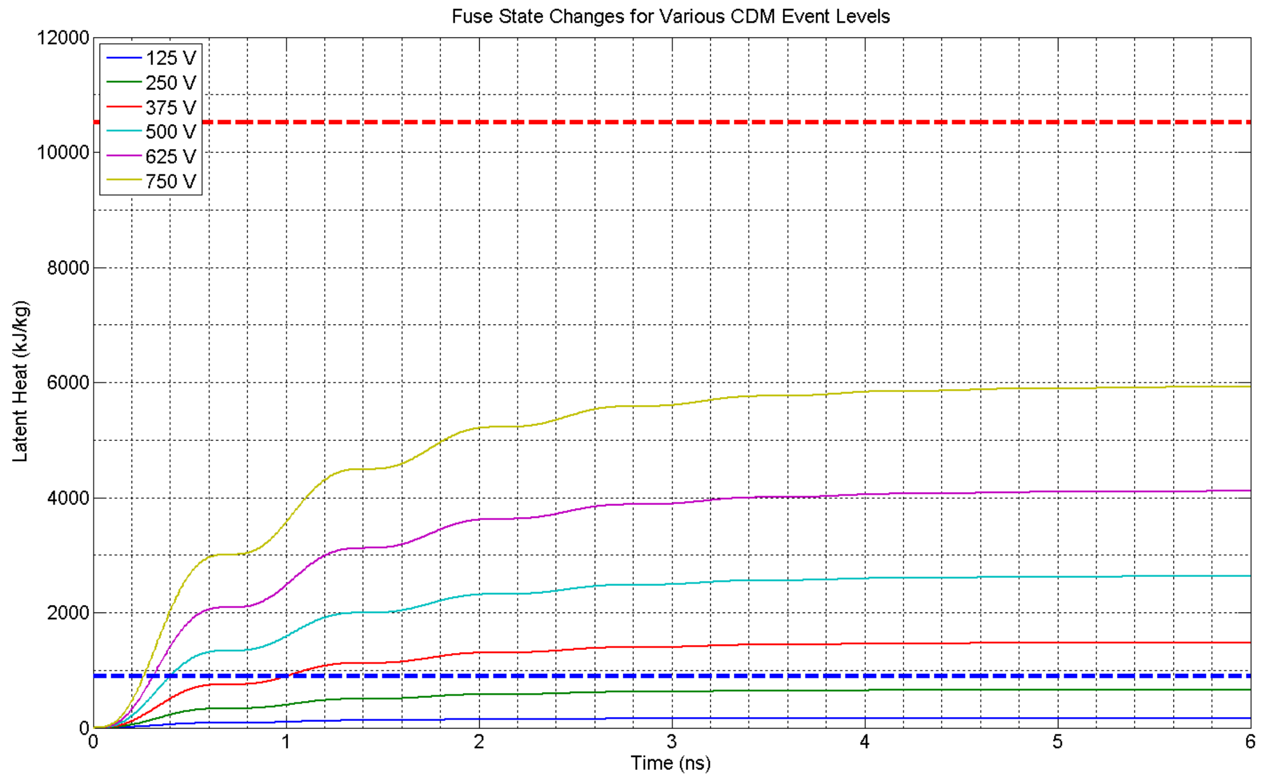

Figure 5.16 Fuse state changes during a CDM event

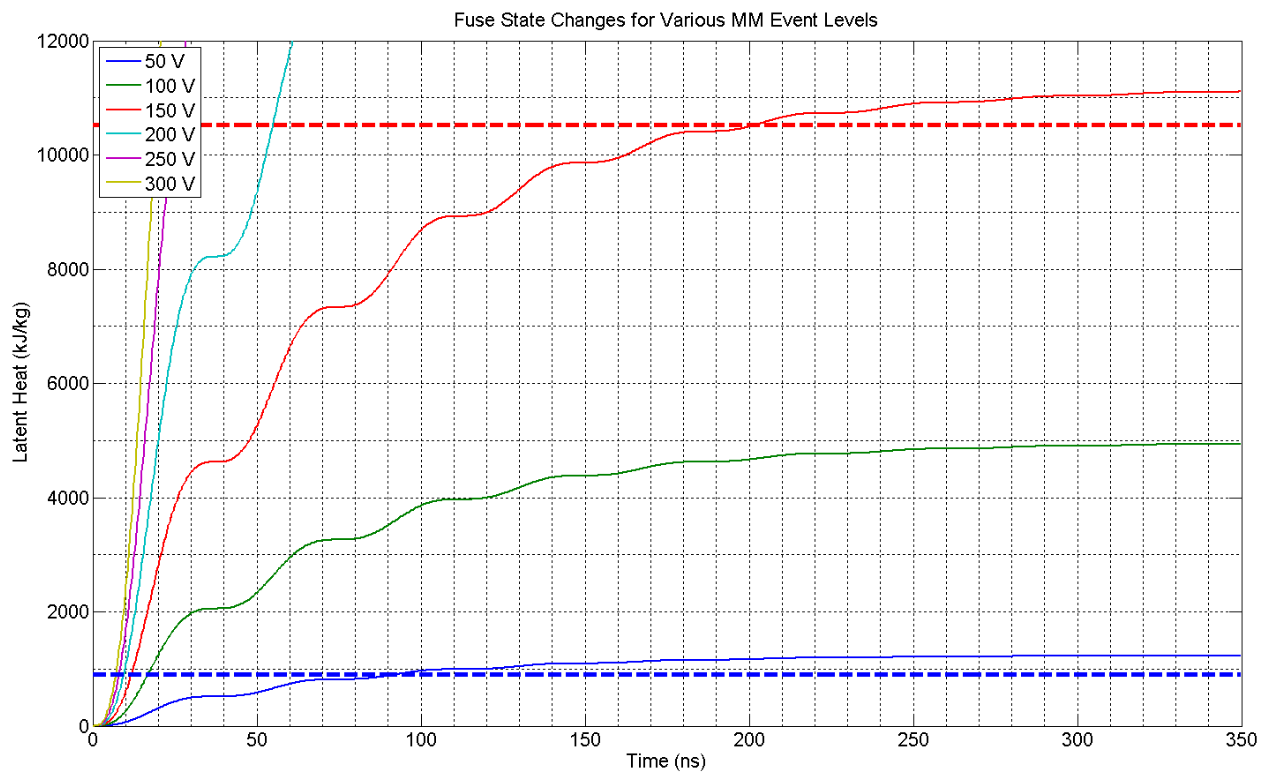

Figure 5.17 Fuse state changes during an MM event

The fuse reaches its melting point for nearly every scenario, leaving only the lowest ESD levels unable to melt the fuse. A system implementing IC fuses must decide whether the ESD detection circuitry needs to be able to detect the full range of ESD events. If so, the size of the fuse can be reduced to make it more sensitive to ESD events.

Ordinarily, melting a fuse would be sufficient for a permanent break. When built into an IC, however, the fuse metal has less room to flow once it melts. It may instead re-solidify such that it maintains a continuous metal trace. If this happens, the detection circuitry has no way of knowing if there has been an ESD event. A fuse vaporizing would likely be a more permanent event, but it could be an unnecessary requirement. To determine if reaching the melting point is sufficient for breaking a fuse, the next section measures fuse response to ESD events.

5.4 IC Fuse Measurements

From the calculations performed, the IC fuses should melt given the 1 kV HBM event used in the measurement setup. Actually testing them in this scenario determines if this ESD level is powerful enough to break the fuse and keep it broken. If not, the fuse may re-solidify and maintain a short circuit. Figure 5.18 shows a screen capture of a fuse breaking. Unfortunately, the same ringing problem that affected the clamp measurements limits the reliability of this measurement. If the pulse is ringing, the pulse is no longer a true HBM event.

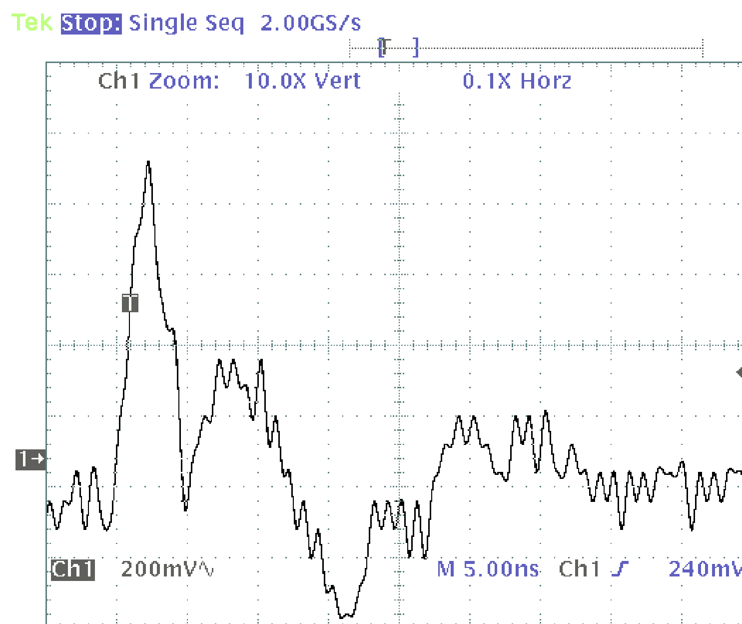

Figure 5.18 Plot of an IC fuse breaking

The sharp rise at the beginning of the event is expected. A voltage drop should develop due to the resistance of the wires running to the fuse and the fuse itself. The voltage should continue to rise as more current flows through the fuse, heating up the fuse and increasing its resistance. When the fuse acquires enough heat to reach its melting point, the flow of metal breaks the connection between one end of the metal and the other. Once an open circuit is created, the voltage should remain constant across the fuse because there is no longer a discharge path. However, Figure 5.18 shows the voltage staying close to zero after the initial event. Looking at a longer time frame, as shown in Figure 5.19, the ringing problem is more apparent.

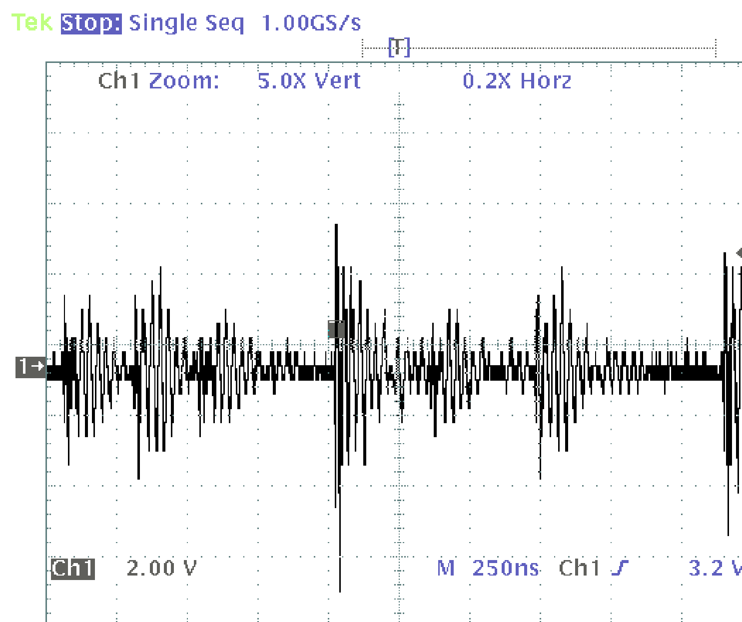

Figure 5.19 Longer time sample showing the breaking of a fuse

The oscillations display pulsing behavior, with each oscillation cycle lasting approximately 250 ns, which is nearly identical to the time of the HBM event shown in Figure 4.3. Perhaps Figure 5.19 is showing the HBM event ringing down the line, but the non-periodic behavior of the pulsations suggests that that conclusion is tenuous at best. Whatever the source of the oscillations, the next measurement setup developed will have to solve the issue to determine the true nature of the voltage across a failing fuse.

5.5 Transmission Line Pulse Measurements

A transmission line pulse (TLP) setup provides a potential alternative to the ESD measurement setup discussed thus far. The goal of a TLP setup, shown in Figure 4.20, is to replicate the energy of an HBM event with a uniform pulse [17]. Whereas an HBM event consists of a sharp voltage spike that tapers off with time, a TLP is a simple square pulse. A correctly implemented TLP pulse uses the same current levels as an HBM event, but at a much lower voltage level. While the HBM is a more accurate representation of the current discharge from a human to an IC, a TLP is a predictable pulse that is easier to measure.

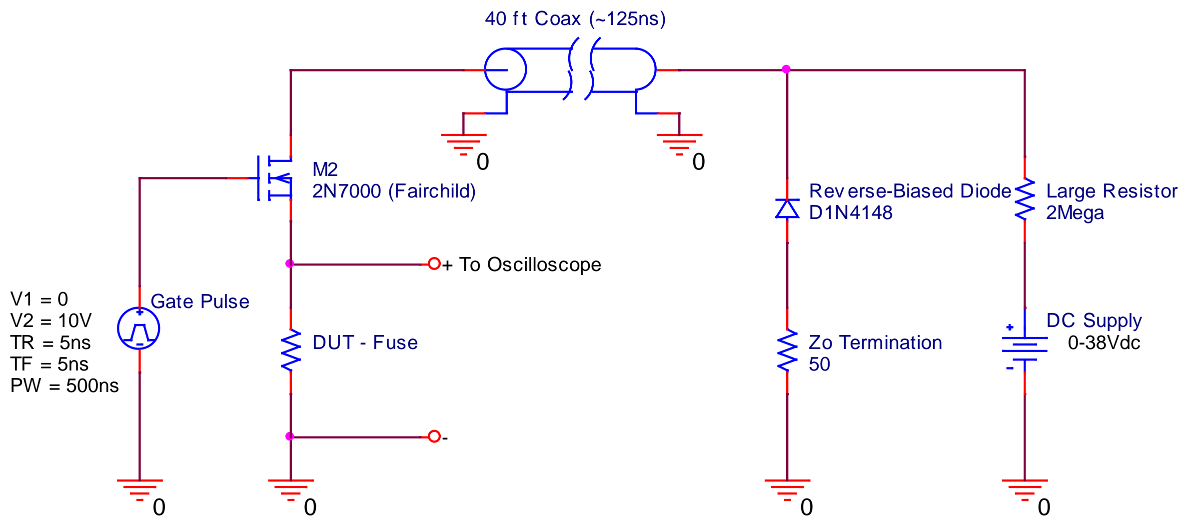

Figure 5.20 TLP measurement setup

The TLP setup in Figure 5.20 is controlled by M2, which operates as a switch controlled by a signal generator set to output a 10 V, 500 ns pulse at the push of a button. With M2 off, the DC supply can charge the 40 foot coax cable. Turning on M2 releases the coax's charge into the DUT. Distributing the capacitance over the length of the cable allows the coax to discharge in a uniform manner, with a pulse width dependent on the length of the cable and a voltage level determined by the DC supply [10]. For this circuit, the 40 foot coax produces a pulse approximately 125 ns in duration.

An advantage of using the TLP setup is that it maintains a 50 Ω system; as long as all connections have a 50 Ω termination, there should be no ringing. The lack of ringing is demonstrated in Figure 5.2, which shows a TLP measured across an IC fuse. The TLP voltage for this measurement was only 15 V, which did not provide enough energy to break the fuse.

This measurement also shows that the fuse resistance is far less than the 50 Ω source impedance created by the coax's characteristic impedance, as only 1.25 V drops across the fuse.

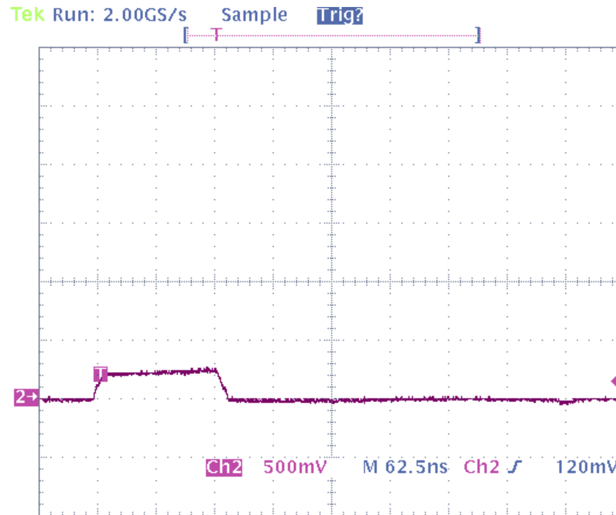

Figure 5.21 15 V transmission line pulse (vertical scale is 2.5 V/div due to 5:1 probe)

As discussed in Section 4.3, fuse heating is a major concern for the proposed ESD detection circuit. The measurement in Figure 5.22 illustrates the problem. This time, the TLP level is 30 V. Rather than having a voltage twice as high as in Figure 5.21, the fuse voltage continues to rise throughout the TLP. Because TLP voltage and current is constant, this confirms that the fuse experiences a rapid increase in resistance due to heating. This could pose a problem for the ESD detection circuit if the fuse does not break before an increase in resistance allows the ESD protection circuitry to turn on.

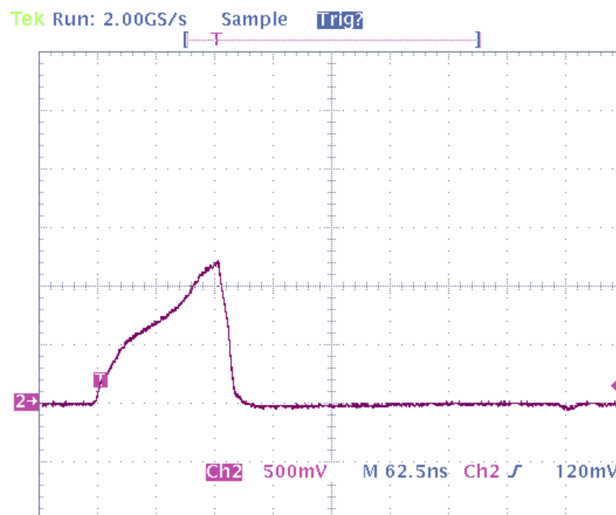

Figure 5.22 30 V transmission line pulse (vertical scale is 2.5 V/div due to 5:1 probe)

Figure 5.23 provides an example of a breaking fuse. In this measurement, the coax was charged to 38 V. From the measurement, it is apparent that the fuse experienced very rapid heating and then it appears that the circuit rings as before. This is not the case. Rather, it shows that the fuse did indeed break. With a TLP setup, this apparent ringing is beneficial – and desired – as it indicates that the fuse broke. When the fuse breaks, it also breaks the 50 Ω system, creating 125 ns reflections between either ends of the coax. The reflections continue until M2 turns off. Not only does this plot show that the fuse broke, it also shows that the fuse likely broke during the initial spike. This result is encouraging because the fuse needs to break very quickly before the ESD protection circuitry draws too much current. The faster the fuse breaks, the better chance it has of working in the proposed ESD detection circuit.

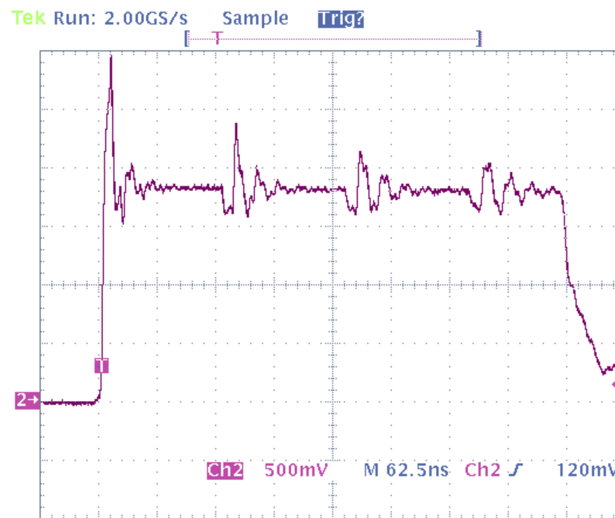

Figure 5.23 Fuse breaking using a 38 V TLP (vertical scale is 2.5 V/div due to 5:1 probe)

Finally, a flaw with this TLP setup is in the way M2 is configured in a common drain configuration. In this configuration, the voltage at the source can be no higher than the gate, except for transient effects such as the spike seen at the leading edge in Figure 5.23. It is believed that drain to source capacitive parasitics allowed this spike to occur. With a signal generator limit of 10 V, this setup prevents the fuse from experiencing more than approximately 8 V. Figure 5.24 highlights this problem, showing the voltage rising steadily before stopping suddenly at 7.5 V. By limiting the voltage on the DUT, this setup does not allow it to experience the full extent of the TLP. A future TLP setup should explore the use of relays in place of a FET.

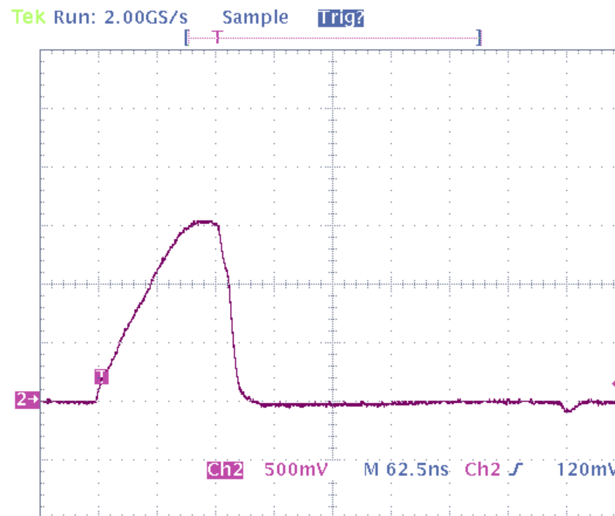

Figure 5.24 TLP measurement showing voltage limiting problem (vertical scale is 2.5 V/div due to 5:1 probe)

Regardless of the shortcomings experienced while performing the IC fuse measurements presented in this section as well as the last, low resistance fuses below 5 Ω reliably broke when hit with either a 1 kV HBM event or 38 V TLP. Stacked via fuses were especially vulnerable to ESD events. In contrast to the fuse diagram shown in Figure 5.5, a stacked via fuse uses vias to change metal layers at their midpoint. By utilizing vias, it is believed that the fuse metal has more room to flow when it melts, reducing the likelihood of the fuse re-solidifying. The measurements performed on IC fuses suggest that they show the potential to be integrated into an ESD protection scheme along with the ESD detection circuitry needed to identify a broken fuse. With more circuitry to determine which pads have broken fuses, a BIST can be implemented to easily determine whether or not an IC has been compromised by ESD.

Chapter 6 - Conclusions and Future Work

The goal of this research was to provide a background of the three main types of ESD and discuss methods of mitigating and detecting an ESD event in an IC. Choosing an ESD pad circuit topology consisting of two protection diodes and a voltage clamp, the research then explored the process taken to design and optimize an ESD pad circuit. Previous ESD detection methods were discussed, and a new ESD detection method based on IC fuses was proposed. Finally, voltage clamps and IC fuses were measured for their responses to an ESD event.

6.1 Regarding ESD Pad Optimization

This research began with an analysis of the three main types of ESD and how ESD protection circuitry handles each type. A few alternative ESD pad design approaches were explored before deciding to use an ESD-transient triggered clamp in circuits. This type of clamp is easier to design than a gate-grounded clamp, limits voltage better, and offers an added benefit of being relatively process-independent.

From a topology consisting of two protection diodes and a voltage clamp, the first ESD pad was designed and simulated. From these simulations, it was determined that the protection diodes could be made larger to handle large ESD event current and the voltage clamp could be altered to produce faster turn-on times. The proposed design presented in Figure 3.40 divides each protection diode into 80 smaller 2 µm x 2 µm diodes connected in parallel, dramatically increasing the overall size and junction area of the protection diodes. The proposed design increases the size of the clamp's driver FET to allow for faster switching time. The final design provides a high level of ESD protection considering the small process dimensions. It accomplishes this level of protection while remaining small enough to be used in conjunction with 2.4 GHz circuitry.

Future work should focus on laying out the proposed design. The large number of parallel diodes should allow for a great deal of flexibility when making the layout. Whereas this research focused on designing an optimized ESD pad, it is recommended that further design work focus on creating an ESD protection scheme that encompasses the entire pad frame. A plan needs to be in place to provide sufficient protection for the inner circuitry without consuming too much area on the chip. For example, instead of having a clamp next to each pad,

a clamp could only be used in coordination with VDD and ground pads. This would free up space near I/O pads, which require a connection to two protection diodes. Designing an entire pad frame would require an analysis of the inductances along the VDD and ground lines between each pad. As Section 3.2.1 demonstrated, inductance along a discharge path greatly degrades the performance of ESD protection circuitry by resisting any sudden change in current. A pad frame design would have to ensure sufficient protection at every pad.

6.2 Regarding ESD Detection and BIST

An ESD detection method was explored that, while effective in its ability to detect ESD events, cannot detect events that occur without power or during production. A proposed method which requires no power to operate is introduced based on IC fuses designed to break when an ESD event occurs. After connecting the IC to a power supply, extra circuitry would determine whether the fuses have been broken.

Combining the proposed detection circuit with the optimized protection circuit would allow for the creation of a BIST for ESD system. In such a system, each pad would have a fuse integrated into the protection circuitry with ESD detection circuitry designed to recognize a broken fuse. A BIST for ESD would query each pad to determine which pads, if any, have been potentially compromised by an ESD event.

Future work should involve determining which passive device can be used in this system. If IC fuses will not break reliably in the proposed circuit due to current diverting through the protection circuitry, perhaps an anti-fuse, or oxide-based device, can be used. Rather than becoming an open circuit, an anti-fuse would short circuit under ESD stress. Being oxide-based, the device would fail due to voltage levels rather than current levels. After choosing the device, the ESD detection circuitry and BIST system should be implemented.

6.3 Regarding ESD Measurements

This research explored methods of measuring ESD events to validate simulations and ESD pad designs. Establishing an effective method proved a difficult task. Several issues were encountered throughout the entire measurement process. Some issues, such as protecting the oscilloscope from high voltage, had simple solutions: use a high voltage probe or divide the voltage down before measuring with a probe.

Other issues were not easy to fix. The setup continues to display oscillatory behavior, rendering an HBM measurement to be more reminiscent of an MM event. Every wire in the setup has been minimized to reduce ringing due to parasitic inductance, even foregoing the use of the long coax connected to the probing structure. Instead, short copper ribbons are connected to the outer conductors of two probes. Future work on an ESD measurement setup should conclusively determine the source of the ringing and work to eliminate this ringing from the measurements. Despite all of the problems, the voltage clamp did function and, from what is observable, it functioned well. Using an ESD measurement setup free from ringing will likely produce results that closely match those seen in simulation.

6.4 Regarding IC Fuses

Future work should continue to test fuses after fixes are made to the current ESD measurement setup. Most of the current fuse prototypes are believed to be too large. It is recommended that fuses be no larger than 7 pg in order to ensure reliable operation. Fuses made using a stack of vias performed well during testing. More exploration into this type of fuse is encouraged.

From calculations, most ESD levels will cause an IC fuse to melt and break given the amount of energy involved. Though measurements were not able to show a clean plot of a fuse breaking, low resistance fuses under 5 Ω broke reliably when hit with a single 1 kV HBM event. TLP measurements provided a setup free from ringing, which allowed fuse heating and fuse breaking to be observed. A future TLP setup should substitute a relay for the switching FET. That the fuses broke reliably with both the ESD measurement setup and the TLP setup indicates that IC fuses show the potential to be used in an ESD detection circuit.

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