A CURRENT LIMIT CONTROL
FOR A CHOPPER-FED D-C MOTOR
BY USING A KIM-1 MICROCOMPUTER

by

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B.S., Tamkang College, Taiwan, 1976

A MASTER'S THESIS

submitted in partial fulfillment of the
requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering
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Manhattan, Kansas
1982

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CHAPTER 1

INTRODUCTION

Since its discovery the thyristor has been widely used in motor control. Also the tremendous progress in semiconductor memory such as ROMs and EPROMs has broadened the application of the microcomputer in industrial control.

This paper discusses a digital system which uses a KIM-1 microcomputer to provide control signals to turn the thyristors' on and off. In that way the current in motor can be limited and the rotational direction of motor can be changed.

Figure 1 illustrates a motor current controller to be used in a feedback control system. The primary thyristors SCR₁ and SCR₄ are turned on and motor rotates in a certain direction. On start, however, if SCR₁ stays on current in motor M will be excessive. In order to limit the current in the motor, SCR₁ must be turned off and on periodically. The current pulses to motor M through SCR₁ are illustrated in Figure 2. In this figure the average current is determined by \( \alpha \) where \( 0 < \alpha < 1 \). At \( \alpha T \) SCR₁ is turned off and current to the motor M is interrupted according to chopping signal that intends to limit the motor current.

To reverse the motor direction SCR₁ and SCR₄ are turned off and SCR₂ and SCR₃ are turned on, and SCR₂ now plays the same role as SCR₁ did above. Thyristor SCR₃ acts the same capacity as SCR₄.
The microcomputer control system requires construction. In response to current limit signals and direction signal, the microcomputer provides appropriate signals to turn the primary thyristors on and off. These signals are controlled by a program stored in the microcomputer's RAMs and are sent to thyristor triggering circuits and provide trigger pulses to SCR's gates.

Fig. 1  MOTOR WITH CURRENT LIMITER.
Fig. 2 (a) PULSE TRAINS USED TO TURN ON THE THYRISTORS.
(b) IDEAL OUTPUT WAVEFORMS OF SCR CHOPPER.
CHAPTER 2

KIM-1 MICROCOMPUTER

2.1 General description:

Since the development of the INTEL 8008 there have been many microcomputer designs produced. In this decade the microcomputer has had a dramatic influence on the engineering world, especially on the area of automatic control. In the motor current limiter system a KIM-1 microcomputer is used.

At the heart of the KIM-1 microcomputer is an MCS 6502 microprocessor operating with two MCS 6530 arrays. The MCS 6530 is a memory/peripheral device used to store the KIM-1 operating program and provide input/output ports to communicate with the outside world. All of these chips and other supporting components such as RAM chips, a crystal, a keyboard/display panel, resistors and capacitors and logic gates are mounted on a printed circuit board. Based on the MCS 6502, KIM-1 is a byte-operated microcomputer (Ref. 6, Ref. 7).

The MCS 6502 provides a full 16-bit address bus and thus the KIM-1 can support up to 64K memory locations in the system. An 8-bit bidirectional data bus carries data between the 6502 array and any memory location. A control bus carries timing and other control signals between the 6502 array and other system elements. The 1 MHz crystal oscillator either generates the basic timing signal used by the 6502 array alone, or gated with other control signals for all other system elements.

The two MCS 6530 arrays are labelled as 6530-002 and 6530-003. Each of the 6530 arrays includes a 1024 byte ROM (Read Only Memory)
array storing the KIM-1 operating program. Each 6530 array also
provides 15 I/O pins (Input/Output pins). The 6530-002's I/O pins are
used to interface with the keyboard, display, TTY, and the audio tape
recorder. The 15 I/O pins on the 6530-003 are brought to a connector
and are available for the user to control a specific application. In
the present system the lower 7 bits of port A of 6530-003 are defined
as output pins to interface with a programmable counter. The most
significant bit works as an input pin to interface with a toggle switch
which is used to select the desired current value. Port B has seven
I/O pins: four of which, PB0 - PB3, are used as output pins for four
output ignition pulses to the thyristor triggering circuits. PB4 and
PB5 are input pins to synchronize the microcomputer with hardware logic
control circuits and PB7 is an input pin interface with a toggle switch
which controls the direction of motor rotation. The data bus and
address bus are also brought to another connector on the KIM-1 printed
circuit board for expanding the I/O system or memory space.

2.2 MCS 6530:

The MCS 6530 is comprised of a mask programmable 1024 x 8 ROM
array, a 64 x 8 RAM array, two 8-bit bidirectional ports, and a
programmable interval timer with interrupt. The programmable ROMs in
the two MCS 6530 chips of KIM-1 system store the KIM-1 executive
programs. The two I/O ports are defined by data direction registers
-DDR). The DDR controls the peripheral output buffer. A "1" written
into the DDR sets up the corresponding peripheral buffer as an output
buffer. A "0" written into the DDR will allow the microcomputer to
read the peripheral pin.
2.3 I/O port expansion:

There are only two I/O ports provided by the 6530-003 chip available for interfacing with the outside world. The present current limit system needs two more I/O ports to interface with two A/D converters. Also required are handshake signals between the microcomputer and the A/D converter, i.e., the KIM-1 microcomputer tells the A/D converter when to start the analog-to-digital conversion and at the end of the conversion the A/D converter signals the microcomputer that the digital voltage is ready. Each port provides one peripheral control line and one interrupt request input line to communicate with an A/D converter. An MC 6821 Peripheral Interface Adapter (PIA) can meet all requirements to provide two input ports in which each port offers eight input data lines, one interrupt request line, and one output control line. In this control system two National Semiconductor ADC0809 analog-to-digital converters are used for conversion.

The ADC0809 is a monolithic CMOS device with an 8-bit output analog-to-digital converter. It has an 8-channel multiplexer and microcomputer compatible control logic. The 8-channel multiplexer can directly access any one of 8-single-ended analog signals. The device uses a single 5 volt power supply and any voltage of 8 analog inputs that may be in the range of $-0.3V$ to $V_{cc}+0.3V$.

The interface between the MC 6821 and the ADC0809 A/D converter is shown in Figure 3. The handshake between these two devices is described below. The two output control lines CA2 and CB2 on PIA will send a high-to-low signal, a conversion beginning command, to the START pin on each A/D converter. Three address pins ADD$_A$, ADD$_B$, and ADD$_C$ on
each A/D converter are all grounded so that the converter begins to
convert the analog voltage on input pin INo. The conversion will take
about 100 micro-seconds. A low-to-high END-OF-CONVERSION signal will
be sent out of EOC pin on converter to the interrupt request input line
CAI or CBI on PIA to tell the microcomputer that the digital voltage
is ready. The two 8-bit unsigned binary digital numbers are provided
on eight TRI-STATE output pins of each converter, 2^-8 (LSB) to 2^-1 (MSB),
to be transmitted to KIM-1 through two input ports of the PIA.

The detail of interface connections between the PIA and the KIM-1
system is shown in Figure 4. A ribbon cable carries all control
signals and data between the PIA and KIM-1 system. Register select
pins RS0 and RS1 on the PIA are brought to E-A and E-B. E designates
expansion connector on the KIM-1 system. Chip select pins CS0 and
CS1 are connected to VCC. Another chip select pin CS2 is brought to C
pin of the application connector (designated A) on the KIM-1 module.
K1, A-C pin, is an output pin of an address decoder included on the
KIM-1 module defining a 1K block of memory addresses from $0400 to
$07FF ($ means hexadecimal number). A 680Ω pull-up resistor is
necessary to supply suitable bias for K1 pin. This kind of connection
of register selects and chip selects will define the I/O ports' addresses as following:

DRA and DDRA $0400
CRA $0401
DRB and DDRB $0402
CRB $0403

where DR means data register, DDR means data direction register, and CR
represents control register. The Interrupt Request lines (IRQA and IRQB) of MC 6821 are active low lines. A 3 KΩ external resistor should be used for proper wire-OR interrupt operation.

This Motorola PIA MC 6821 provides two 8-bit bidirectional data buses for interfacing with peripheral devices. Each data line of these two I/O ports can be programmed to act either as an input line or as an output line by the data direction register. A DDR bit set at "0" configures the corresponding peripheral data line as an input line; a "1" will result in an output line. A "0" on bit-2 of each control register will select the corresponding data direction register; a "1" will select data register. The two control lines of each port are programmed by the control register (Ref. 8). CA1 and CB1 are input only lines that set the interrupt flags of the control register. However, CA2 and CB2 can be programmed to act as interrupt inputs or as peripheral control outputs. The detail of modification of the control register is described in hardware manual of the M6800 microcomputer. Actually this Motorola product is identical to the MCS 6520 of Technology, Inc.
Fig. 3 INTERFACE OF PIA AND A/D CONVERTERS.
Fig. 4 INTERFACE OF PIA AND KIM-1 system.
CHAPTER 3

CHOPPER CIRCUIT

3.1 Introduction:

The thyristor chopper now is very popularly used in the control of d-c motors. In such a system thyristors are used to control the motor current. A problem with such an application is associated with the turn-off of the primary thyristor. Following are some discussions of some conventional choppers and a chopper called Activated Commutation Chopper (Ref. 1, Ref. 4) being used in the motor current limit system.

3.2 Conventional choppers:

There are a variety of conventional circuits used in choppers. In most of these the turn-off of the primary thyristor is accomplished by using a commutation capacitor which is charged in a series resonant circuit and is capable of providing a reverse bias for the primary thyristor. Two of the most popular circuits (Ref. 1, Ref. 5) are shown in Figure 5.

In these circuits the energy provided by the commutation capacitor must be sufficient to cause the current of the primary thyristor to be reduced to a value less than its holding current and keep it there longer than the Off-time of the primary thyristor so that it may turn off. In these circuits when the commutation of the primary thyristor fails there is no means to recharge the commutation capacitor.

3.3 Activated commutation chopper:

In order to ensure the successful commutation of the primary thyristor the circuit called Activated Commutation Chopper (Ref. 1,
Fig. 5 CONVENTIONAL CHOPPERS
(a) JONES CHOPPER
(b) PARALLEL-CAPACITOR COMMUTATED THYRISTOR CHOPPER.
Ref. 4) is proposed in this motor current limit system as shown in Figure 6. This circuit can drive the motor in both directions. In this diagram SCR₁ and SCR₄ are the primary thyristors carrying the load current which drives the motor in one direction, while SCR₂ and SCR₃ are the other pair of primary thyristors for driving the motor in opposite direction. SCR₅ is the secondary thyristor for turning off SCR₁ and SCR₄. SCR₆ is used to turn off SCR₂ and SCR₃. C₁ and C₂ are commutation capacitors. e₁ and e₂ are used to charge C₁ and C₂ and are voltages provided by two output windings of an independent source, an inverter.

At the start of the load cycle SCR₁ and SCR₄ are fired on and e₁ will charge C₁ through the path D₅ and SCR₁ to the peak-to-peak output voltage of e₁ with dotted plate positive. The load current now flows through SCR₁, motor M, reference resistor R, and SCR₄. When SCR₅ is turned on at ϑₐ, SCR₁ is turned off by the reverse bias provided by the commutation capacitor C₁ and C₁ now starts to discharge. After the capacitor voltage of C₁ reaches zero, it will be recharged with another plate positive by load current through the path of the secondary thyristor SCR₅. SCR₅ will turn off automatically and load current circulates through SCR₄ and the free-wheeling diode D₃ then drops to zero.

In this circuit four pulse transformers are used to turn on those thyristors. Each pulse transformer has one primary winding and two output windings. When a voltage pulse appears on the primary winding, a pulse is sent to the gate of the coupled tryristor of the corresponding output winding and that thyristor is turned on. In this way SCR₁ and SCR₄ can be turned on at the same time. The pulse being
Fig. 6 ACTIVATED COMMUTATION CHOPPER FOR MOTOR CURRENT LIMITER.
sent to the primary winding of pulse transformer is controlled by some logic control circuits and the microcomputer through triggering circuits as shown in Figure 7.

Fig. 7  THYRISTOR TRIGGERING CIRCUIT.
4.1 Introduction:

The thyristor must be triggered at the time they should be on. The triggering circuits are controlled by hardware logic control circuits and software programs stored in the microcomputer's RAMs. The combined hardware and software controller will generate pulse trains for triggering the circuits. The hardware logic control circuits are discussed in this chapter.

4.2 Overview of logic control:

The block diagram of logic control circuits for producing turn-on pulses using programmable counters is shown in Figure 8. The astable oscillator, shown in Figure 9, is composed of two NOR gates (Ref. 2) and is the basic pulse source from which all the necessary pulse trains are derived as shown in block diagram of Figure 8.

Pulse train e₁ periodically turns on SCR₁ and SCR₄. These in turn apply power to the controlled motor such that the motor rotates in a certain direction. The commutation capacitor C₁ may now be charged. The second pulse train e₂ turns on the secondary thyristor SCR₅ which in turn commutates the primary thyristor SCR₁. In order to reverse the rotation of the motor, e₃ is generated to turn on SCR₂ and SCR₃ periodically. A fourth pulse train e₄ turns on SCR₆ which in turn commutates SCR₂.

The amount of phase shift between e₁ and e₂, or e₃ and e₄ for reverse direction, is transmitted to pulse generator (programmable
counter) from an output port of the KIM-1 microcomputer in a form of binary number. The digitally controlled pulse generator can vary the phase difference up to 360 degrees at pulse frequency. In reference to Figure 8, the principle of logic control can be outlined as follows:

(1) Block \(2\) produces \(f_1\) which is sent to logic control block \(4\) and the microcomputer. Depending on the motor direction signal, the microcomputer will determine which one of \(e_1\) and \(e_3\) should be sent out to start the duty cycle.

(2) Block \(3\) provides \(f_2\) to logic control block \(4\) and the microcomputer. Whenever the microcomputer receives \(f_2\) according to motor direction signal, it will send out a pulse to turn on the secondary thyristor to commutate the primary thyristor.

(3) The reset and inhibition of programmable counter is controlled by block \(4\).

(4) The phase shift time between \(f_1\) and \(f_2\) is controlled by the microcomputer.

4.3 Programmable binary counter:

The programmable divide-by-\(N\) 4-bit binary counter MC 14526 is a down counter to provide the down counting mode. In this control system a 2-stage cascade connection is used. The programming is achieved by applying the preset variable to \(D_p\)'s input pins (Ref. 10) where the preset variable is determined by output of the KIM-1 microcomputer as illustrated in Figure 8. Block \(4\) of Figure 8 will send an initiation signal to make MR, Master Reset, go low to start the count-down process.

The chopper frequency is determined by the output frequency of
Fig. 8 LOGIC CONTROL FUNCTION.
clock ① and the 7-bit binary counter ②. The output frequency of clock ① in the present system is 12700 Hz. Block ② will send a pulse $f_1$ every 127 pulses of clock ①. Thus each chopper cycle is divided into 127 time units. The amount of phase shift $\phi$ of $f_2$ after $f_1$ is given by

$$\phi = N \times \frac{360}{127} = N \times 2.83^\circ \quad (0 \leq N \leq 127)$$

where $N$, a positive integer, is the time unit number of duty cycle $\alpha$.

---

**Fig. 9** ASTABLE OSCILLATOR.
Fig. 10 INTERFACE OF PROGRAMMABLE BINARY COUNTER.
4.4 Reset and inhibit control:

The outputs of block 2 and 3, f₁ and f₂, go to both the KIM-1 microcomputer and the reset & inhibit control circuits. The KIM-1 microcomputer will use these two pulse trains as synchronous signals to send out negative pulses to triggering circuits to turn on the thyristors. However, the reset and inhibit control circuits use these two pulse trains to control the operation of the programmable binary counter (block 3, Figure 8). The detail circuit diagram of reset and inhibit control is shown in Figure 11 and those important input and output signals are shown in Figure 12. In this circuit CMOS integrated circuits are used. The advantage of using CMOS ICs is that these ICs can be coupled with each other without external pull-up resistors.

Reset and inhibit logic control block will make the potential on MR of programmable binary counter go to low whenever it receives a positive pulse, f₁, from the 7-bit binary counter's output pin "0". Low signal on MR will start the count-down process in the programmable binary counter. When the zero state is reached, this counter will send the potential on output pin "0" to high. This high signal to the reset and inhibit control circuit will make the potential on MR of programmable counter go to high. High potential on MR will reset the binary counter and inhibit its count-down process. In this way the microcomputer knows when to send out suitable ignition pulses to triggering circuits.

4.5 Summary:

The delay control circuit discussed above is highly flexible and has wide application in solid state power control. The firing period and the length of "ON" time of chopper are controlled by digital
processor. The digital control circuits and the microcomputer are isolated from the load and power circuits by using electro optical couplers to trigger thyristors' gates. In this way the expensive digital circuits and the microcomputer are protected from damage caused by unexpected feed-back voltage from load and power circuits. The resolution of this system can be made very high by increasing the number of binary counter IC chip and expanding the output port of the microcomputer.
Fig. 11  RESET AND INHIBIT CONTROL CIRCUITS.

FLIP-FLOP: MC 14027
NOR-GATE: MC 14001
INVERTER: MC 14049
Fig. 12 WAVEFORMS OF RESET AND INHIBIT CONTROL.
CHAPTER 5

AVERAGE LOAD CURRENT

5.1 Introduction:

In this current limit system, the average load current is compared with the desired average current. With reference to the error, the duty cycle \( \alpha \) (Fig. 2) is changed by the software program to adjust the current to the motor. This chapter describes the detail of a software program used to convert the voltage drop across a reference resistor (Fig. 3) into an average current in the motor.

5.2 Measurement of motor current:

Since the analog input voltage of the A/D converter must not exceed \( V_{CC} + 0.3 \) volts and the two reference voltages of the converter, \( \text{REF}(+) \) and \( \text{REF}(-) \), are \( V_{CC} (+5 \text{ volts}) \) and \( V_{SS} \) (ground) individually. The resistor network is used to drop the terminal voltage of reference resistor to a value less than or equal to \( V_{CC} \) before it is usable for the A/D converter as shown in Figure 3.

In the model constructed the d-c power source is limited to 30 volts. The two resistors \( R_1 \) and \( R_2 \) (Fig. 3) are 165 K\( \Omega \) and 33 K\( \Omega \) respectively. Those are used to lower the reference resistor voltage so that the input voltage of A/D converter will not exceed its limit.

5.3 Voltage-to-current subprogram:

The voltage drop on the reference resistor is sent to a subroutine program which will convert the voltage drop into the average current in the motor. Actually this subprogram includes two do-loops where each loop performs an 8-bit unsigned binary multiplication and an 8-bit
unsigned binary division.

In the primary thyristor's "ON" interval, chopper duty cycle $\alpha T$ of Figure 2, the motor current is given by

$$I_L = \frac{VDIFF}{R_L} \quad (1)$$

where $I_L$ = motor current = reference resistor current
$VDIFF$ = voltage drop across the reference resistor
$R_L$ = resistance of the reference resistor.

Immediately after the primary thyristor has been turned off the load current will decrease to zero rapidly. Thus the average current in the motor can be written as follows:

$$I_{av} = I_L \times \frac{\text{Unit}}{127} \quad (2)$$

where $I_{av}$ = average load current
Unit = number of time units of the primary thyristor's "ON" time
127 = each chopper cycle includes 127 time units.

$VDIFF$ is a hexadecimal number in the microcomputer stored at memory address $\$00C3$ and has maximum value of $\$FF$ (255 in decimal number) when the power source for the load circuit is its maximum value of 30 volts. Thus $I_{av}$ must be multiplied with a constant so that the analog voltage can be matched with the digital output of A/D converter. The calculation of this constant is discussed below.

The analog value of 30 volts equals to $\$FF$ after the conversion of the resistor network and the A/D converters. Thus, the constant $K'$ is

$$K' = \frac{30}{255} = \frac{2}{17} \quad (3)$$
The unit of $I_{av}$ is in amperes. When the desired current unit is set at 10 mAmp then $I_{av}$ has to be multiplied by 100. Hence the constant $K'$ becomes

$$K = \frac{2}{17} \times 100 = \frac{200}{17} = 12 = \$0B.$$  \hspace{1cm} (4)

Now $I_{av}$ is obtained by the subroutine program which makes the following calculation:

$$I_{av} = \frac{V_{DIFF} \times \text{Unit}}{127 \times R_L}$$  \hspace{1cm} (5)

where the unit of $I_{av}$ is 10 mAmp.

This software subroutine is listed step by step in Appendix B. It begins at address $0320$. The multiplication and division loops in this subroutine are suitable for unsigned numbers. Thus all numbers in this subroutine are considered as positive numbers although some of them may have a "1" at their most significant bit (sign bit for signed number). The flow chart of this subroutine is shown in Figure 13.

In the first multiplication loop the multiplicand and the multiplier are $V_{DIFF}$ and Unit respectively. As shown in the flow chart, the binary multiplication in the microcomputer is accomplished by shifting both the multiplier and the product left one bit. If the carry from shift of the multiplier is one, the product equals the sum of the product and the multiplicand; otherwise, the product keeps its value. In fact this is the same way to do a multiplication by hand.

After first multiplication loop, the product is a 2 byte long binary number. The higher order byte of the product works as the high byte of the dividend and the lower order byte of the product plays the
role of the low byte of the dividend in the next division loop. The divisor is 127 (the number of time unit of one chopper cycle). Like binary multiplication, the binary division in the microcomputer is the same way as the division performed by hand, i.e., using trial subtraction. If the divisor can be subtracted from the eight most significant bits of the dividend without a borrow, the corresponding bit in the quotient is 1; otherwise, it is 0. As shown in the flow chart this is accomplished by shifting left one bit then testing if the high byte of the dividend is greater than the divisor. The quotient must also be shifted so that it can line up properly with the dividend.

As shown in equation (5) the average current is obtained after two multiplications and two divisions are accomplished. The outer loop counter Y is set two. The quotient obtained from first division loop is the multiplicand in the second multiplication loop and constant K is the new multiplier. The resistance value of the reference resistor is the divisor for the second division loop.

The remainder of binary division will cause an error in the calculation of the current value. Compensation is made by adding one on the quotient of first division loop. The error on the second division loop can be reduced to a smaller range by using a smaller resistance value of reference resistor.

The last instruction, RTS, of this subprogram will bring the MPU of microcomputer back to main program. At this time the calculated average load current is stored in the accumulator A.
Fig. 13  FLOW CHART OF VOLTAGE-TO-CURRENT SUBPROGRAM.
Fig. 13  FLOW CHART OF VOLTAGE-TO-CURRENT SUBPROGRAM.
Fig. 13  FLOW CHART OF VOLTAGE-TO-CURRENT SUBPROGRAM.
(CONCLUDED)
CHAPTER 6

SYSTEM CONTROL PROGRAM

6.1 Concept of system control:

The functional block diagram of the proposed system is shown in Figure 15. It illustrates the configuration of the current limit control system. The system measures and corrects motor current at discrete level. The complete control cycle is described as a flow chart below.

![Flow Chart of Control Loop](image)

Fig. 14 FLOW CHART OF CONTROL LOOP.
The desired current value is stored in memory space of the microcomputer. The motor current value and rotational direction can be changed via toggle switches which are connected to I/O ports of the microcomputer. The average current applied to the motor is determined by the duty cycle ($\alpha$ in Fig. 2) which is a function of the relative displacement in phase of the "turn-on" and "turn-off" pulse trains. Based on the number of I/O ports of the KIM-1 microcomputer the system is limited to divide every chopper cycle into 127 time units. Each time unit represents a phase shift of $2.83^\circ$ relative to chopping frequency. The number of time units of the duty cycle is delivered to a programmable binary counter through an output port of the KIM-1 microcomputer.

The length of the duty cycle is adjusted according to the difference between the desired current value and the calculated value obtained from the voltage-to-current subprogram, named "MULT", discussed in Chapter 5. If the calculated value is smaller than the desired value, then the control program will adjust the firing time of the commutation thyristor, increasing the length of chopper's "ON" time, to supply more power to the motor. If the calculated value, on the other hand, is greater than the desired value, then the program will decrease the count of programmable binary counter's preset count value to move the firing pulse of commutation thyristor backward. This will decrease the power supplied to the motor.

Four I/O ports are used in this control system. The PIA MC 6821 provides two of these interfacing with two A/D converters where each port offers eight input data lines, one interrupt input line, and one peripheral control output line communicating with an A/D converter.
Fig. 15  Functional Block Diagram of Motor Current Control System.
The other two ports are provided by the 6530-003 of the KIM-1 system. The lower seven lines of port A are output lines for the use of time delay units of the primary thyristor's "OFF". The most significant bit is an input line for the current value select switch. The lower four lines of port B are reserved for outputs of ignition pulses of four trigger circuits. The other three are input lines for motor direction signal and two synchronous signals. Before these I/O ports are usable for the microcomputer, they must be well defined. The definition of I/O ports usually is placed in the first part of the program.

6.2 Initialization:

A data direction register bit set at "1" configures the corresponding data register bit as an output; an "0" results in and input. The data direction register and the data register of 6530-003 use different memory addresses. However, both data direction register and data register of MC 6821 use the same memory address. Thus bit-2 of control register of each port in MC 6821 is used to select either a DDR or DR.

Control lines of each port in MC 6821 are also defined by the corresponding control register. In this control system CA1 and CB1 must be defined to respond to low-to-high positive transition End-Of-Conversion signals to set an interrupt flag on bit-7 of their control registers. CA2 and CB2 are programmed as output lines to send out START (of conversion) signals to the A/D converters.

The A/D converter will begin the conversion on the falling edge of the START pulse. Hence control lines CA2 and CB2 are always high as long as bit-3 of CRA and CRB is high. This is accomplished by writing 111 into bit-3, bit-4, and bit-5 of the control registers. Whenever
the microcomputer wants the converter to start working, the program will write a "0" into bit-3 of control register, which will make a high-to-low negative transition, the falling edge of the START pulse, on CA2 or CB2.

6.3 Synchronous signal:

The turn-on of chopper is under control of a software program and must synchronize with the hardware control circuits. Hence the timing of the software program is very important. In some other control systems a software loop program may be used as a timer. In this system, however, the output pulse of 7-bit binary counter, block 2 in figure 8, works as a synchronous signal which will signal the microcomputer to turn on the primary thyristor. And this is the beginning of software control loop. Therefore the software program can synchronize with the hardware control circuits perfectly. The procedure of synchronization may be stated as follows:

The MPU of microcomputer reads the data on PB-5, bit-5 of port B of 6530-003, and test it until a "1", a positive pulse, appears on it at which time the MPU will execute the next instruction on the program; otherwise, the MPU will repeat this reading and testing loop as shown in the flow chart of figure 16. Therefore when the primary thyristors are turned on, the microcomputer will start its control job simultaneously.

The output pulse of programmable counter, block 3 of figure 8, is another synchronous signal to signal the microcomputer to turn on the secondary thyristor. This pulse will appear on PB-4.
6.4 Interrupt:

After the chopper is turned on to supply current to the controlled d-c motor, the MPU will write an "0" into CRA-3 and CRB-3 of control registers of PIA to make CA2 and CB2 low as START signals of conversion for converters. The program is in a time loop waiting for an interrupt request (End-Of-Conversion) which comes from the A/D converter. In response to the interrupt request appearing on CA1 or CB1, the MPU will jump to another subprogram where the starting address of this subprogram is preset at IRQ vector, $17FE for low byte and $17FF for high byte in the initialization part of this main program.

The major job of this interrupt request signal is to signal the microcomputer that the analog-to-digital conversion is done. The duty of the microcomputer in the interrupt subprogram is merely to clear the interrupt flags in the control registers. The last instruction of this subprogram is RTI (return from interrupt) which will bring the MPU back to main program to continue its unfinished work.

When the MPU reads data register of PIA the address line K1 and R/W signal (Fig. 3) will enable the TRI-STATE of A/D converter such that the digital data appears on output buffer which is connected to data register of PIA. After the conversion, CA2 and CB2 must be brought to high again for next conversion job. This is accomplished in the main program by writing a "1" into CRA-3 and CRB-3.

6.4 Start up or changing direction:

At start up the power source is turned on, however there is no ignition pulse from the KIM-1 to turn on the thyristors of chopper circuit. Upon commanding the "GO" to KIM-1, the control program begins its control and power is supplied to the motor.
Either on the start of power is supplied to the motor or whenever the rotational direction of motor is changed, if the primary thyristor stays on current in motor will be excessive. Thus the primary thyristor must be turned off and on periodically until the motor runs in its steady state. This is the second portion of the main control program as discussed below.

When the first synchronous signal SYNOOO appears on PB-5, the microcomputer will pick up the direction signal at PB-7 and store it at SIGN ($0000). Then subprogram "ON" will turn on the primary thyristor to supply power to the controlled motor. The primary thyristor will stay on for two time units (about 156 $\mu$s) then subroutine program "OFF" will turn on the secondary thyristor to turn off the primary thyristor. Two time units later, subprogram "ON" will turn on the primary thyristor again. After five times of the periodic "ON" and "OFF" of the primary thyristor, the power supplied to the motor is enough for the motor running in steady state. The main control program now goes to the next part which begins at the instruction labeled "START".

Whenever the sign signal is changed, the motor will be supplied current of opposite polarity. This abrupt change will cause the motor current to exceed its limit again if the primary thyristor stays on. Actually, this is the same situation as in start up. Thus the program will run for an idle chopper cycle (not to turn on the chopper for one chopper cycle) and then jump to the second part of the main program as discussed above to wait for the motor running in steady state again.

6.6 Compensation:

The last portion of the main program is to limit the motor's
average current. In this portion the microcomputer compares the calculated current obtained from "MULT" subprogram with the desired current and generating the time delay units (preset count number of programmable counter) of the primary thyristor's "OFF" time. The MPU must decide whether to increase or not to change or to decrease the control counter depending on which of three conditions is prevailing: either the calculated value is smaller than the desired value, the calculated value equals to the desired value, or the calculated value is larger than the desired value. To increase the control counter's preset count value will extend the chopper's "ON" time to supply more power to the motor. On the other hand, to decrease the control counter's preset value will shorten the chopper's "ON" time to reduce the power for the motor. The flow chart of the whole control program is shown in figure 16.

The chopper frequency of the experimental system is 100 Hz. It is found that the inverter (the independent power supply used to charge the commutation capacitors) must be synchronized with the turn-on and turn-off of the chopper, otherwise, here will be some noise while the inverter trying to synchronize with the chopper. This chopper circuit and motor are driven by a 20 volts power supply. The desired values of average motor current are stored in KIM-l's memory. The actual current values read from an ammeter are listed and compared with the desired values in Table 1. It shows a largest error of 4.2 mAmp. The error is caused primarily in the "MULT" voltage-to-current subprogram and noise from the load motor.
<table>
<thead>
<tr>
<th>DESIRED CURRENT $I_d$ (mAmp)</th>
<th>ACTUAL CURRENT $I_c$ (mAmp)</th>
<th>ERROR (mAmp)</th>
<th>ERROR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>85.8</td>
<td>4.2</td>
<td>4.67</td>
</tr>
<tr>
<td>100</td>
<td>96.5</td>
<td>3.5</td>
<td>3.50</td>
</tr>
<tr>
<td>110</td>
<td>108.6</td>
<td>1.4</td>
<td>1.27</td>
</tr>
<tr>
<td>120</td>
<td>118.5</td>
<td>1.5</td>
<td>1.25</td>
</tr>
<tr>
<td>130</td>
<td>126.4</td>
<td>3.6</td>
<td>2.77</td>
</tr>
</tbody>
</table>
 Initialization

Yes

Sync. signal PB-5 = 1 ?

No

Input current sign (motor direction signal)

Is sign signal changed ?

Yes

Subprogram "ON": to turn on the primary thyristor

Subprogram "CURENT": to input desired current value

Subprogram "STEADY": wait for motor in steady state

No

Unit = $14

Wait for pulse $f_1$, go to low.

Fig. 16 FLOW CHART OF MAIN CONTROL PROGRAM.
Subprogram "CONVER":
command A/D converter
start to work

Subprogram "VOLTAGE":
to obtain voltage
difference V(DIFF)

Subprogram "MULT":
to calculate average
motor current

If \( I_d > I_c \):
\[ I_d = I_c \]
Unit = Unit + 2

If \( I_d \leq I_c \):
\[ I_d = I_c \]
Unit = Unit - 2

Unit \leq 78
Yes
Unit > 14
No

Unit = 78
Yes

Fig. 16  FLOW CHART OF MAIN CONTROL PROGRAM.
PAD = Unit

Output PAD to programmable binary counter

Sync. signal PB-4 = 1?

No

Yes

Subprogram "OFF":
to turn on the secondary thyristor

Fig. 16  FLOW CHART OF MAIN CONTROL PROGRAM.
(CONCLUDED)
CHAPTER 7

FUTURE IMPROVEMENTS

7.1 Introduction:

The motor current limit system is controlled by a KIM-1 microcomputer. In this system the experimental results in Table 1 shows a largest error of 4.2 mAmp. Actually this error can be reduced to a smaller range by improving the control system.

7.2 I/O port expansion and capacity of binary counter:

The basic system needs four I/O ports. One of which must take charge of the output of time delay units to the programmable binary counter. The binary counters in this system can only count up to 127 pulses in each countdown period. As mentioned in Chapter 4, the phase shift between the "ON" and "OFF" of chopper is obtained from

\[
\phi = N \times \frac{360^\circ}{127}
\]

where \(N\) is the number of time delay units of chopper's "OFF". The average load current is determined by the phase shift \(\phi\). Thus, when the capacity of binary counter is increased, the phase shift \(\phi\) will has higher precision and the calculated average load current will be much close to the desired value. This will also lower the error which occurs in the process of division in "MULT" subprogram. Nevertheless, this "MULT" subprogram will take much more time to handle the multiplication and division of numbers having more bits. This method also needs to expand the output port to adapt the microcomputer to deal with the number of time delay units \(N\) which may now have more bits.
For those systems high precision being more important than speed of response, it is therefore necessary to consider the tradeoff of time and cost.

7.3 Powerful microcomputer:

KIM-1 is an 8-bit microcomputer having a 1 MHz clock. The register structure in the MPU of KIM-1 is quite simple although this is good enough to control a simple system. For a complicated system or when the high precision is required, the KIM-1 may need a longer program and more time to manage the control job.

In the microcomputer market, many new powerful products have been introduced recently. Some of them are 16-bit machines. Some of these have more registers or register pairs in their MPU. Some have more powerful instruction sets. These new microcomputers can do the same job as KIM-1 and obtain a higher precision. They may also require shorter processing time.

Higher precision could be reached by using 16-bit microcomputer because of the chopper period can be divided into more time units. Use of more bits for A/D converters is possible when 16-bit microcomputer is used or when more I/O ports are available. When using KIM-1 microcomputer, "MULT" subroutine in control program will take about 14 time units (78 μseconds per time unit). Now some microcomputers are designed to have one step instruction to handle 8-bit multiplication or 8-bit division (such as M6809, a product of Motorola). Then the execution time of "MULT" subprogram can be reduced to only a few μseconds (less than one time unit) when this kind microcomputer is used. This will not only speed up the system response but also spare memory space.
CHAPTER 8

CONCLUSION

A motor current control system has been devised and built. Except for the analog load network, the digital system has low power dissipation and high noise immunity control system. Four electro optical couplers used to control the chopper isolate the digital control system from the load network.

The motor current limiter works at a frequency of 100 cycles per second. The whole control system can limit the motor current either on the start up of the power supplied to the motor or when the motor direction changed. This system can also limit the average motor current. The resistor network designed to measure the reference resistor's terminal voltages is suitable for 5V A/D converters and 30V power supply for the chopper circuit.

Microcomputers have many advantages in size and flexibility. These advantages make microcomputers have the adaptability when changes of system parameters and environment occurred. Microcomputers may be modified to reach the goal of higher precision. Due to the progress of semiconductor technology, the price of microcomputer and its supporting components are lower while its powerful performance is greater. The microcomputer makes the automatic control digitalized and computerized easier than before.

The control program used in this system works as the comparator and the compensator. The desired current value and its direction can be changed by the toggle switches on the front control panel. Other
parameters of this system are prestored in the microcomputer's memory. When outside world is changed, all the controller has to do is changing the parameters in the memory. Thus this microprogram can be built in EPROMs or metal masked ROMs.
APPENDIX A

00000
00001 ; MAIN CONTROL PROGRAM
00002 

02000 A9 JO INITIA LDA #$00 ;
02020 BD 01 04 STA CRA ;PRINT TO CERA.
02050 BD 00 04 STA DDRA ;PORT A IS INPUT PORT.
02080 A9 3C LDA #$3C ;PRINT TO CRA, C11 INPU;
020A0 BD 01 04 STA CRA ;C22 OUTPUT, C22 HIGH.
020C0 A9 JO LDA #$00 ;
020F0 BD 03 04 STA CRB ;PRINT TO DBE.
02120 BD 02 04 STA DCRB ;PORT B IS INPUT PORT.
02150 A9 3C LDA #$3C ;POINT TO DBE C11 INPUT,
02170 BD 03 04 STA CRB ;C12 OUTPUT, C12 HIGH.
021A0 A9 7F LDA #$7F ;PA0----PA6 ARE OUTPUTS.
021C0 BD 01 17 STA PADD ;PA7 IS INPUT LINE,
021F0 A9 3F LDA #$3F ;PB0----PB3 ARE OUTPUTS.
02210 BD 03 17 STA PBDD ;PB4----PB7 ARE INPUTS.
02240 A2 00 LDX #$00 ;SET INTERRUPT VECTOR AT
02260 8E FF 17 STX #$17FF ;50000.
02290 A2 80 LDX #$80 ;
022B0 8E FE 17 STX #$17FE ;
022E0 A9 3F LDA #$3F ;
02300 BD 02 17 STA PBO ;PB4----PB3 ALWAYS HIGH.
02330 A9 14 LDA #$14 ;PRESUTE TIME DELAY UNITS.
02350 BD 03 17 STA PADD ;
02380 35 C6 STA UNIT ;
023A0 A9 80 LDA #$80 ;1ST SIGN IS POSITIVE.
023C0 35 C6 STA SIGN ;
023E0 EA NOP ;
02420 EA NOP ;
02450 BD 17 SYNCOD BIT PBO ;WAIT FOR FIRST Sync.
02420 2C 02 17 SYNCOD BIT PBO ;SIGNAL.
024F0 F0 FR BEQ SYNCOD ;
02470 AD 02 17 LDA PBO ;INPUT SIGN SIGNAL.
024A0 2B 80 AND #$00 ;
024C0 A9 20 LDA #$20 ;POW.
024E0 A2 05 POWER LDX #$05 ;SET COUNTER.
02500 2D 00 00 MODULE JSR ON ;THE PRIMARY THYRISTOR IS
02530 2C 10 00 JSR PULSE ;TURNED ON AND OFF
02560 2D 30 00 JSR OFF ;PERIODICALLY WAIT FOR
02590 2C 10 00 JSR PULSE ;MOTOR RUNNING IN STEADY
025C CA
025D 00 F1
025F A9 20
0261 2C 02 17
0264 F3 FH
0266 AD 02 17
0269 29 30
026B C5 C0
026D F0 0F
026F 85 C0
0271 A9 14
0273 8D 03 17
0276 35 C6
0278 20 18 00
027E 20 20 00
0281 20 90 00
0284 20 58 00
0287 20 60 00
028A 20 78 00
028C 20 23 03
0290 18
0291 A5 C1
0293 E5 C7
0295 DC 03
0297 4C AD 02
029A 10 DA
029C 18
029D A5 C6
029E E9 01
029F D5 C6
02A1 4C AD 02
02A2 18
02A5 69 01
02A8 A5 C6
02AF C5 78
02B1 30 07
02B3 A9 78
02B5 45 C6
02B7 4C 02 02
02B9 C9 14
02C3 10 04
02C5 A9 14
02C6 35 C6
02C8 3D 03 17
02CA 09 10
02CC 20 02 17
02CF 4C 0F 02

**DEX**

STATE UNTIL UNIT = #14.

**BNE** MODULE

WAIT FOR SYNC. SIGNAL.

**LDA** #820

**BIT** PBD

**BEC** SYNCO1

INPUT SIG. SIGNAL.

**AND** #88

**CMP** SIGN

**BEQ** SIGN

**STA** SIGN

**INC** BRANCH AND GO ON.

**STA** PAD

**OUTPUT TO COUNTER.**

**STA** UNIT

**AND SAVE IT.**

**JSR** ADDU

**WAIT FOR SYNC. SIGNAL LOW**

**JMP** START

**AND NEXT LOOP.**

**JSR** ON

**TURN ON THE PRIMARY SCR.**

**JSR** CURRENT

**PICK UP DESIRED CURRENT.**

**JSR** Steady

**WAIT FOR STEADY STATE.**

**JSR** CONVER

**COMMAND A/D CONVERTERS.**

**JSR** VOLTAGE

**CALCULATE V/DFI.**

**JSR** MULT

**CALCULATE AVERAGE CURRENT.**

**LOA** VALUE

**COMPARE DESIRED CURRENT**

**SBC** UNIT

**WITH CALCULATED VALUE.**

**BNE** ERROR

**NOT EQUAL, BRANCH AWAY.**

**JMP** TIMER

**EQUAL, JUMP TO TIMER.**

**BPL** LARGE

**IF (C).GT. (C), BRANCH.**

**BMI** SMALL

**IF (C).LT. (C), THEN**

**LDA** UNIT

**UNIT = UNIT - 1.**

**LDA** #501

**SBC** #501

**STA** UNIT

**JMP** TIMER

**IF (C).GT. (C), THEN**

**LDA** UNIT

**UNIT = UNIT + 1.**

**LDA** #501

**STA** UNIT

**LDA** UNIT

**IS UNIT TOO BIG?**

**CMP** #78

**BNE** SMALL

**UNIT TOO BIG.**

**LDA** #78

**OUTPUT**

**CMP** #14

**IS UNIT TOO SMALL?**

**DPL** OUTPUT

**LDA** #14

**UNIT TOO SMALL.**

**STA** UNIT

**BACK UNIT.**

**STA** PAD

**OUTPUT TO COUNTER.**

**LDA** #10

**WAIT FOR "OFF" SYNC.**

**JMP** OFF

**TURN ON THE SECONDARY SCR.**

**STA** START

**SO THAT CHOPPER IS OFF.**
LIST OF SUBROUTINE PROGRAMS.

; PULSE WIDTH OF IGNITION PULSE FOR TRIGGER CIRCUITS IS 50 MICRO SEC.

*=$0010

LDY #$0A ; THE EXECUTION TIME OF
DEY ; THIS SUBPROGRAM IS
BNE WIDTH ; MICRO SEC.
RTS ;

A/D CONVERTER

; A/D CONVERSION TIME IS 100--150 MICRO SEC.

*=$0018

; THE EXECUTION TIME OF
DEY ; THIS SUBPROGRAM IS
BNE PROCES ; 156 MICRO SEC.
RTS ;

; THE IGNITION PULSE FOR TRIGGER CIRCUITS
; IS SENT OUT ACCORDING TO SIGN SIGNAL TO
; TURN ON CHOPPER CIRCUITS.

*=$0020

LDA SIGN ;
CMP #$80 ;
BNE REVERS ;
JMP CURRENT ; TO TURN ON SCK(1,4).
LDA #$0E ; SIGN IS POSITIVE, PB0 LOW
REVERS LDA #08 ; SIGN IS NEGATIVE, PB2 LOW
CURRENT STA PB0 ; TO TURN ON SCK(2,3).
JSR PULSE ; PULSE WIDTH 50 MICRO SEC.
STA PB0 ; PB0 HIGH AGAIN.
LDA #0F ;
STA PB0 ; PB0 HIGH AGAIN.
; THE IGNITION PULSE FOR TRIGGER CIRCUITS;
; IS SENT OUT ACCORDING TO SIGN SIGNAL TO
; TURN OFF CHOPPER CIRCUITS.

; == $003A

003A A5 0D 00 OFF LDA SIGN ;
003C C9 80 CMP #80 ;
003E D0 05 BNE RECOMM ;
0040 A9 3D 00 LDA #50 ;SIGN IS POSITIVE, PB1 LOW
0042 4C 47 0D JMP COMMUT ;TO TURN ON SCR(5).
0045 A9 37 RECOMM LDA #57 ;SIGN IS NEGATIVE, PB3 LOW
0047 8D 02 17 COMMUT STA PBD ;TO TURN ON SCR(6).
004A 20 13 00 JSR PULSE ;PULSE WIDTH 50 MICRO SEC.
004C A9 3F 00 LDA #5F ;
004F 8D 02 17 STA PBD ;PBD HIGH AGAIN.
0052 60 RTS ;

; == $0053

0053 ; WAIT FOR MOTOR CURRENT GOING TO STEADY STATE
0053 ;

; == $0053

0058 A5 50 00 STEADY LDY #50 ;WAIT FOR 400 MICRO SEC.
005A 88 00 STATE DEY ;
005B 00 FD BNE STATE ;
005D 60 RTS ;

; == $0060

0060 A9 34 CONVER LDA #34 ;BRING CONTROL LINES CA2 &
0062 8D 01 04 STA CRA ;CA2 LOW AS START SIGNAL.
0065 8D 03 04 STA CRB ;
0068 26 16 00 JSR AADD ;WAIT END-OF-CONVERSION.
006B A9 3C 00 LDA #3C ;
006E 8D 01 04 STA CRA ;BRING CA2 & CB2 HIGH FOR
0070 8D 03 04 STA CRB ;NEXT CONVERSION LOOP.
0073 60 RHS ;
; PICK UP DIGITAL POTENTIALS AT ORA & ORB.
; AND CALCULATE THE VOLTAGE DROP ON REFERENCE RESISTOR.

; *=S0078

0078 A5 C0 VOLTAG LDA SIGN ; FIND OUT SIGN SIGNAL.
007A C9 80 CMP #$80 ;
007C D8 09 BNE NEG ;
007E AD 00 04 LDA ORB ; POSITIVE, V(ORB) HIGHER THAN V(ORB).
0081 ED 02 04 SBC DRB ;
0084 40 8D 09 JMP POSI ;
0087 AD 02 04 NEG LDA DRB ; NEGATIVE, V(ORB) HIGHER THAN V(ORB).
008A ED 00 04 SBC ORB ;
008E 35 C3 POSI STA DIFF ; SAVE V(DIFF).
0090 60 RTS ;

; SELECT DESIRED CURRENT VALUE AND SAVE IT.
; THE SELECTION IS CONTROLLED BY A TGGOLE SWITCH WHICH IS CONNECTED WITH PA-7.

; *=S0090

0090 AD 30 17 CURRENT LDA PAD ;
0093 29 80 AND #$80 ;
0095 10 05 BPL AMP01 ;
0097 A9 14 LDA #$14 ; PA-7 HIGH, DESIRED=14.
0099 40 9E 00 JMP AMPERE ;
009C A9 0A AMP01 LDA #$0A ; PA-7 LOW, DESIRED=10A.
009E 35 C1 AMPERE STA VALUE ; SAVE IT.
00AC 60 RTS ;

; INTERRUPT SUBPROGRAM: TO CLEAR INTERRUPT FLAG AT CRA-7 & CR3-7.

; *=S00BA

00BA AD 00 04 INTER LDA ORA ; READ DATA REGISTER WILL
00BB AD 02 04 LDA ORB ; CLEAR INTERRUPT FLAG OF
00BC 40 RTI ; ITS CONTROL REGISTER.
APPENDIX B

0323
; SUBPROGRAM "MULT" TO CALCULATE
0323
; AVERAGE CURRENT OF MOTOR.
0323

0323
85 C3
MULT
STA DIFF
; SAVE V(DIFF).
0325
A5 C6
LDA UNIT
; GET DELAY UNITS.
0327
65 C8
STA UNITCD
; 1ST MULTIPLICAND.
0329
AC 02
LDY #$02
; SET LOOP COUNTER.
032B
AC 22 03
LDA PERIOD
; SAVE 1ST MULTIPLICAND.
032C
85 C2
STA LOADR
;
0330
A9 00
MUL2
LDA #0
; LOW BYTE OF PRODUCT=0.
0332
85 C5
STA PRODH1
; HIGH BYTE OF PRODUCT=0.
0334
A2 03
LDX #00
; SET MUL COUNTER.
0336
0A
MULT3
ASL A
; SHIFT PRODUCT LEFT 1 BIT.
0337
26 C5
ROL PRODH1
;
0339
0E C3
ASL DIFF
; SHIFT MULTIPLIER LEFT.
033B
80 05
BCS MULT4
; NEXT BIT "ONE", BRANCH.
033D
48
PHA
; DUMMY DELAY.
033E
68
PLA
;
033F
4C 48 03
JMP MULT5
;
0342
13
MULT4
CLC
; INCREMENT FROM NEXT BIT 1
0343
65 C8
ADC UNITCD
; ADD MULTIPLICAND, PRODUCT
BCS  MULT6 ; WITH CARRY IF NECESSARY.
NOP  ;
JMP  MULT7 ;
INC  PRODH1 ; INCREMENT OF HIGH BYTE.
MULT7  DEX  ;
BNE  MULT3 ; CHECK MULT COUNTER.
STA  PRODLC ; SAVE LOW BYTE OF PRODUCT.
STA  QUOT  ; AS LOW DIVIDEND BYTE.
LDX #08  ; SET DIVISION COUNTER.
LDA  PRODH1 ; GET HIGH DIVIDEND BYTE.
DIVID1 ASL  QUOT  ; SHIFT QUOTIENT LEFT.
ROL  A  ; SHIFT QUOTIENT LEFT.
CMP  LOADA  ; CAN DIVISER BE SUBED?
BCC  DIVID2  ; NEG, JD TO NEXT STEP.
BSC  LOADA  ; YES, SUBTRACT DIVISER.
INC  QUOT  ; AND INCREMENT QUOT BY 1.
JMP  DIVID3  ; DUMMY DELAY.
PHA  ;
PLA  ;
NOP  ;
NOP  ;
DIVID3  DEX  ;
BNE  DIVID1  ; CHECK DIVIDION COUNTER.
DEY  ;
BEQ  DIVID4  ; CHECK LOOP COUNTER.
INC  QUOT  ; COMPENSATION FOR ERRORS.
LODA  ;
STA  UNITC  ; NEW MULTIPLIER.
LDA  QUOT  ; NEW MULTIPLICAND.
STA  DIFF  ;
; LOAD VALUE MUST BE CHANGED ACCORDING TO THE ; MOTOR LOAD RESISTANCE WHEN MOTOR IS CHANGED.
LDA  LOAD  ; NEW DIVISER.
STA  LOADA  ;
JMP  MULT2  ; JD ON SECOND LOOP.
RTS  ; DONE, GO BACK TO MAIN.
END

END OF MUS/TECHNOLOGY 650X ASSEMBLY VERSION 5
NUMBER OF ERRORS = 0, NUMBER OF WARNINGS = 0
BIBLIOGRAPHY


ACKNOWLEDGMENTS

The writer wishes to express his sincere appreciation to Dr. Wellington W. Koespel, his major professor, for his valuable assistance and advice in preparing this thesis.

The writer is grateful to Dr. Donald Howard Lenhert and Dr. Michael S. P. Lucas for providing the components and to the Department of Electrical Engineering for providing the facilities to make this project a reality.

The writer also likes to give thanks to Dr. John Maurice Marr and Dr. Nasir Ahmed for serving as committee members.
A CURRENT LIMIT CONTROL  
FOR A CHOPPER-FED D-C MOTOR  
BY USING A KIM-1 MICROCOMPUTER  

by  

CHIH-SHYONG SHIH  
B.S., Tamkang College, Taiwan, 1976  

AN ABSTRACT OF A MASTER'S THESIS  

submitted in partial fulfillment of the  
requirements for the degree  

MASTER OF SCIENCE  

Department of Electrical Engineering  

KANSAS STATE UNIVERSITY  
Manhattan, Kansas  
1982
ABSTRACT

A system using digital techniques to control the current and the direction of rotation of a chopper-fed d-c motor is discussed. This system is composed of logic circuits and a KIM-1 microcomputer which offers overall advantages in performance, flexibility, and reliability.

While controlling the motor current, it is measured and compared with a reference setting (the desired current in binary form) and the error is then used to adjust the length of thyristor chopper's "ON-time" such that the motor current is maintained at its desired value.

The KIM-1 microcomputer is used to implement the sampled data feedback control. The motor current at start up or changing direction is limited by the chopper's "ON-time" which is controlled by the logic circuits and the KIM-1 microcomputer.