

INTEGRATED UHF CMOS POWER AMPLIFIERS IN SILICON ON INSULATOR
PROCESS

by

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B.E. Kyungpook National University, Republic of Korea, 2001
M.S. Kansas State University, 2003

AN ABSTRACT OF A DISSERTATION

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Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2008

Abstract

Design challenges and solution methods for Watt-level UHF CMOS power amplifiers are presented. Using the methods, a fully-integrated UHF (400MHz) CMOS power amplifier (PA) with more than 1-Watt output is demonstrated for the first time in Silicon on Sapphire (SOS) process. The design techniques are extended for a two-stage five-chip 5-Watt CMOS PA.

In the 1-Watt PA, a differential stacked PMOS structure with floating-bias and a 1:3 turns-ratio output transformer are chosen to overcome low breakdown voltage (V_{bk}) of CMOS and chip area consumption issues at UHF frequencies. The high Q on-chip transformer on sapphire substrate enables the differential PA to drive a single-ended antenna effectively at 400 MHz.

The PA is designed for a surface-to-orbit proximity link microtransceiver, used on Mars exploration rovers, aerobots and small networked landers. In a standard package the PA delivers 30 dBm output with 27 % PAE. No performance degradation was observed in continuous wave (CW) operation with various output terminations and the PA was tested to 136 % of its nominal 3.3 V supply without failure. Stability analysis and measurements show that the PA is stable in normal operation. It is also shown that the PA is thermally reliable. In the microtransceiver circuits, the PA works in conjunction with transmit/receive (TR) switch to allow nearly the full 1-Watt to reach the antenna.

The 1-Watt PA design is also leveraged to demonstrate a power-combined two-stage five-chip PA. The 1-Watt PA's output balun is modified for the four-transformer combining. Four identical chips are wire-bonded in the output stage and the fifth identical chip is added as a drive-amplifier. Despite low efficiency due to damaged bias circuits, the PA provides 5-Watt output power (37 dBm) at 480 MHz with 17 % PAE with 17 dB gain. The PA layout is carried out considering full integration on a $7 \times 10 \text{mm}^2$ die. It will be the highest output CMOS PA ever reported once the full integration is implemented.

The research contributes to state of the art by developing design-techniques for a TR switch and PAs on SOS process. The resonant TR switch technique is applied to a full transceiver and the multi turns-ratio on-chip transformer is used in PA's output matching network for the first time. The PA design is also extended to the 5-Watt PA, demonstrating the highest output power in CMOS process.

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Major Professor
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Dedication

When I arrived at Kansas City airport in the hot evening in August 2001, I was alone and serious. Hot humid wind in the airport was not pleasant but I had to figure out how to get on the shuttle to Kansas State University, Manhattan. Since then, there were hard times but I am graduating with a lot more sweet memories. Thank God I did it.

First and most of all, I want to thank my parents YoungGi Jeon and OiSoon Jeong for their endless belief and support during my never-ending school years. I thank my wife, Miryung So, for encouraging me all the time and sacrificing her career only to become a miserable international student's wife. And our baby girl, Robin Jiwoo Jeon, gave us wonderful experience of life – being parents.

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Chapter 1 - Introduction

In January of 2004, photographic panoramas from another world were transmitted to the earth by the Mars Exploration Rovers, Spirit and Opportunity, captivating the public's attention. In the following year, more than 90 Gbits of photos and data were relayed through the UHF surface-to-orbiter proximity links [1], offering evidence of past liquid water environments in which life could have developed.

Despite their great scientific functionality and achievements, the rover's large size ($\approx 5 \text{ m}^3$) and mass ($\approx 185 \text{ Kg}$) allowed only one rover per launch, limiting surface exploration of the planet to only two sites [2]. If a number of much smaller scout vehicles could be designed, the number of successful missions at given revenue would increase dramatically and many more sites could be explored. The Mars microtransceiver project, under which this work was carried out, targets significant reductions in size, mass, and power consumption of the UHF communications radio system as an enabling technology for such future missions [3].

Although reduction of a radio communication circuit's size/mass comes directly from high integration, the associated Power Amplifier (PA) is implemented traditionally in a compound semiconductor process and requires additional off-chip components. This thesis discusses design challenges and provides solutions of Watt-level UHF CMOS power amplifiers. For the first time, a 400 MHz band CMOS Watt-level PA is fully integrated, utilizing an on-chip multi-turn transformer in Silicon-on-Sapphire (SOS) process. Furthermore, a new design technique is developed to apply a resonant switch in a complete transceiver.

The fully integrated CMOS PA and the resonant TR switch developed in this research lets a miniature transceiver unit be built with two analog chips, one digital chip, and a few off-chip parts as suggested by [3] and shown in Figure 1-1, while holding the promise of a single chip high power radio implemented entirely in the space-qualified SOS CMOS process selected for the work.

In addition to detailing the new techniques in the 1-Watt PA, developed for this application, this thesis demonstrates a multi-Watt power combining utilizing the 1-Watt PA design in a separate project. Chapter 2 presents a brief introduction of RF power amplifiers, in

which numerous RF PA classes and techniques are described. General tutorials on thermal analysis and stability analysis are provided in Chapter 3 and Chapter 4, respectively. In Chapter 5 it is shown that the SOS process has unique characteristics and advantages in the RF PA design. As for circuit implementation, Chapter 6 discusses the microtransceiver RFIC in Figure 1-1, which drives the 1-Watt PA and provides a T/R switch function. Chapter 7 and 8 elaborate the 1-Watt PA with information on design, performance, stability and reliability. Nonlinear effects of the PA are also discussed. Using the multi-Watt power combining technique, a two-stage five-chip 5-Watt PA are demonstrated in Chapter 9, followed by conclusions in Chapter 10.

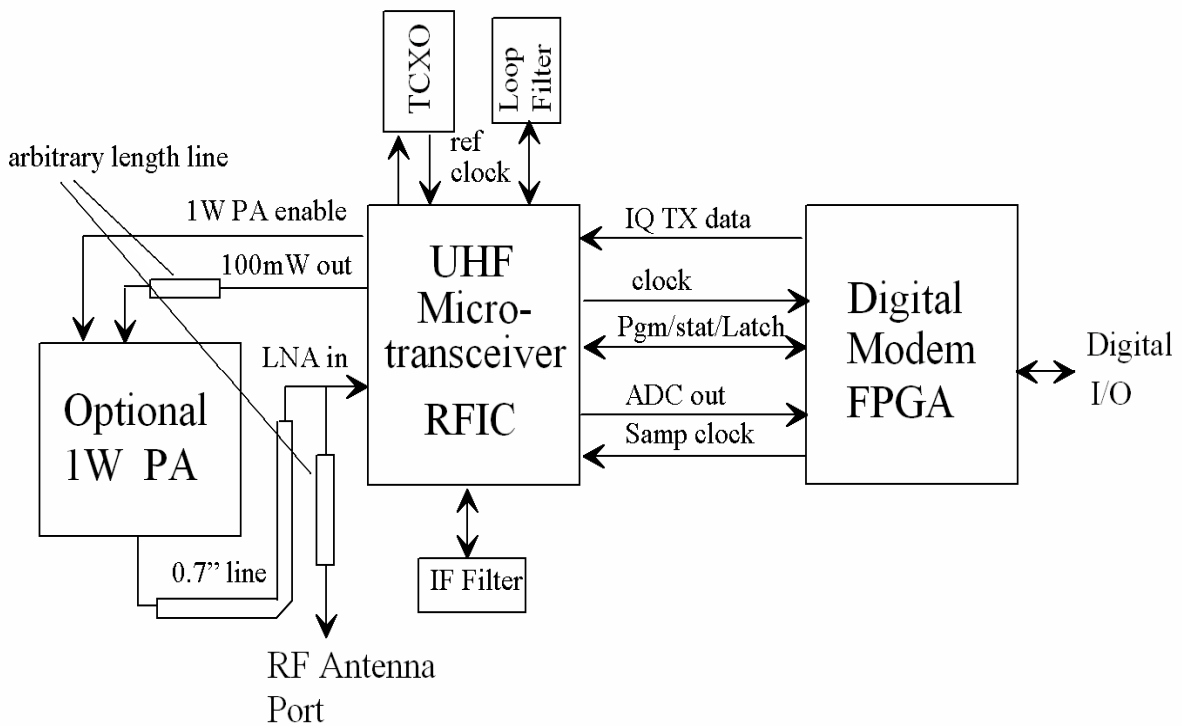


Figure 1-1: The microtransceiver layout floor plan

Chapter 2 - RF PAs

1. RF PA Classes

Nearly all the alphabetical letters are already assigned to define numerous PA classes. If one invents a totally new PA class, he/she must spend considerable time to name its class. However, some definitions are very subjective, and, in some cases, the boundary between different classes is indistinguishable. This Chapter introduces only well-defined and popular RF PA classes.

When we evaluate a RF PA, efficiency is one of the most important specifications, but the efficiency does not accompany linearity of the PA. As an active component is driven strongly into compression for high efficiency, the PA tends to generate large harmonics. The classes of RF PAs are diversified in pursuit of either linearity or efficiency as they are divided into two categories whether transistor acts as a current-source or a switch. The current-source classes include class-A, B, AB and C. The latter, switching-modes, are class-D and E. Class-F is also described at the end.

The efficiency must be defined before elaborating on each class. The efficiency (η) is the ratio of RF output power to DC power from supply.

$$\eta = \frac{P_{out}}{P_{DC}} \quad (2.1)$$

In order to take power gain into account, Power Added Efficiency (PAE) is also defined. RF input power is subtracted from the output power in the definition. Therefore, the RF PA with low power gain is not PAE-efficient.

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout}}{P_{DC}} \left(1 - \frac{1}{G}\right) = \eta \left(1 - \frac{1}{G}\right) \quad (2.2)$$

Current Source Mode RFPA Classes

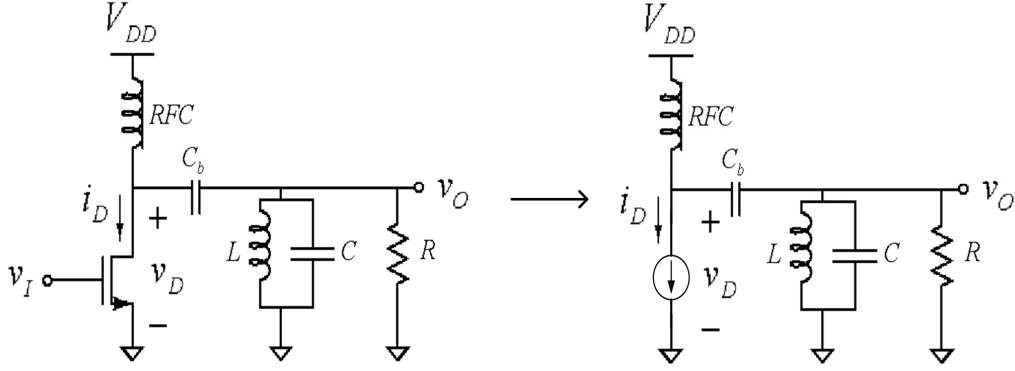


Figure 2-1: Class-A, B, AB and C RF PA (a) schematics and (b) equivalent circuit.

Class-A, AB, B and C RF PAs belong to the current source mode, which means the current-source can model active components or transistors in the RF PA as shown in Figure 2-1. Details on the schematics can be found in [4]. For example, in a class-A PA, input DC gate bias V_{GG} is greater than the amplitude of the input RF signal V_G . Therefore, RF current always flows through the transistor, even at the minimum V_G , and both v_I and i_D maintain sinusoid without clamping. The voltage at the input and the drain current are presented as

$$v_I(\theta) = V_{GG} + V_G \sin \theta \quad (2.3)$$

$$i_D(\theta) = I_{DC} - I_D \sin \theta \quad (2.4)$$

When v_I is adjusted for maximum drain voltage amplitude, v_D , and $I_D = V_{DD}/R$, Figure 2-2 shows waveforms of the PA.

The class-A PA has superior linearity but suffers from low efficiency due to large DC current which flows even without input signal. With an RFC at the power supply line as shown in Figure 2-1, the maximum theoretical efficiency is 50% when the PA is fully driven [5].

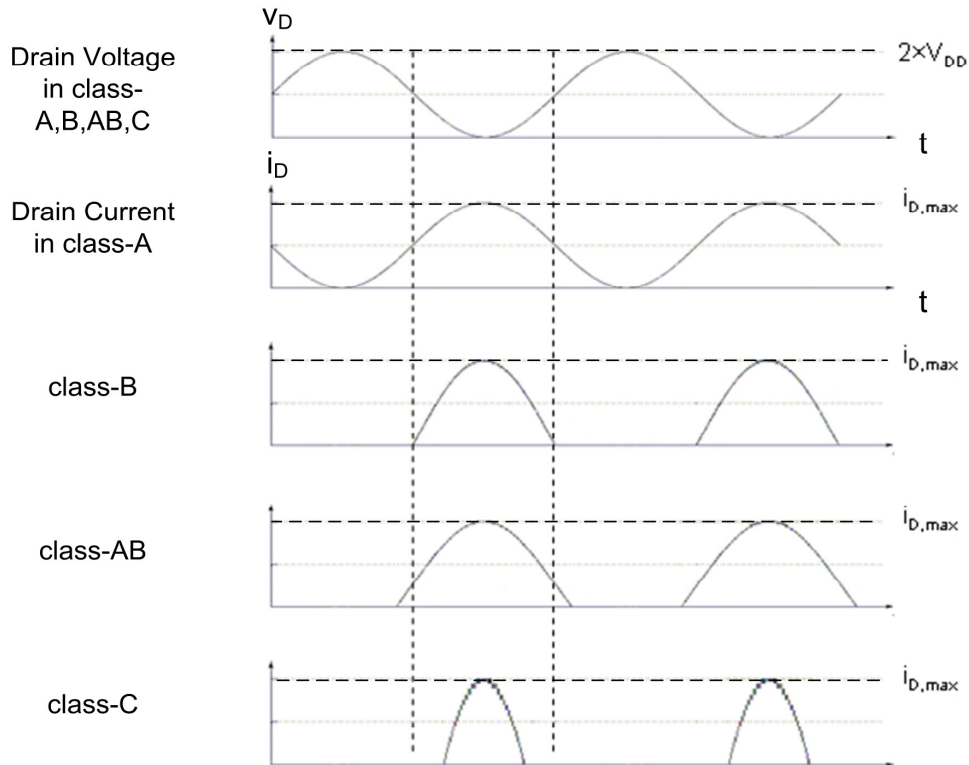


Figure 2-2: Waveforms in class-A, B, AB and C PA

A Class-B PA is biased such that the current source is active for only half a cycle, and $V_{GG}=0$. However, it generates the same drain voltage waveform due to output resonant circuit and improves efficiency from the class-A PA. A push-pull, transformer-coupled circuit is commonly used for class-B PA.

As implicated in the name, the class-AB compromises between the class-A and B and $0 < V_{GG} < V_G$. Hence, it can offer good linearity and acceptable efficiency. Many linear PAs are claimed to be the class-AB [6] [7].

Very high efficiency can be achieved as i_D flows for only a small portion of period ($V_{GG} < 0$) in a class-C PA, but pulse-like current in the drain generates even stronger harmonics than the class-AB PA.

Switch-Mode RFPA Classes

A transistor can be modeled as a switch instead of a controlled current-source when it is driven by a sufficiently strong input. The transistor alternates between on and off states and

voltage and current does not co-exist across the device. Therefore, no power is dissipated in the device and all DC power is converted to RF power ($\eta = 100\%$). For example, when constant DC voltage is supplied through the switch and drain voltage has a rectangular shape, the PA becomes a voltage-switching class-D (VSCD, Figure 2-3). Instead of the constant voltage, constant current is steered via switches in a current-switching class-D PA (CSCD, Figure 2-4).

Although the class-D RFPA ideally achieves 100% efficiency in either case, the efficiency is sensitive to frequency and duty-cycle variation. Due to their rectangular voltage and current waveforms, the voltage-current product across the transistor becomes significant once the ideal waveforms are disestablished, which results in power loss in real-world transistors. Although the class-D works well in low frequency applications, the transistor's loss increases significantly at high frequency. It is difficult to control the duty-cycle and parasitic passives are substantial at high frequency. For instance, due to parasitic C_{DS} , high order harmonics are suppressed and the waveforms become smoother than square.

In order to alleviate the wave shape sensitivity, a class-E PA (Figure 2-5) was invented by Sokal [8]. The class-E topology manipulates output networks in such a way that v_D decreases gradually and its slope becomes zero before the switch turns on (Zero Voltage Switching, ZVS). Therefore, the PA maintains minimum low voltage-current overlap during the turn-on moment. The traditional class-E associates an RF choke inductor at supply line but a finite inductor can also be used in order to meet the ZVS condition (in the parallel circuit class-E) [9]. Despite the class-E PA's advantage, the output network raises the v_D peak to a very high level – $v_{D,peak} = 3.56V_{DD}$ in the traditional class-E, and $v_{D,peak} = 3.65V_{DD}$ in the parallel circuit class-E.

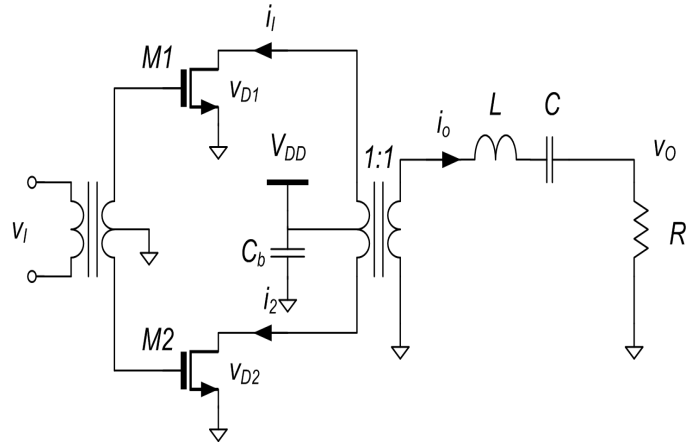


Figure 2-3: Transformer-coupled voltage-switching class-D PA.

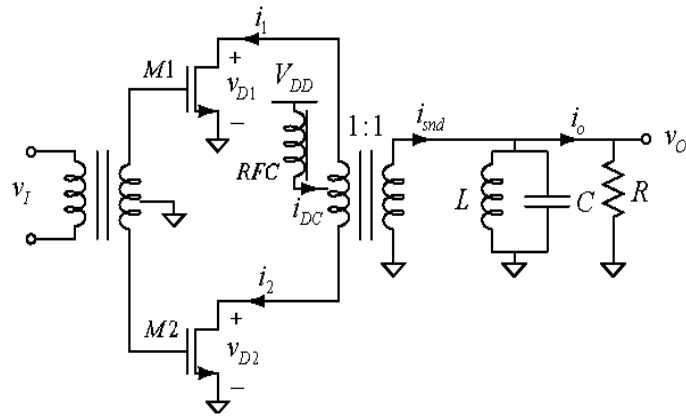


Figure 2-4: Transformer-coupled current-switching class-D PA.

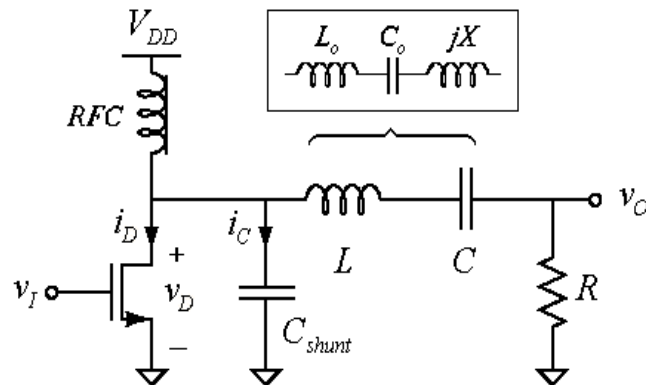


Figure 2-5: Traditional class-E PA.

Class-F and Inverse Class-F RFPA

While the class-D PA creates a rectangular waveform by switching either constant voltage or current from the power supply, a class-F PA builds the rectangular waveforms by terminating the transistor's drain with harmonically tuned filters. In other words, if the drain sees open circuits at odd harmonics and short circuits at even harmonics, the drain voltage becomes rectangular. Tuning up to 5th harmonics is a practical limit since higher tuning returns no improvement due to resistive loss in the filters. Instead of the square voltage waveform, the inverse class-F (F^{-1}) passes rectangular current through the transistor as it sees short circuits in odd harmonics.

Whether it is class-D, E, or F, it is possible to achieve very high efficiency if high order harmonics are in control. However, as operating frequency goes up and susceptance of parasitic capacitance becomes comparable to load resistance, there no longer exist the perfect square waveform and ZVS. The efficiency degrades and the difference among the classes becomes less conspicuous. It is analytically shown by Rabb [10] that the high efficiency PA classes improve the efficiency almost at the same rate as the number of harmonics in use increases.

2. Breakdown Voltage Issues

It is difficult to fabricate a Watt-level RF PA in CMOS process without power combining or impedance transformation. The CMOS's low breakdown voltage (V_{bk}) makes the PA vulnerable to high output voltage value. Normalized power output capability (P_{max}) quantifies the voltage and current stress on the PA [5].

$$P_{max} = \frac{P_{out}}{i_{D,max} v_{D,peak}} \quad (2.5)$$

The definition is meaningful when the PA is made of a discrete transistor, which has $i_{D,max}$ fixed by the manufacturer. However, $i_{D,max}$ can be decided by a designer as far as an integrated PA is concerned and a different measure is needed. Since $v_{D,peak}$ cannot exceed V_{bk} , it is convenient to equate P_{out} with V_{bk} . The relations are shown in Table 2-1. A push-pull and 1:1 transformer-coupled PA is assumed since it is favored in CMOS implementation because of virtual ground and a balun function. The output power of a single-end PA can be easily calculated by dividing it

by four. The derivations are found in Appendix A, where it is shown that high V_{bk} and low R are essential to generate high output power. When V_{bk} is fixed by process, voltage switching class-D has the highest output power. Interestingly the parallel circuit class-E [9] is capable of generating approximately 2.3 times more power than the traditional class-E with slightly higher $v_{D,peak}$.

RFPA Class	A, B, AB and C	D (voltage switching), F	D (current switching), F ⁻¹	Traditional E	Parallel circuit E
$v_{D,peak}$	$2V_{DD}$	$2V_{DD}$	πV_{DD}	$3.56V_{DD}$	$3.65V_{DD}$
P_{out}	$V_{bk}^2/2R$	$8V_{bk}^2/\pi^2R$	$V_{bk}^2/2R$	$0.18V_{bk}^2/R$	$0.41V_{bk}^2/R$

Table 2-1: Output power of the classes in terms of V_{bk}

Stacked Transistors

If 1-Watt output power is needed and $R = 50 \Omega$, v_D must be as high as 20 V_{pp}. Typical 0.5um CMOS FET only survives approximately 4 V and short channel processes result in much lower V_{bk} . Stacking transistors can afford double $v_{D,peak}$ by sharing v_D in two transistors [11] as shown in Figure 2-6b but the penalty for the stacking is increased transistor loss by twice R_{on} in S1 and S2.

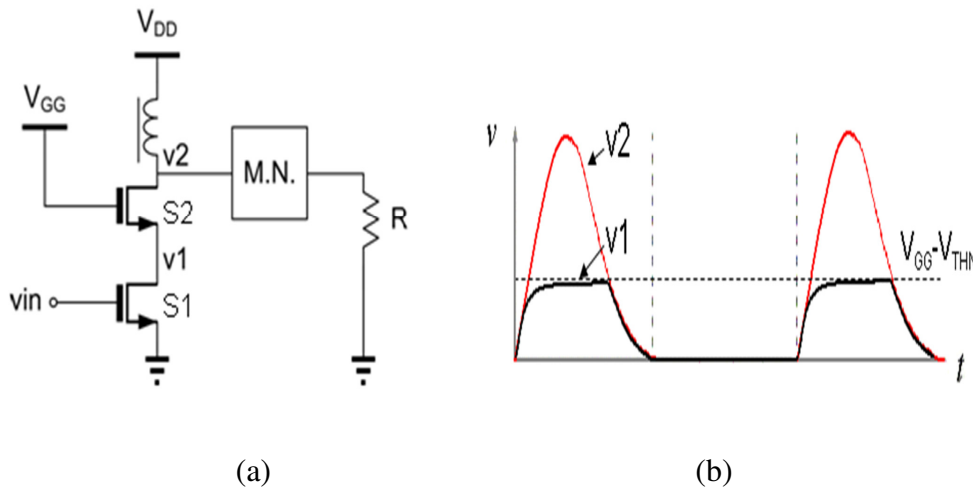


Figure 2-6: Stacked transistors: (a) schematics and (b) waveforms

Load Transformation

In addition to increasing v_D by stacking, reducing R is another way of boosting output power. All the impedance matching techniques are applicable for the purpose. For instance, LC networks are shown in Figure 2-7a. High transform ratio N degrades its efficiency, $\eta = P_{out}/P_{in}$, because parasitic resistance in the inductor and the capacitor becomes significant relative to R_2 . Since Q of the capacitor is much higher than that of the inductor, it is mandatory to use high Q inductor for the transform-efficiency. Bondwire inductors are suitable for the inductor due to its high Q factor as long as length of the wire is well controlled. The efficiency of the LC networks is [9]

$$\eta = \frac{1}{1 + \frac{\sqrt{N-1}}{Q_{ind}}}, \quad N = \frac{R_2}{R_1}. \quad (2.6)$$

Secondly coupled spiral inductors can be used for the load transformation. The efficiency of the transformer in Figure 2-7b is a function of the Q factor and of the coupling coefficient k . If the Q factor of the primary and the secondary coils are Q_{pri} and Q_{sec} , respectively, and the leakage inductance at the secondary are tuned out by a series capacitor, the efficiency is [12]

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_{pri}Q_{sec}k^2}\right)\frac{1}{Q_{pri}Q_{sec}k^2} + \frac{2}{Q_{pri}Q_{sec}k^2}}} \quad (2.7)$$

Although not shown explicitly in (2.7), the efficiency falls with increasing N since difference in turns between primary and secondary coils weakens magnetic coupling in the 2D on-chip transformers. The transformer also functions as a balun in many differential PA applications. Lastly if the frequency of operation is high and wavelength is relatively short, microstrip-line circuits offer high efficiency impedance transformation as shown in Figure 2-7c.

Table 2-2 shows the efficiency comparison among the techniques assuming a modest Q of 5 in a bulk CMOS process. For $N = 10$, the bondwire LC matching and the microstrip-line circuit outperform the others. The on-chip circuits attribute low efficiency to their low Q factors.

As will be seen later, this efficiency reduction is less in the Silicon on Sapphire process used in this research effort, due to available Q s from 10 to 30 depending on frequency of operation.

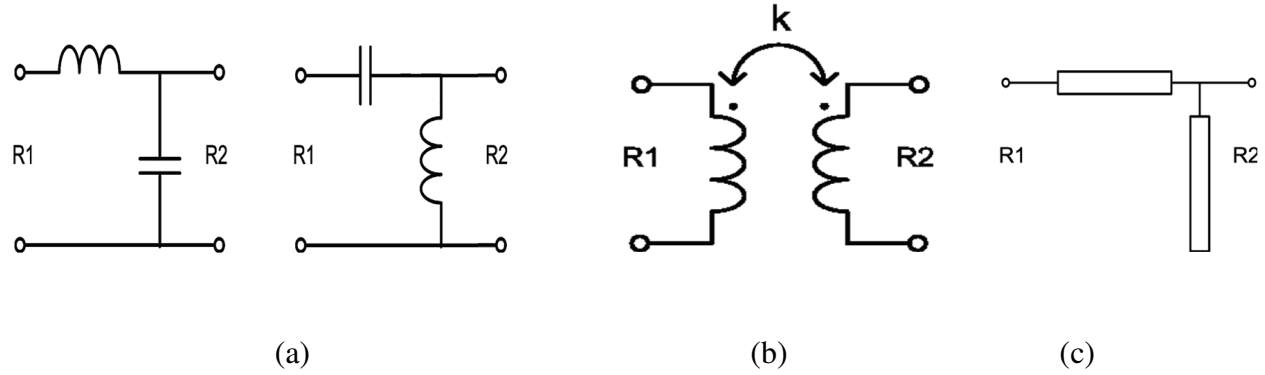


Figure 2-7: Load transformation methods: (a) LC matching networks, (b) transformer, and (c) transmission-line.

	loss	η
LC matching	$Q=5$ (on-chip)	63% by (2.6)
	$Q=50$ (bondwire)	94% by (2.6)
Transformer	$Q=5$ (on-chip, $k=0.8$)	61% by (2.7)
Microstrip line	Loss tangent=0.01 (FR4, $h=62$ mil at 400MHz)	97% by simulation

Table 2-2: Impedance transformation efficiency ($N=10$).

Power Combining

It is possible to arrange multiple PAs in order to add up their output power. Transformer combining as shown in Figure 2-8a is well suited with push-pull PAs. The differential structure offers benefits from virtual ground and the transformer not only combines two outputs but it converts them into single-ended output. The LC balun in Figure 2-8b [13] also power-combines the differential output but does not provide virtual ground at common nodes. Expanding the transformer combining, two [14] or four differential pairs [12] are combined in a circular geometry for less voltage stress distributed to transistors (Distributed Active Transformer, DAT) as shown in Figure 2-8c. Transmission-line circuits such as Wilkinson combiner (Figure 2-8d)

and coupler combining (Figure 2-8e) are rarely seen in integrated PAs due to their size but were still applicable at 5.8 GHz [15].

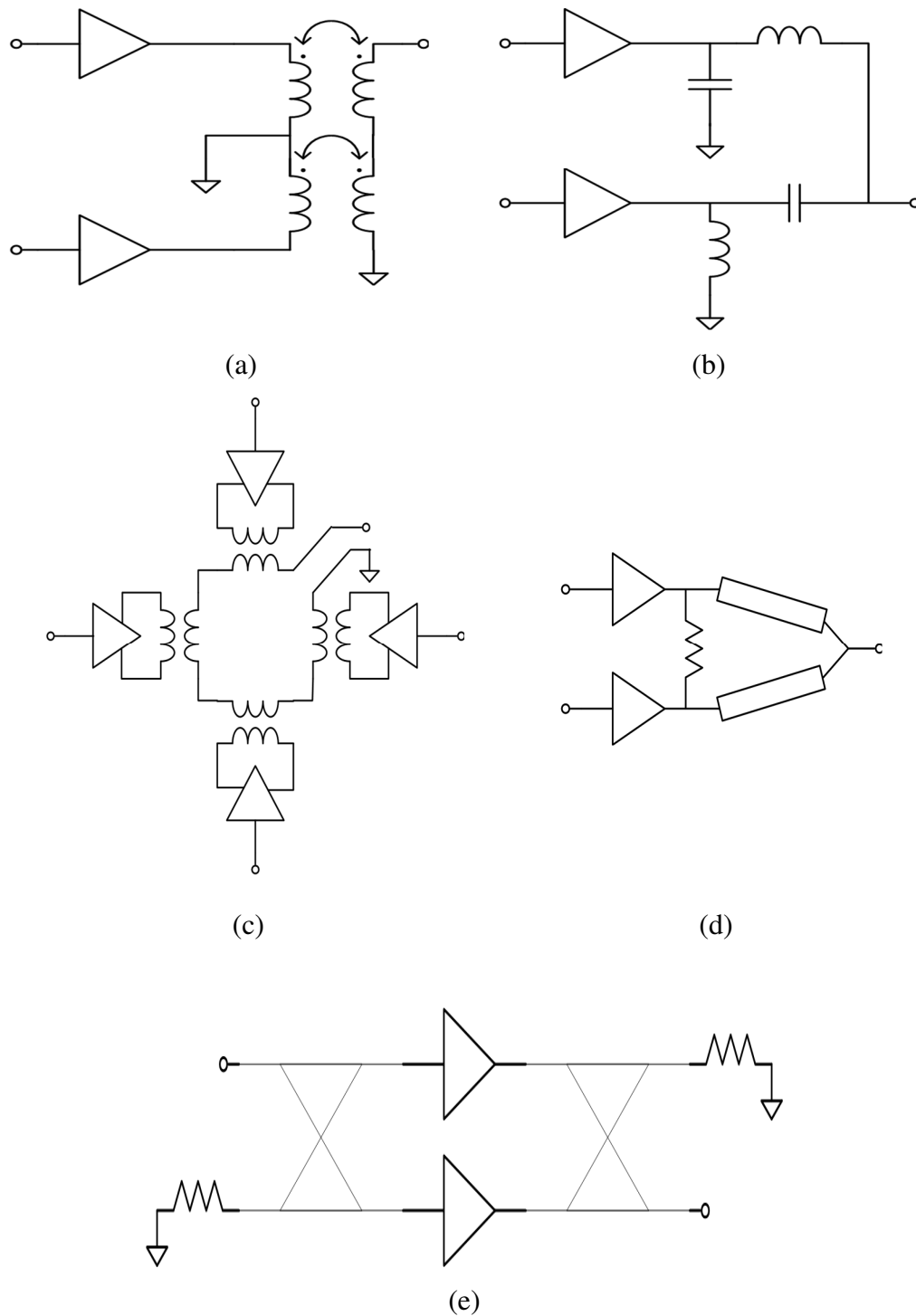


Figure 2-8: Power combining techniques: (a) transformer combining (b) LC balun (c) DAT (d) Wilkinson combiner and (e) coupler combining (a balanced amplifier)

3. Linearization Techniques

There was a time when communication systems generously allowed an RF PA's nonlinearity. For example, AMPS (Advanced Mobile Phone System) used FM so that it was possible to utilize the highly efficient but nonlinear PA in the constant amplitude signal transmission. However, the modern communication system demands much more data volume, and a complex modulation scheme is inevitable. A lot of the communication protocols adopt wideband multi-carrier modulation schemes, and they require stringent linearity as the peak-to-average power ratio becomes large and IM products are more troublesome. The high linearity can be achieved simply by backing-off class-A PA, but other methods are needed to deal with the resulting decrease in efficiency.

Pre-distortion

In order to compensate the RF PA's distortion when operating with small back-off, a predistorter can be inserted between input and the PA as shown in Figure 2-9a. The predistorter's gain function has high order coefficients which nullify the nonlinearity of the PA. As shown in the figure, the predistorter has inverse gain curve to the PA along the linear line. Analog predistorters such as a PIN diode, a mesa resistor, and a cuber, are simple and fast but only work well in certain input power levels and need adjustment due to process variations [16]. A DSP predistorter is more robust and adaptable than the analog version but power consumption is a problem with ADC, DAC and look-up table (LUT). Moreover, they require overwhelming efforts for high precision correction.

Feedback

It appears that feedback is a panacea in designing a low frequency amplifier. Yet, the powerful technique loses its edge due to phase delay around the loop in RF and microwave whereas the significant delay makes the loop unstable. In order to circumvent it, the feedback is done in IF or baseband, where the phase delay is negligible, in polar-loop systems [17] and Cartesian loop [18] as shown in Figure 2-9b and 2-9c. By closing loops, both systems have high immunity to drift, aging, and power supply variation. In the polar-loop, modulated IF at the input is separated into envelope and phase and they are compared with down-converted PA's output, and then compensation signals are provided by video amplifiers as shown in Figure 2-9b.

A challenge in the polar loop is that splitting QPSK into the polar form results in wide bandwidth requirement in the phase channel [7]. On the other hand the Cartesian loop separates modulation signal into I and Q forms and the quadrature signals make up independent feedback paths due to their orthogonality. In a system with DSP at baseband, the I and Q can be provided without the wideband audio phase-shifter at the input. The Cartesian loop has advantages in reduced loop bandwidth and simple hardware implementation [19]. Recently a multi-band cellular polar-loop transmitter was demonstrated by Sowlati et al [20].

Feedforward

Instead of feeding an error signal or distortion back to input, a feedforward technique amplifies a compensation signal by an auxiliary PA and adds it forward to output as shown in Figure 2-9d. The input RF signal is split and passes through a nonlinear main PA and a delay. When the split signals are summed again, v_e is the difference between the distorted signal and the linear signal. The difference is amplified and subtracted from the delayed RF output by the coupler, resulting in linear RF output. The feedforward is relatively easy compared to the feedback and more effective than the predistorter. However, since it is an open-loop-correction method, drift and environmental change could deteriorate performance [19]. Noting that there is no correction for the nonlinearity of the auxiliary PA, multiple loops may be needed.

Envelope Elimination and Restoration (EER)

EER, also called Khan-technique named after the inventor, is basically an envelope modulation technique [19]. It extracts amplitude information from the input before making a constant envelope signal via a limiter. The limited input is amplified by a high efficiency but nonlinear RFPA. Then, the amplitude information is recovered by an audio or baseband supply voltage control as shown in Figure 2-9e. The technique underperforms when the input signal level and bias voltage are too low since the RFPA needs headroom. Incorporated with an envelope feedback, the EER met NADC requirements in a CMOS monolithic implementation [21].

Doherty Power Amplifier

As mentioned earlier, the trouble with class-A, B, and AB PAs is low efficiency if the PAs need to operate at low power for most of the time and jump to full power mode occasionally

with the load optimized for the full power operation. If the load resistance increases dynamically for lower output power with constant drain voltage, the efficiency at the low power level need not to be sacrificed.

The Doherty power amplifier, shown in Figure 2-9f, enables the dynamic load transformation by an Auxiliary PA (APA) and a quarter-wavelength transmission-line. At low power mode, a Main PA (MPA) operates alone and it sees R_1 , which is Z_0^2/R_L . Therefore, a linear PA is chosen for the MPA. For instance, if the MPA is class-B, the maximum efficiency of the Doherty PA is 78.5 % ideally right before the APA becomes active.

A typical APA is biased for class-C that I_2 contribution to I_L is zero until input voltage reaches a half of the maximum level (-6dB from the maximum input). As the input power increases over the 6 dB back-off level, R_3 begins to increase to $(1+I_2/I_1)R_L$ by the APA's output current contribution. However, the MPA sees inverse action by the quarter-wavelength transmission-line, and R_1 actually decreases, resulting in higher output power with unchanged drain voltage. At the maximum output power, the MPA sees $Z_0^2/2R_L$, which is a half of the load at low power level. If $Z_0 = 2R_L$, both PAs see $2R_L$ and contribute the same power ($I_1 = I_2$) with the same efficiency of 78 % because the APA also enters the class-B mode. The APA's output power is also combined at R_L as the same quarter-wavelength is added in front of the APA so that both the PAs are in phase.

The Doherty PA is popular in cellular base station PA applications using commercial power transistors [22] [23] because the quarter-wavelength transmission-line in low RF is too long to fit in mobile applications. However, equivalent circuit to the quarter-wavelength transmission-line can be implemented using an LC pi-network. The Doherty PAs with on-chip inductors were demonstrated at 1.7 GHz and 3.65 GHz in [24] and [25], respectively.

LINC (Linear amplification using Nonlinear Components)

Finally, if RF input signal $S(t)$ in Figure 2-9g can be separated into two constant envelope signals with different phases, we can use two nonlinear switch-mode PAs for $S_1(t)$ and $S_2(t)$ [19]. The concept is straightforward, but it is complicated to implement the signal separator by analog circuits. Instead the mathematical expression of $S_1(t)$ and $S_2(t)$ can be devised by modern DSPs. For example, the input signal is separated in baseband by the DSP and then up-converted by a local oscillator (LO). The up-converted signals are amplified by PA1 and PA2 in the same way.

Phase error between two PAs' paths is critical in the LINC. For example, in order to achieve 40 dB amplitude dynamic range, $S1(t)$ and $S2(t)$ need the precision of one degree phase-shift [16]. The DSP signal separation and a feedback loop for less phase error are adopted in the practical implementation [26].

A hybrid power combiner, which isolates two PAs, as shown in Figure 2-9g wastes output power unless it is at maximum power mode (180° off-phase). In other words, the PAs generate constant power regardless of the input signals but the combined output power is varied linearly with the input. Consequently, the LINC with the hybrid power combiner maintains the linearity by dissipating extra power to a ballast resistor at low power operation resulting in poor efficiency [9]. The Chireix outphasing PA is a special type of the LINC that associates load-pulling mechanism for power combining with high efficiency similar to one described in the Doherty PA – the PA1 and the PA2 provides load-pulling effects to each other [9] [16].

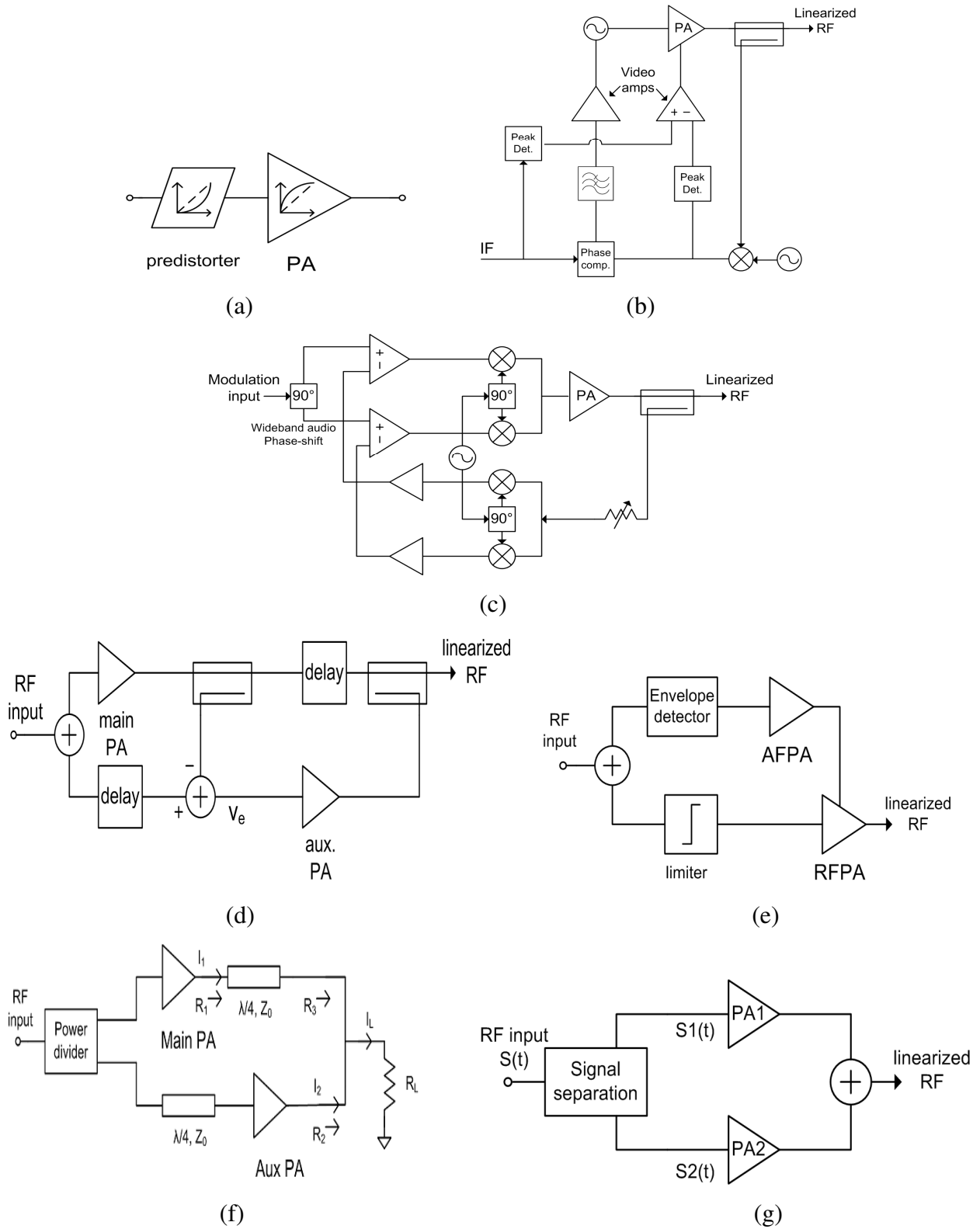


Figure 2-9: Linearization techniques: (a) predistorter technique, (b) polar loop system, (c) Cartesian loop system, (d) feedforward technique, (e) EER, (f) Doherty PA and (g) LINC

Chapter 3 - Thermal Analysis

RF PAs based on compound semiconductors such as GaAs, SiC, and GaN have been popular choices in commercial products thanks to high voltage breakdown and high gain. While there have been efforts to minimize a system size including the compound material PA and a CMOS base-band circuitry using new package techniques [27][28], research on a fully-integrated CMOS radio has also continued [29][30]. When the PA is integrated onto a single chip system, much simplified manufacturing and cost saving are obtained. However, the more CMOS processes scale for speed and power consumption, the more difficult it gets to build a Watt-level PA since thin gate metal oxide and short channel length are vulnerable to breakdown. In addition, the scaling makes heat concentrate in small areas, which results in hot spots and degrades circuit performance instantly and also gradually. For multi-Watt PA applications, thermal analysis is therefore necessary to assess heat concentration effects.

1. Thermal Fundamentals

Thermal energy transfer in a PA is composed of radiation, convection and conduction. In integrated PA application the conduction mechanism is dominant. If the heat source is distributed evenly on the entire surface of the chip and heat flows vertically as shown Figure 3-1a, temperature difference (ΔT) and thermal resistance (R_θ) of the chip can be found in simple equations.

$$\Delta T = \frac{Ph}{\kappa A} \quad (3.1)$$

$$R_\theta = \frac{\Delta T}{P} = \frac{h}{\kappa A}, \quad (3.2)$$

where P , h , and A are defined in Figure 3-1a and κ is a thermal constant.

Since the heat source is relatively small on the PA chip surface, the vertical conduction is not valid for the PA IC. As shown in Figure 3-1b, thermal resistance of the chip is better

estimated by heat spreading [31]. The spreading method estimates the average temperature of the heat source but more precise methods are needed in order to find the junction temperature of the power FETs channel and other critical regions.

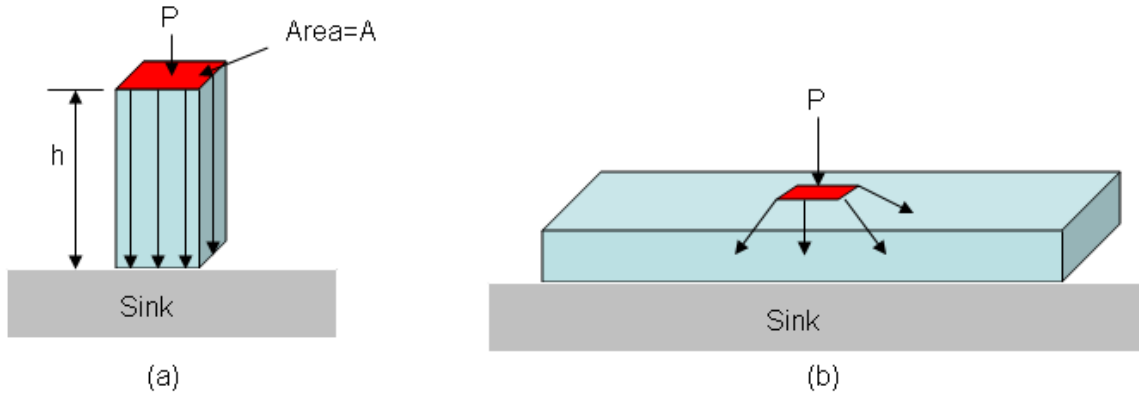


Figure 3-1: Thermal transfer: (a) vertical conduction (b) spreading

2. Thermal Analysis of Power FETs

To determine the junction temperature of multi-finger power FETs, Cooke [32] used an analogy between electrostatic capacitance and thermal resistance (Figure 3-2). Thereby, the temperature is found by a coupled transmission-line equation. Cooke's method assumes that all the fingers have the same temperature. Higashisaka [33] developed a thermal resistance formula assuming 45 degrees downward spreading heat flow. R1 and R2 are calculated by integrating infinitesimally thin substrate plate under the 45-degree roof along h-axis (Figure 3-3).

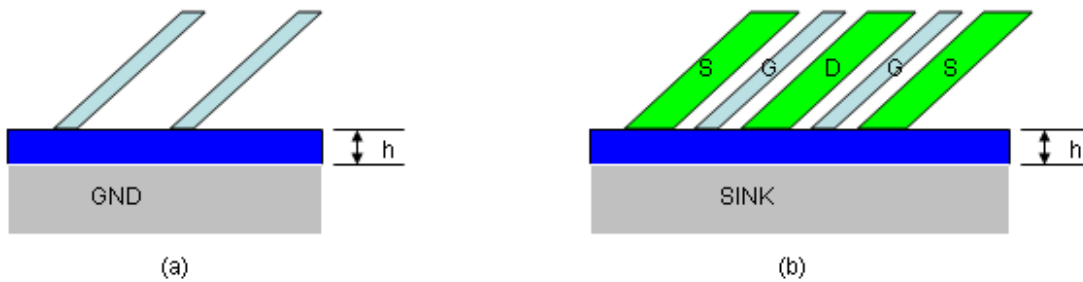


Figure 3-2: microstrip-FET analogy: (a) microstrip (b) FET, excerpted from [33]

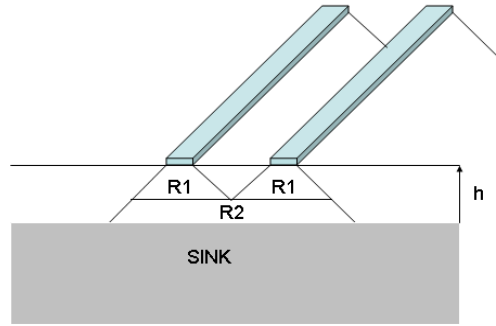


Figure 3-3: Thermal resistance model of a power FET by Higashisaka

Giving less insight, an exact solution of the temperature distribution is obtained by solving a three-dimensional partial differential equation. In steady-state, the equation becomes

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \quad (3.3)$$

Culbertson and Lehmann [33] wrote a computer program based on equation (3.3). Their surface temperature plot by the program provides important conclusions:

- i) The gate at the center peaks in temperature
- ii) The peak temperature is much higher than average temperature of the power FET
- iii) The peak temperature is tightly related with the spacing between gates.

Hence, approximation methods like Coke's and Higashisaka's have only limited use by which the average thermal resistance is evaluated. The thermal differential equation must be solved for accurate junction temperature prediction. In order to determine the temperature of the 1-Watt PA chip, a commercial software, which solves the thermal equation, is used in Chapter 7. For the other supporting materials in Figure 7-13, the vertical conduction in Figure 3-1a is assumed for calculation. The spreading is negligible since thermal adhesive and thermal compound are relatively thin and numerous vias are installed under the PA.

3. Reliability and Junction Temperature

Device failures can be ascribed to errors in manufacturing, external accidents such as static discharge, transients in a dc power supply, etc. Although these kinds of failures can be screened, there are other causes that degrade power FETs over a period of time. For instance, contact degradation, electro-migration, and channel changes under gates are all long term failure mechanisms and they are temperature activated [34]. Therefore, the tight relations between the failures and temperature can be utilized to estimate the device life by thermally accelerated aging in laboratory environments. The Arrhenius equation [35] states that

$$\ln \frac{t_{f2}}{t_{f1}} = \frac{E_a}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \quad (3.4)$$

where t_f = median time to failure, E_a =activation energy(eV), k = Boltzman's constant (8.6E-5 eV/K), and T =absolute temperature (K).

Since the failure of the transistor is complex mechanism, E_a in equation (3.4) quantifies a combination of multiple reactions such as hot carrier effects and gate oxide breakdown. Once the E_a is determined by the thermal aging experiment, the failure time in normal temperature can be estimated.

As FETs scale for high frequency operation and high gain, heat density becomes so high that the performance improvements are nullified without good heat dissipation. Although no general data on heat dissipation of integrated PAs has been reported to date, the data of microprocessors is available. Air cooling with a normal thermal interface material (TIM) can handle less than 60 W/cm², and an improved TIM or liquid cooling are necessary for higher heat density [36]. Since the heat is highly localized in the integrated PA, the heat dissipation is as important as in the microprocessors. Insufficient heat dissipation of devices might not destroy them immediately but performance degradation and short failure time are inevitable. Failure time is an especially critical issue when the devices are boarded on space applications.

4. Integrated PA Performance Degradation with Junction Temperature

The elevated temperature not only shortens the life of the devices, but it also instantly degrades an integrated PA's performance. For example, at the high temperature, parasitic source resistance (R_s) increases and transconductance (g_m) decreases, which result in reduced gain. Also, decreased drain DC current leads to less output power. Experimental results of GaAs transistor measurements have revealed that the linear gain and the output power decreases by 0.015 dB/°C and 0.008 dB/°C respectively [37], which is equivalent to 30 % output power loss by a 100 °C increase. Similarly, output power decrease has been reported in a silicon bipolar PA [38], where 1 dB output power reduction by 50 °C temperature increase was measured. Secondly dynamic junction temperature variation can distort the signal and impair linearity. As PA's output power varies in time due to modulation, the junction temperature becomes a function of a time-varying signal envelope and thermal memory effects or asymmetric IM (intermodulation) products are unavoidable. The effects are also called thermal power feedback [39]. The nonlinearity by the temperature is troublesome because an exact junction temperature detection/compensation is difficult to achieve.

In Chapter 7, the thermal analysis of the 1-Watt PA is presented, where a thermal simulator is utilized for SOS and GaAs substrates. Thereafter, related tests such as a pulsed operation, a low temperature test, and a reliability test are followed in Chapter 8.

Chapter 4 - Stability Analysis of Nonlinear Power Amplifiers

Common wisdom often expressed by RF designers states that “Amplifiers oscillate and oscillators don’t.” It is not surprising that a PA can become an oscillator since the PA has, when examined with all parasitics included, many similarities in the topology with many well-known feedback circuits such as the Hartley and Armstrong oscillators. When the PA forms unfortunate feedback paths by capacitive, magnetic coupling, power supply lines and so on, oscillation may occur. Therefore, the PA’s stability must be analyzed in the design phase.

1. Linear Amplifier Stability

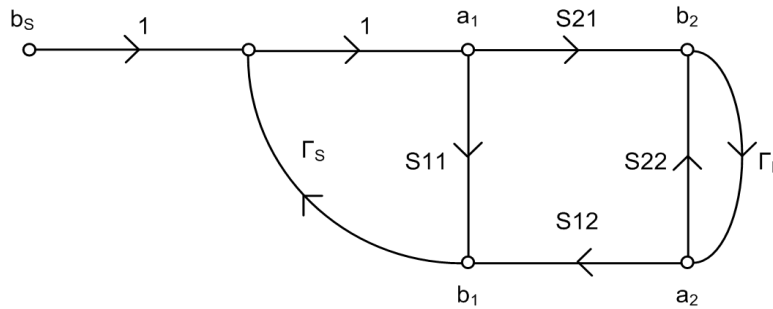


Figure 4-1: Signal flow path for two-port network, redrawn from [40]

When RF signal power is so small that the amplifier has a linear transfer function, unconditional stability can be decided by S-parameters of the amplifier and k -factors. The conditions are [40]

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1, \quad (4.1)$$

$$|\Delta| < 1, \quad \Delta = S_{11}S_{22} - S_{12}S_{21}, \quad (4.2)$$

which are derived from Figure 4-1 to satisfy the following inequalities. Those are:

$$|\Gamma_{in}| = \left| \frac{b_1}{a_1} \right| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \quad |\Gamma_{out}| = \left| \frac{b_2}{a_2} \right| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \quad (4.3)$$

for all passive source and load impedance. In the signal flow path, b_S is signal from the source, Γ_S and Γ_L are reflection coefficients by the source and the load.

2. Nonlinear Stability

Large-signal S-parameters

Since the S-parameter data is given under the linear circuit assumption, it does not consider harmonics; therefore, neither compression nor intermodulation effects are included. Fortunately, a commercial RF software such as Agilent ADS can generate large-signal S-parameters for heavily nonlinear circuits such as oscillators, mixers and PAs based on Harmonic Balance (HB) simulation [41]. The large-signal S-parameter is not only a function of frequency, but also depends on power level of ports. In Chapter 7, the stability of the 1-Watt PA with different input power is tested by large-signal S-parameter analysis.

Auxiliary Generator Analysis Method

We can also find the oscillation condition in terms of admittance instead of the S-parameters. When the PA has entered a free running oscillator state, relations between reflections coefficients are [42]

$$\Gamma_S \Gamma_{in} = 1, \quad \Gamma_L \Gamma_{out} = 1 \quad (4.4)$$

implying $|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$ since $|\Gamma_S|$ and $|\Gamma_L|$ are less than unity. The oscillation conditions are derived from the signal flow in Figure 4-1 and equation (4.4) and

$$\frac{b_1}{b_S} = \frac{\Gamma_{in}}{1 - \Gamma_{in}\Gamma_S} \quad (4.5)$$

The correlation implied by equation (4.4) can also be written as

$$R_{in} + R_S = 0, \quad X_{in} + X_S = 0, \quad (4.6)$$

when $Z_{in} = R_{in} + jX_{in}$ and $Z_S = R_S + jX_S$, resulting in

$$Y_{in} + Y_S = 0. \quad (4.7)$$

When the HB simulation is used to find a free-running oscillation, the circuit may converge to DC solution because a bias source forces the solution or to a mathematical solution without physical existence [43]. However, using an auxiliary generator in the HB simulation, the oscillation condition in the nonlinear circuit can be determined with or without an RF input source as shown in Figure 4-2 because the auxiliary generator keeps the circuit from converging into the DC solution [43]. In order to prevent shorting the node m to ground for harmonics, a band-pass-filter at the fundamental frequency is inserted between the auxiliary generator and the node m. The frequency and amplitude of the oscillation that satisfy the equation (4.7) can be found in a parameterized sweep. Furthermore, an admittance diagram, parameterized by the sweeping frequency and amplitude, illustrates how the oscillation evolves to a steady state: a synchronized oscillation or a free-running oscillation.

Examining the total admittance at node m, $Y_T = I_{AG}/V_{AG}$, it is found that the oscillation starts up where

$$\text{Re}(Y_T) < 0 \quad \text{and} \quad \text{Im}(Y_T) = 0, \quad (4.8)$$

and enters steady state oscillation at $Y_T = 0$ as already described in equation (4.7). Since the HB simulation is performed, nonlinearity of the circuits is already taken into account as it separates the circuit into linear and nonlinear parts and equates in the frequency domain [44]. The auxiliary generator method has been used to analyze a Ku-band VCO [45], bifurcation of a switching PA, and to implement a stabilization network [46]. In Chapter 7, the auxiliary generator method is used to investigate the possibility of a self-oscillation when no RF input is given. In addition, the

large-signal S-parameter simulation is carried out for stability analysis with input sources of different levels.

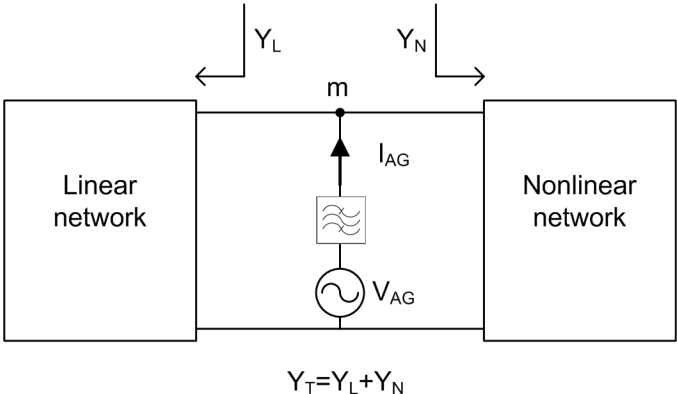


Figure 4-2: Auxiliary generator method for tracing the admittance diagram, redrawn from [43]

Chapter 5 - Silicon-on-Sapphire Process

In this research, the silicon-on-sapphire process from Peregrine Semiconductor is chosen in the 1-Watt PA design due to its unique advantages over the bulk CMOS process.

Regular digital-friendly bulk silicon CMOS process has a low resistance substrate to prevent latch-ups as shown in Figure 5-1a. However, when an inductor is fabricated on the silicon substrate, the capacitive coupling path between the inductor's metal layer and the substrate becomes a dominant loss contributor. The quality factor of the inductor on the silicon substrate is much less than five [47] at low UHF band. On the other hand, a sapphire substrate, shown in Figure 5-1b, is completely insulating and eliminates the loss by R_{sub} in Figure 5-2a. The inductor can be represented by a simpler model with only R_s loss in Figure 5-2b when current crowding effects are minor [48]. Q higher than 20 at S-band, which is approximately twice as high as that of the inductor on silicon substrate with similar dimensions, has been reported [48]. The inductor layout and a Q plot are shown in Figure 5-3. The high Q on-chip inductor/transformer is a key component in order to integrate RF front-end circuits: resonant TR switch, LNA and PA. Moreover, the SOS process has unique advantages over the bulk CMOS process for system-on-a-chip applications such as those in which this work was conducted.

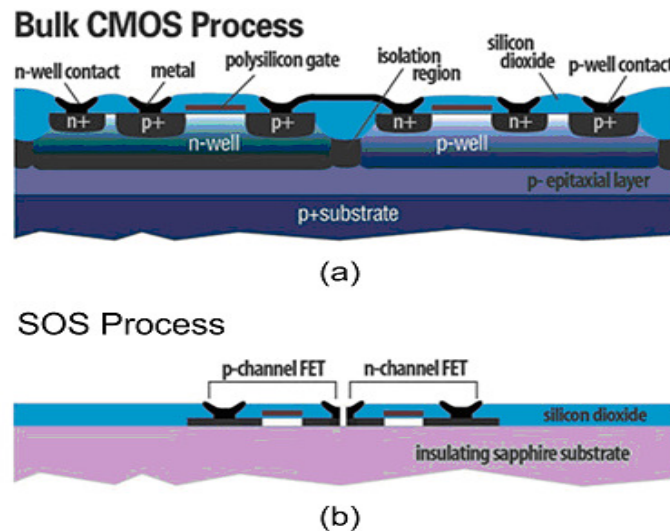
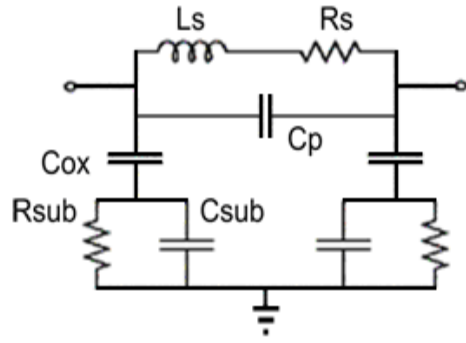
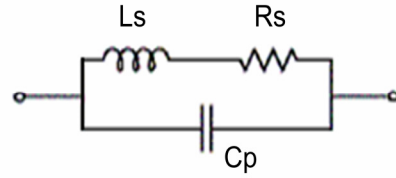


Figure 5-1: Active devices and substrate structure in (a) bulk silicon CMOS process and (b) SOS process [49]

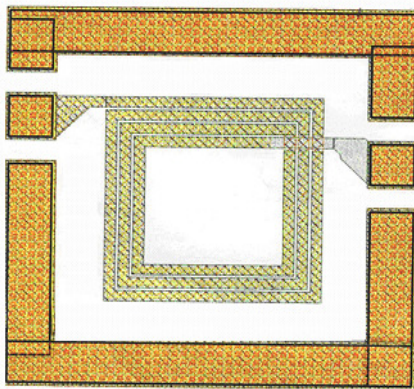


(a)

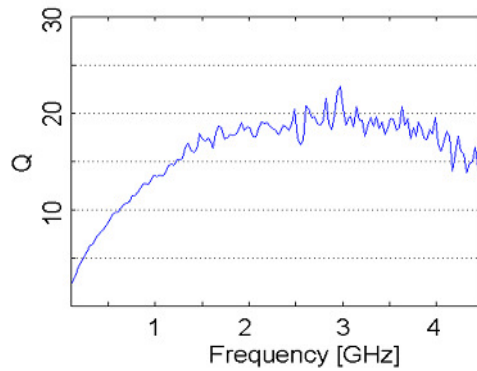


(b)

Figure 5-2: Schematic models of inductors on (a) bulk silicon CMOS process and (b) SOS process



(a)



(b)

Figure 5-3: Spiral inductor in SOS. (a) test structure of a $450 \times 450 \mu\text{m}^2$ inductor. (b) Q plot.

1. Transformer Efficiency

As already mentioned in equation (2.7), the efficiency of the transformer is strongly dependent on Q , and is only 61 % when $Q = 5$. It is obvious why many CMOS PAs could not be fully integrated [11] [50] [51]. If an on-chip transformer of $Q = 20$ is possible, using a process such as SOS, efficiency will reach 88 %. That is only less than 10 % short of the efficiency of bondwire and microstrip line according to Table 2-2.

2. Breakdown Voltage of PMOS FET

Another advantage of the SOS process is that PMOS has very high breakdown voltage (V_{bk}). Along with the 1-Watt PA, a stacked PMOS test structure was fabricated and tested. The

dimension of the power cell is same as the one used in the PA, 20000um/0.5um. Die photo and schematics are shown in Figure 5-4. In a DC I-V test, as depicted in Figure 5-4c, the PMOS stacked transistors were destroyed and sudden I_D increase was observed when V_{D_CG} is increased to 12 V and V_{G_CG} is fixed at 3.3 V. Since V_{SD_CS} is approximately 3 V with low V_{TH} and negligible overdrive voltage ($V_{TH} + \Delta V \approx 0.3V$), the V_{bk} of PMOS is 9 V. Since low load transform ratio (N) is needed with the high V_{bk} , the transform efficiency improves both in a LC network and a transformer as described in Chapter 2.

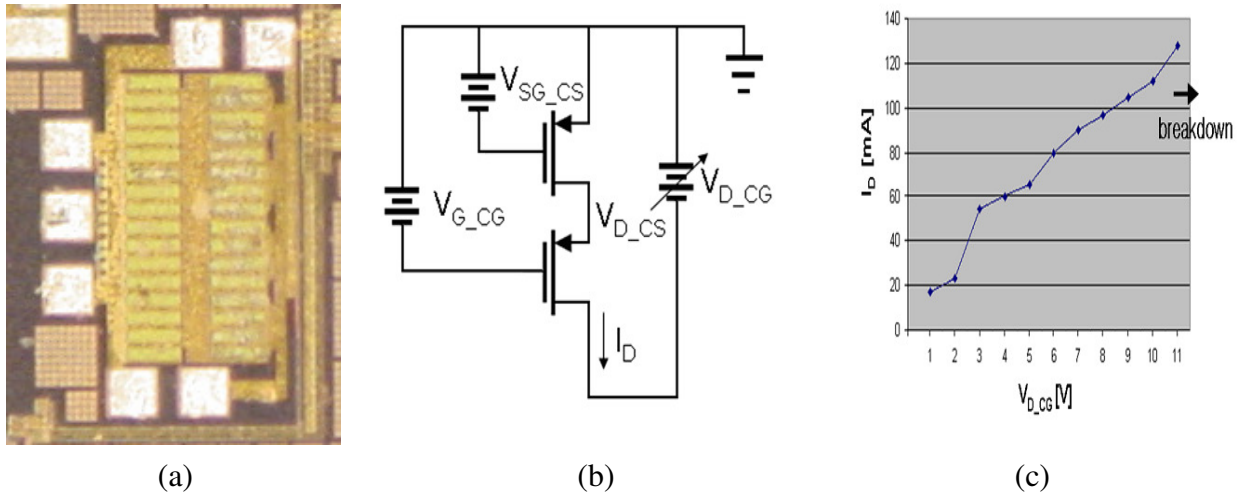


Figure 5-4: Breakdown voltage test of the PMOS stacked transistors. (a) Die photo, (b) schematics. $V_{SG_CS}=0.3V$, $V_{G_CG}=3.3V$ and $W/L=20000/0.5$. (c) I_D vs. V_{D_CG} plot.

3. Parasitic Drain Capacitance

Transistors in a Watt-level RFPA occupy sizable chip areas to accommodate large current. Therefore, there exists significant parasitic diode junction capacitance between drain and substrate (C_{DS}). Instead of fighting the parasitic capacitance, it can be utilized in PA design. For example C_{DS} provides harmonic short for class-A, AB and B PA and can be merged to a parallel tank in a current-switching class-D. C_{DS} is also mandatory in a class-E PA to meet the ZVS conditions. However, the junction capacitance is not a linear component, and aggravates nonlinearity as high voltage swing is needed. Although nonlinear C_{DS} is less problematic than gate capacitance, it increases IM3 products in class-AB PA [52]. Moreover, when it comes to a class-E PA, it lowers output power [53] and raises drain voltage higher, consequently lowering normalized power output capability [54]. In addition, output voltage is no more a linear function

of supply voltage with the nonlinear C_{DS} [55], which impairs a linearization technique using bias modulation such as EER in Figure 2-9e. Conversely the SOS process does not create the junction capacitor in the absence of the resistive substrate. The only capacitance exists between drain and source metal layers, and the capacitance is linear.

4. Radiation Tolerance

Finally, the SOS generates very few electron-hole pairs under radiation since it has an Ultra-Thin Silicon (UTSi®) layer on sapphire [49]. Its radiation hardness is well suited in the Mars application [56] [57].

Chapter 6 - A Drive-amplifier and TR Switch Design

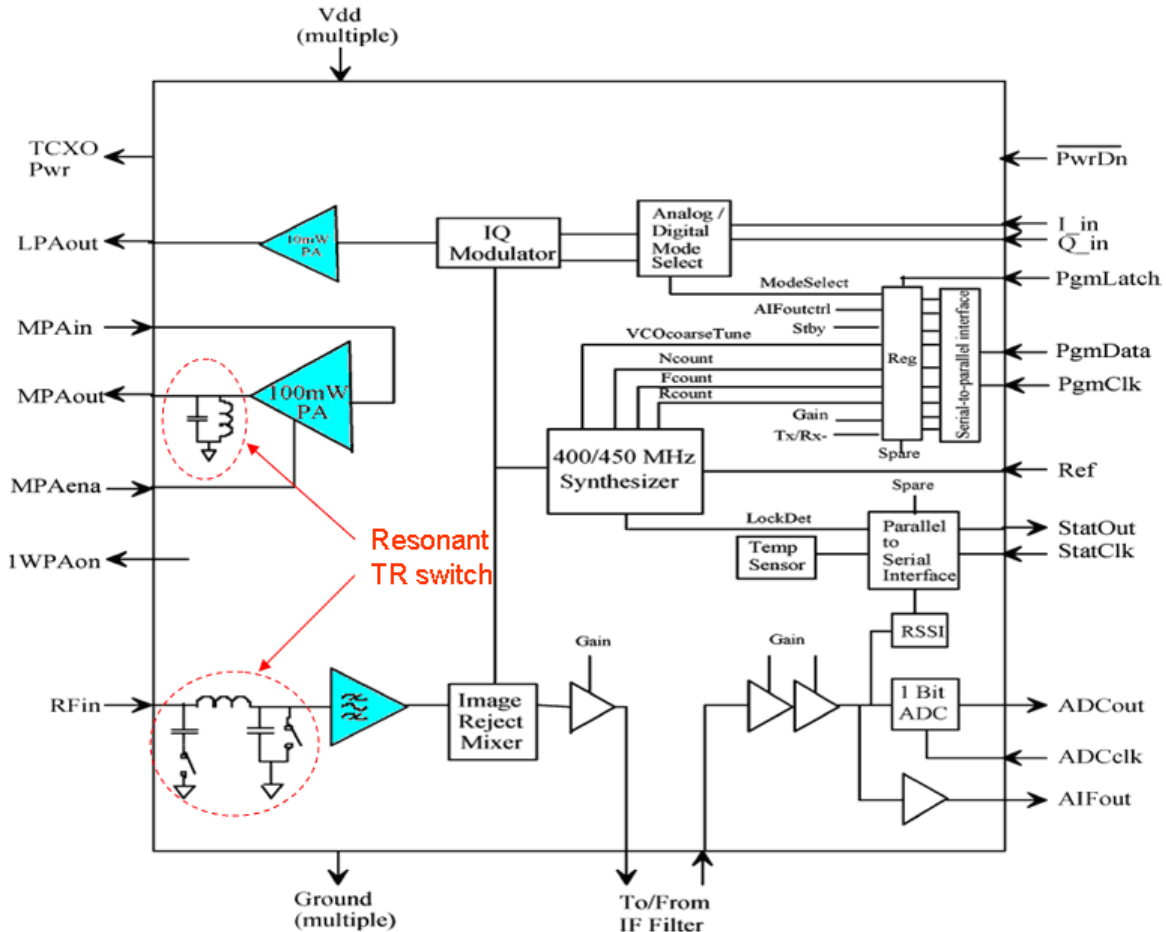


Figure 6-1: RFIC block diagram, redrawn and modified from [58].

As already introduced, the microtransceiver includes three ICs: an RFIC, a digital IC and an optional 1-Watt PA to minimize the number of components, thus achieving the low mass, low volume, and low power goal. In order to build a single chip high power radio ultimately, a space-qualified Silicon-on-Sapphire (SOS) CMOS process is selected for this work.

There are a few challenging circuit blocks in transceiver architecture for CMOS integration. A PA, a TR switch, and a front-filter are often implemented off the chip due to the reasons like low breakdown voltage, lack of a high Q resonator, and high loss in transistor channel. However, as shown in Figure 6-1, drive-amplifiers – a 10mW low power amplifier

(LPA) and a 100mW medium power amplifier (MPA) – and the TR switch were able to be integrated due to insulating substrate in SOS process and the resonant TR switch technique [59]. When 100mW output power is needed, a complete transceiver is implemented by connecting MPAout and RFin in Figure 6-1, where both face the antenna.

The RFIC in the Mars microtransceiver circuit includes a fully integrated radio front-end and the optional 1-Watt PA can be attached to it to boost the output power level. This chapter describes the front-end circuitry and the resonant TR switch techniques in Figure 6-1 when the MPA is directly connected to the antenna and the LNA (Low Noise Amplifier).

The author acknowledges that much of this chapter is taken from his paper [59] in observance of the IEEE copyright policies and that the LNA is designed and tested by his advisor, William B. Kuhn.

1. CMOS Resonant TR Switch – Background and Analysis

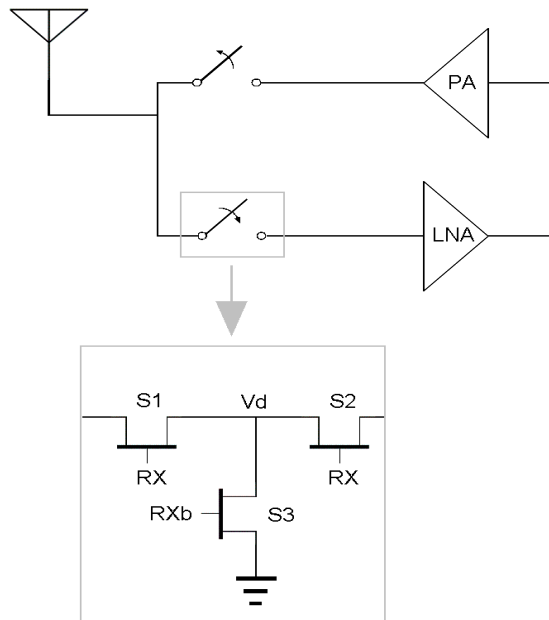


Figure 6-2: Traditional GaAs FET T/R switch

Although a time-division duplexing (TDD) system and a half-duplexing system can eliminate a bulky duplexer filter, they need switches along the path from antenna to RF front-end. The traditional GaAs switch shown in Figure 6-2 isolates the PA and the LNA by non-

overlapping control signals. At receive mode RX is high and S1 and S2 connect the LNA and the antenna and RXb opens S3. The switch between the antenna and PA is set in the opposite way, removing the path to the PA. At the transmit mode S1 and S2 open and S3 closes to ground. The method protects the LNA from high voltage PA output by opening the path (S1 and S2) and effectively grounding Vd (S3). However, S1 and S2 involve transistor on-resistance loss when closed and degrade PA output and LNA noise performance. In addition, the method cannot be used in typical CMOS processes because S1 has to stand high V_{ds} at transmit mode. A new technique has shown that matching networks and switching functions can be combined in a CMOS LNA [60]. The method is expanded to the PA and it makes a complete T/R switch at RF front-end.

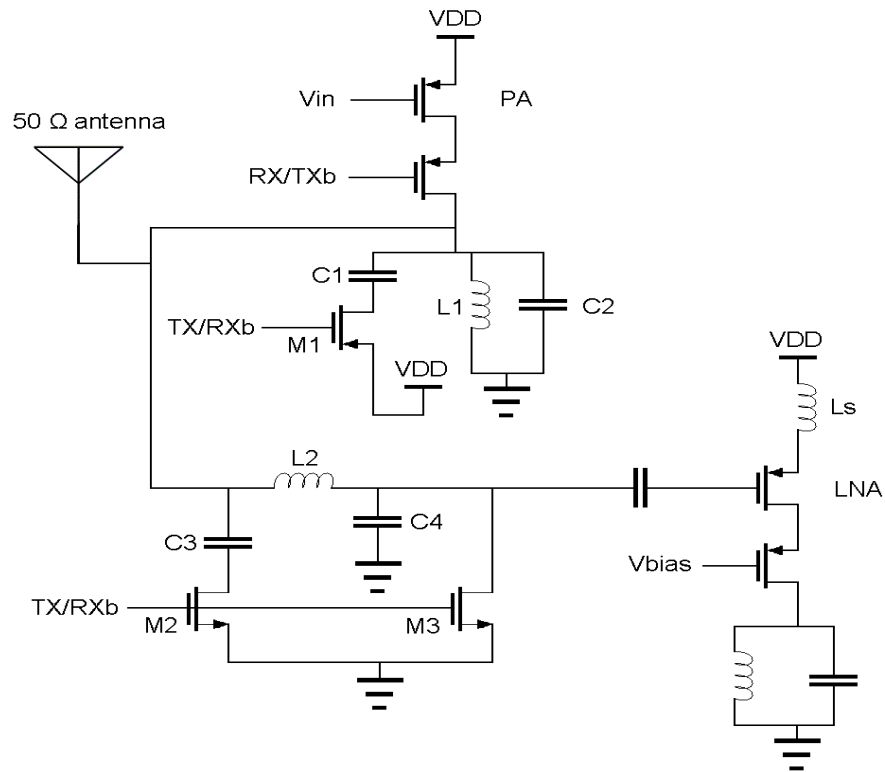


Figure 6-3: Proposed T/R switch

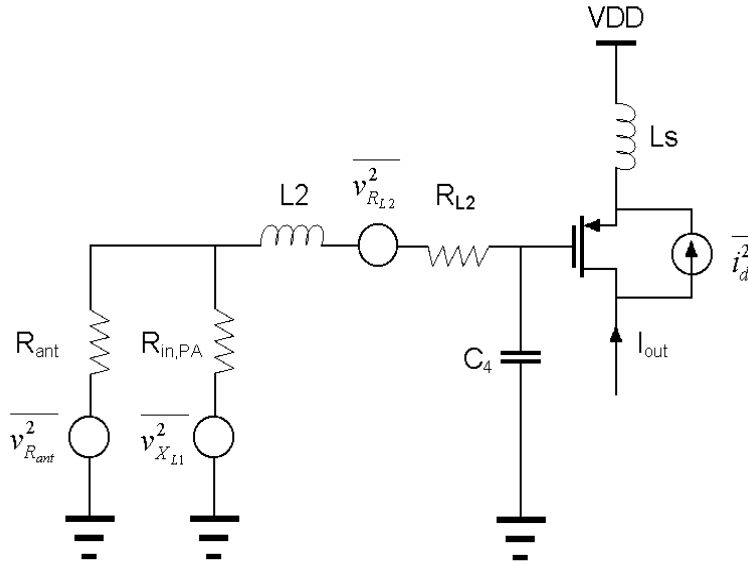


Figure 6-4: Noise model of the LNA

The full T/R switch with simple PA and LNA is shown in Figure 6-3. The half-duplex transceiver operates at 400 MHz and 435 MHz for transmit and receive respectively. The PA has stacked PMOS transistors in order to sustain high voltage at the antenna node without using load resistance transformation. A high efficiency switching mode PA is possible without an RF choke inductor if output reactance is tuned to minimize transistor loss [9]. Inductor L1 together with capacitor C2 in the PA forms parallel resonance for the modified class-E PA mode and maximizes efficiency at transmit mode. At the same time, M2 and M3 close and a parallel resonant circuit is composed of L2 and C3 at the LNA side. If sufficiently high Q inductor is available, $Z_{in,LNA} \gg R_{ant}$ and the transmit power loss to the tank is minimized. Suppose that $R_{in,LNA}$ is the effective resistance of the LNA's input in transmit mode. Then loss contributed by the LNA's switch is

$$\frac{P_{loss}}{P_{out}} = \frac{V_{ant}^2 / R_{in,LNA}}{V_{ant}^2 / (R_{in,LNA} \parallel R_{ant})} \quad (6.1)$$

Since L2 is fairly large in order to match LNA input to 50 Ω , $R_{in,LNA}$ will be relatively large when it is resonated with C3 during transmit mode and P_{loss}/P_{out} can be held to less than 10 % or 0.5 dB [60].

An inductive source degeneration technique [61] is used for the LNA as shown in Figure 6-3. However, unlike traditional implementations where the goal is a 50 Ohm input to match to a front-end filter, here inductance at the source is chosen to result in a high input resistance at the PMOS gate and it is matched to the source resistance by L2-C4 L-type impedance step-up network. Series resistance in Ls can be neglected if Ls has high Q and total noise output power density is contributed by R_{ant} , $R_{out,PA}$, series resistance R_{L2} in L2, and MOS channel current noise. The noise factor of the circuit can be analyzed from the noise model in Figure 6-4 [61] as

$$F = \frac{\text{total output noise}}{\text{total output noise due to source}} = \frac{S_{no,R_{ant}} + S_{no,R_{out,PA}} + S_{no,R_{L2}} + S_{no,R_{id}}}{S_{no,R_{ant}}} \quad (6.2)$$

The addition of $R_{out,PA}$ in parallel with R_{ant} does not change the total output noise due to the source significantly, but the total output noise increases by $S_{no,R_{out,PA}}$. Therefore, to avoid degradation of the LNA noise factor, the effects of $R_{out,PA}$ must be minimized and high Q parallel resonance at the PA output is required. The NF degradation by $R_{out,PA}$ is mathematically analyzed in Appendix C.

2. Design and Implementation

The transceiver with TR switch is implemented in 3.3 V Peregrine CMOS SOI process. The schematics of the PA in the transceiver chip are shown in Figure 6-5. The first stage is an inverter to generate fast switching input to the second stage. The PMOS transistors are stacked in the second stage. The PMOS has higher breakdown voltage than NMOS in this process. Thus, it can tolerate safely more than 20 dBm output power at drain. The PMOS is also a lower channel noise source [62] so it adds less noise to the LNA when it is shut down. Taking advantage of thick top metal layer, L1's inductance and Q are approximately 15 nH and 13. At transmit mode L1, C2 and parasitic capacitance C_{ds1} and C_{ds2} form output tuning. The size of L1 is decided

initially for class-E operation, and then load-pull simulation is carried out to find the optimum efficiency point. Since the output network is inductive for soft switching, C1 should be added to the circuit at receive mode even though the receive frequency is higher than the transmit frequency. The LNA is also designed on the transceiver chip (Figure 6-6). Inductive source degeneration and L-section network match the LNA to 50 Ω input. Cascoding transistors increases voltage gain and makes the circuit more stable by isolating input and output. L3-C3 tank boosts voltage swing before the gain stage. On-chip spiral inductors are used for L1, L2, and L3. Their specifications are 80 nH ($Q = 10$), 72 nH ($Q = 7$), and 220 nH ($Q = 5$) respectively. Two 18-turn spiral inductors are series-connected to make L3 so its Q is lower than others. The gain stage is a cascoded differential amplifier with active load M10 and M11. It adds not only signal gain, but also converts single-ended signal to differential signal. A buffer stage follows.

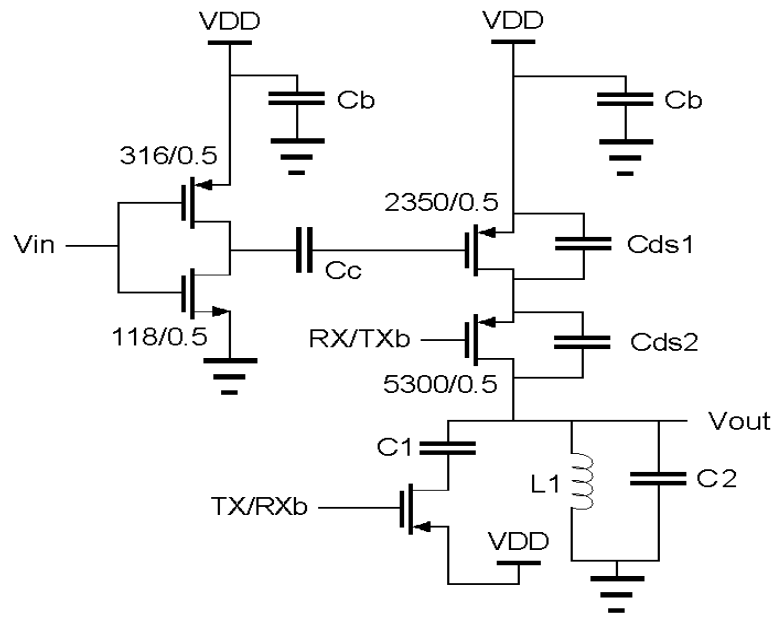


Figure 6-5: Power amplifier schematics

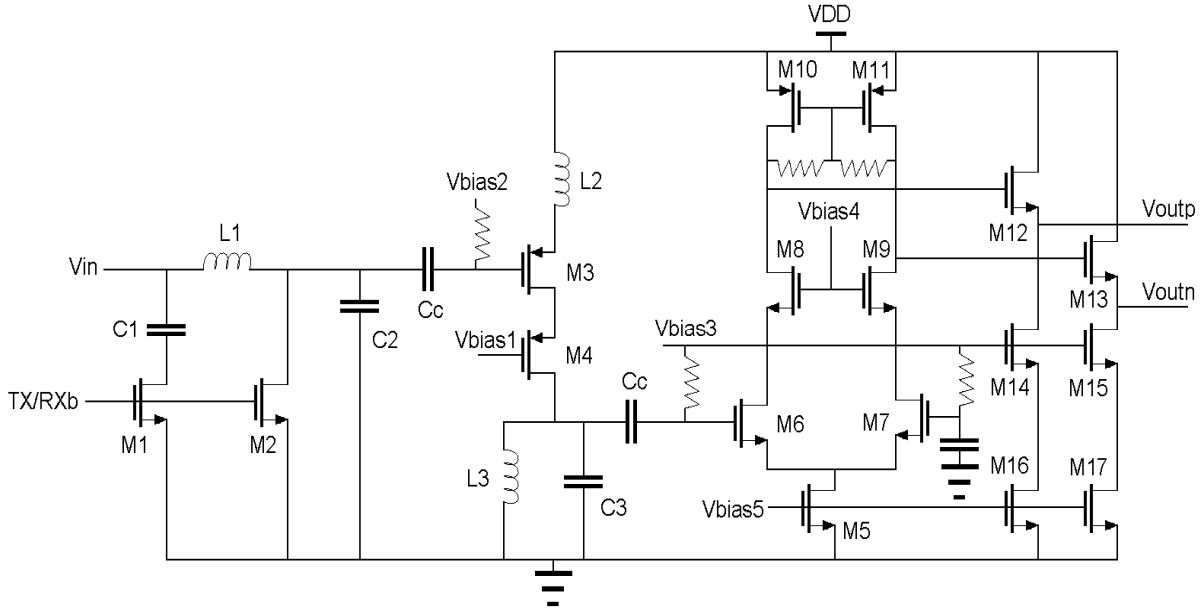


Figure 6-6: Low-noise amplifier schematics

3. Measurements

The die photo of the transceiver is shown in Figure 6-7. The size of the die is $1.5 \times 3.0 \text{ mm}^2$. The transceiver was packaged and tested on the FR4 PCB board. The transceiver's PA delivers 19 dBm to 50Ω load at the 10 dBm input and PAE is approximately 36 %. The measurement shows that PAE peaks at 9 dBm input (Figure 6-8a). S_{11} of the PA at receive mode is 300Ω (Figure 6-8b). Measured LNA S_{21} gain is 22 dB with -50 dBm input (Figure 6-9a). Hot/cold noise measurement method was used and NF was 3.4 dB at room temperature. Referring to Appendix C and the NF degradation plot (Figure 7-5), the NF should degrade by 0.7 dB by the PA's 300Ω output resistance. 1-dB compression point is -40 dBm. The LNA draws 2.5 mA at the 3.3V power supply excluding 50Ω output buffer used in testing. S_{11} at transmit mode is shown in Figure 6-9b. The measured S_{11} is $1 \text{ K}\Omega$ and it is equivalent to less than 5% (0.25 dB) transmit power loss from equation (6.1).

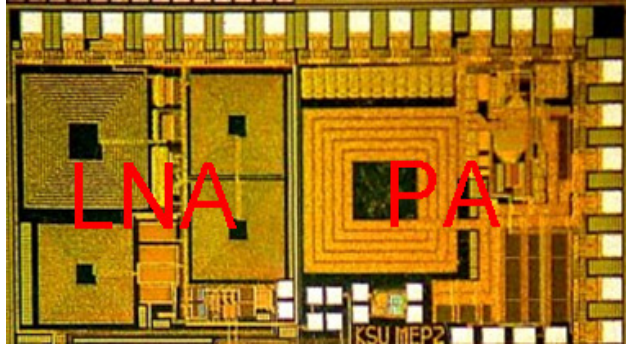
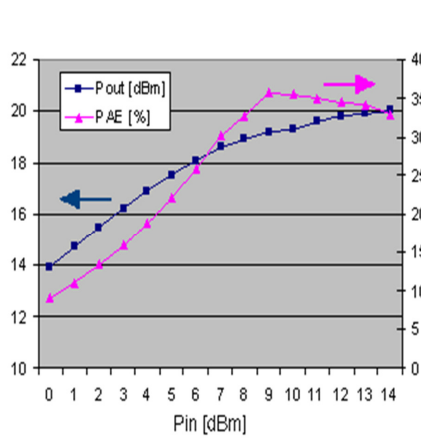
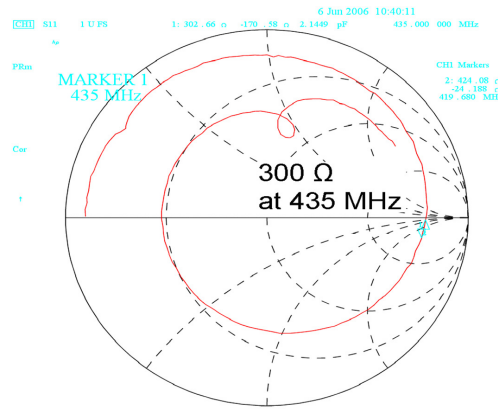


Figure 6-7: Die photos of the transceiver.

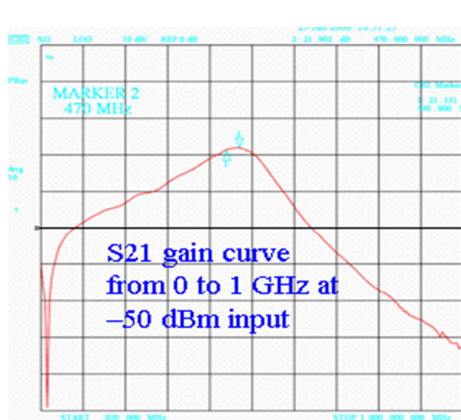


(a)

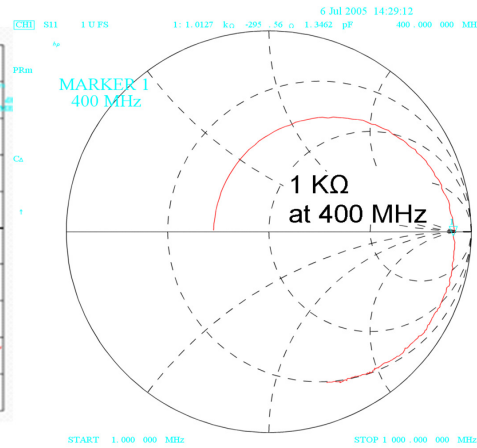


(b)

Figure 6-8: The transceiver's PA measurement (a) P_{out} and PAE at transmit mode (b) S_{11} at receive mode



(a)



(b)

Figure 6-9: LNA measurement (a) gain at receive mode (b) S_{11} at transmit mode

Chapter 7 - Design of 1-Watt UHF Power Amplifier

Although a CMOS process is not the best fit for the RF power amplifier design, research on the Watt-level CMOS RF PA has been continued. Not only is the CMOS process cost-effective, but it is also considered to provide a single chip radio solution by its compatibility to both digital and analog circuitry. This chapter discusses the design challenges for the Watt-level PA in CMOS process and presents the design techniques devised for the optional 1-Watt PA in the Mars microtransceiver project.

The RFIC chip in Chapter 6 drives the 1-Watt PA in the Mars microtransceiver and the TR switch function is maintained in a PCB level using a microstrip line.

The PA is the first fully integrated Watt-level CMOS power amplifier in UHF 400 MHz band at the author's knowledge. The author also acknowledges that much of this chapter is taken from his paper [63] in observance of the IEEE copyright policies.

1. Prior Art

Efforts to build a Watt-level CMOS PA are found in numerous papers. 1-Watt output has been successfully demonstrated in the 1.9 GHz cellular frequency band [64]. Due to the loss of silicon substrate, bondwire inductors and a microstrip-line balun were utilized. A similar level of performance was also achieved in a single-ended structure at 1.8 GHz with comparable use of off-chip components [65]. Yoo has shown that a common-gate switching technique can avoid CMOS's low voltage breakdown problem in a 900 MHz 0.9 W PA [11] and a very high efficiency fully differential PA was reported by Mertens [51]. However, both have to depend on off-chip circuit components or be forced to interface a differential antenna nearby in the absence of high quality inductor/balun. A fully integrated 2.4 GHz 2.2 W CMOS PA was reported by Aoki where a distributed active transformer (DAT) combines outputs of four circularly laid out differential pairs [66]. The DAT technique fits well for the 2.4 GHz application, but the Mars transceiver's much lower operating frequency (400 MHz at TX, 435 MHz at RX) makes it difficult to fit such structure on a $3 \times 3 \text{ mm}^2$ die. The following section discusses challenges in CMOS integration of UHF Watt-level PAs.

2. CMOS RF PA Design Challenges

A fully integrated Watt-level CMOS RF PA has been a formidable task due to barriers given by CMOS processes. In order to deliver higher output power the net size of the transistors must increase proportionally. Because the CMOS FET does not have as much transconductance as GaAs FET, very wide gates are needed and associated large gate capacitance becomes hard to match. Moreover, when multiple transistor cells are used, parasitic inductance and resistance in input distribution networks drop capacitive input Q , adversely increasing input conductance. Similarly bondwire parasitic inductance becomes substantial when they are connected to off-chip signal ground, resulting in ground bouncing and gain degeneration. A differential structure alleviates the bondwire problems by setting virtual ground on the chip.

For Watt-level output with $50\ \Omega$ load, voltage swing is larger than $10\ V_{\text{peak}}$. GaAs FET and LDMOS can handle much higher drain-source voltage than the CMOS FET and multi-Watt PAs have been reported without efforts to reduce the drain voltage swing in these processes [20] [67] [68]. However, the CMOS transistors would be broken by the stress in the same drain voltage. Therefore, it is required to utilize techniques such as transistor stacking, output transformation, and/or combinations of multiple outputs.

Stability issues must also be considered. Since the PA creates a variety of input/output feedback paths through magnetic coupling, and the transistor's parasitic capacitance and signal level is very large, a careful layout and modeling including a test board are essential before fabrication. Finally, heat dissipation in the PA is a complicated problem due to the concentration of heat at the multi-finger transistor channel regions. If we assume a fully integrated PA has 50% drain efficiency and 1 W output, although it is not very easy in CMOS, the PA must dissipate 1 W as heat. The heat must be spread away from the transistor junction as fast as possible or the temperature increase in the devices results in carrier mobility reduction and degrades overall performance.

Whereas innovative design strategies are needed to address many of the aforementioned challenges, some of them can be relieved by using an RF-aware CMOS process. In this project Silicon-on-Sapphire (SOS) is used due to its potential for high quality inductors [48].

3. Stacked PMOS Class-E/ F_{odd} PA Design

Designing a CMOS RF PA involves close attention to efficiency, signal swings, device breakdown, and inductor Q .

Selection of RF PA Class for Good Efficiency

In the absence of supporting linearization systems, linearity of an RF PA is often sought in a class-AB mode design. The RF CMOS class-AB PAs have reported approximately 30 % PAE with satisfactory linearity for their application objectives [6] [69] [70]. On the other hand, there are nonlinear-mode PAs such as class-D, class-E, class-F and so on. In the latter modes, the transistors are saturated and the output power is not proportional to the input power – instead it is a function of power supply voltage. By giving up linear input/output relations, these PAs theoretically convert all the DC power into RF output power without loss, and they are suitable for systems with constant amplitude modulation such as GMSK, unfiltered BPSK, QPSK, and residual-carrier BPSK used in spacecraft systems.

Space systems based on the Proximity-1 Space Link Protocol [71], which the Mars exploration project uses, have relaxed linearity requirements. Thus, a nonlinear mode PA is chosen for the project. Although the PA using nonlinear modes can acquire 100 % efficiency in theory, practical limitations keep the efficiency well below perfection. For example, the class-D mode has been rarely implemented in RF CMOS because its finite switch transition time and parasitic capacitance results in high drain voltage and current product [44]. Multi-harmonic tuned class-F mode is not practical in monolithic implementation since the additional on-chip harmonic resonators involve more loss rather than increasing the efficiency. However, the class-E mode was originally invented to achieve no switch transition loss and needs only one resonator at its output network. Moreover, a differentially driven class-E with finite RF choke inductors has extra advantages such as less sensitivity to bondwire parasitics, good even-order harmonic rejection, and lower peak drain voltage. A class-E/ F_{odd} mode provides the same benefits of the differential class-E in a compact circuit [72].

In this thesis, the class-E/ F_{odd} mode is chosen for high efficiency and reproducibility. A Watt-level output PA is realized without violating break down voltage (V_{bk}) limit through the use of stacked PMOS devices for high V_{bk} , differential topology, and an on-chip transformer as

shown in Figure 7-1. Output network is tuned for class-E/ F_{odd} mode initially and load-pull simulation is carried out.

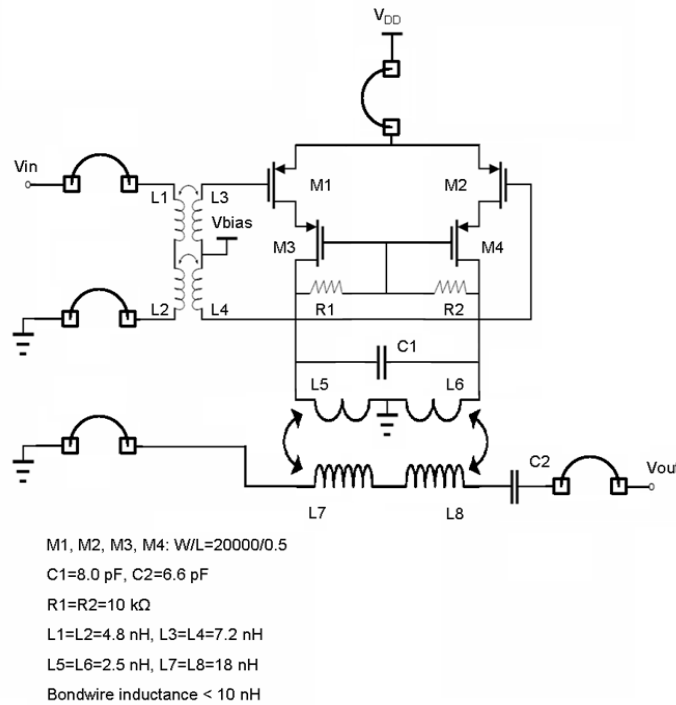


Figure 7-1: The stacked PMOS class-E/ F_{odd} PA schematics. Inductance and coupling coefficient are extracted from an EM simulator ($k_{L1,L3} = k_{L2,L4} = 0.73$ and $k_{L5,L7} = k_{L6,L8} = 0.75$).

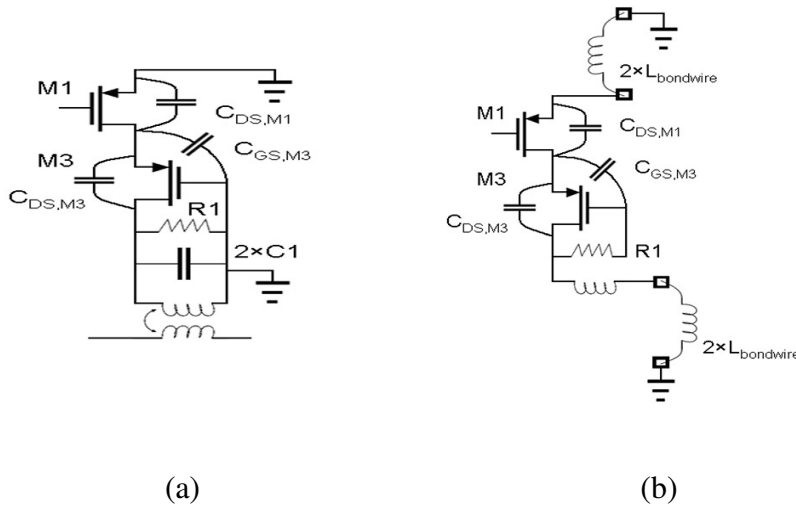


Figure 7-2: Half circuit schematics (a) at fundamental and odd harmonics and (b) at even harmonics.

Signal Swing and Breakdown Issues

As a CMOS process scales, its drain-source V_{bk} tends to scale. For example, at 0.35 μm , transistors may break down at around 4 V, while at 0.18 μm devices would fail at only 2 Volts. Fortunately, in the selected SOS process, good high frequency performance exceeding that of 0.35 μm bulk CMOS is achieved at 0.5 μm [57]. Moreover, measurements show that the PMOS transistor's V_{bk} is well above 4 V in Chapter 5. Although the high V_{bk} of the PMOS device is traded with lower transconductance and higher switch resistance, the drain efficiency (DE) of the PA can still improve with higher power supply [11]. The PMOS devices therefore form the core of the PA design in this application and the added voltage swing afforded by them is leveraged to achieve the desired 1-Watt output on a single 3.3V supply.

The schematic of the implemented stacked PMOS class-E/ F_{odd} PA is shown in Figure 7-1. Two transformers are series-connected for the input balun (L1, L2, L3, and L4) and they are wound in opposite directions to minimize the effects of magnetic coupling with the output transformer. Otherwise the coupling would degrade performance and in worst case could cause instability.

The differential structure provides a near virtual ground to the common-source, mitigating gain reduction by bondwire inductive degeneration. The virtual ground at the output keeps the RF currents in the primary coil from entering the GND bondwire improving immunity of the design to bondwire inductance. The PMOS differential pairs are stacked to allow high voltage swing at the primary and the common-gate transistors are self-biased by a resistor-voltage-divider without extra bondwire connection to ground. Large R1 and R2 have little effect on the load circuit at the fundamental and odd harmonics and a virtual ground develops at the common-gate as shown in Figure 7-2a. At the even harmonics the currents in both sides of the primary coil flow into the center-tap and no voltage or current develops in the secondary coil. Hence the drain of M1 sees very high impedance toward the transformer leaving $C_{\text{DS},\text{M1}}$ as dominant load effectively as shown in Figure. 7-2b.

Although V_{bk} of PMOS is as high as 9 V as shown in Figure 5-4, v_{SD} is limited not to exceed 5 V for reliability since high voltage swing can result in gate oxide breakdown, which is approximately 6 to 7 V for 100 angstroms-thick oxide [73].

Transformer Design

The output transformer matches the load impedance for 1-Watt output and combines the differential output into the single-ended. In order to find the load-transform ratio, it is initially assumed that the transformer efficiency is 70 %. If we further assume that the differential voltage on the stacked PMOS's is a $(3.3 \times 2) V_{\text{peak}}$ sinusoid, the load resistance needed for the 1-Watt output is approximately 16 Ohms from equation (7-1).

$$\frac{(2 \times V_{DC})^2}{2R} = \frac{P_{out}}{\eta_T / 100}, \quad \frac{(2 \times 3.3)^2}{2R} = \frac{1}{0.7} \quad (7-1)$$

For the maximum transformer efficiency, the inductance of coils are decided from the following equation [12]

$$\omega L_{pri} = \frac{R_{load} / n^2}{\sqrt{Q_{sec}^2 + \frac{Q_{pri}}{Q_{sec}} k^2}}, \quad (7-2)$$

when n is turns-ratio and the secondary coil is tuned by series capacitor C_s , which satisfies $1/(\omega C_s) = \omega L_{sec}$.

If we assume $R_{load} = 50$, $n = 3$, $Q_{pri} = 10$, $Q_{sec} = 10$ and $k = 0.7$, the inductance of the primary coil L_{pri} for the maximum efficiency is 5 nH. However, the equation (7-2) neglects parasitic capacitors in the transformer and an EM simulation is necessary for a better modeling. In order to decide the transformer layout, a transformer simulator ASITIC [74] [75] was used. Then, Agilent's Momentum electromagnetic simulation was carried out to fine-tune the transformer.

There are a few important considerations in designing on-chip transformers. On-chip transformers have low coupling between primary and secondary coils and, therefore, load resistance transform-ratio does not follow turns-ratio quadratically [47]. The input impedance can be derived from a transformer model with low coupling (Appendix B). Secondly, although high Q and k are needed for high transformer efficiency in equation (2.7), they must be compromised. The centers of the primary and the secondary layers must be close for the tight coupling but narrow metal layer results in high resistive loss. Besides the loss consideration, the

metal layer has to be wide enough to handle high current to prevent electromigration. Lastly, parasitic capacitance lowers self-resonant frequency and degrades the transformer.

Based on the EM simulations, 1:3 turns-ratio is selected to provide the 16 Ohms load at the primary with improved coupling. The primary coil is 75um-wide and the secondary is 50um-wide for the efficiency and current handling. The outer dimension of the transformer is $2910 \times 1365 \text{ um}^2$. In the ADS simulation, the transformer (L5, L6, L7 and L8) in Figure 7-1 has $L_{pri} = 5 \text{ nH}$, $L_{sec} = 36 \text{ nH}$, $Q_{pri} = 10$ and $Q_{sec} = 13$ when the primary coil has one turn and three turns in the secondary. Coupling coefficient k is 0.75.

The transformer's S-parameter model was simulated with the series capacitor, $C_s = 6.6 \text{ pF}$, and 50 Ohms load as shown in Figure 7-3. C_p of 8 pF is added in the primary side to obtain class-E/ F_{odd} output tuning. The transformed impedance at the primary, Z_{in} , is $16 // j31 \text{ Ohms}$ and the efficiency of the transformer is 67 % when it is conjugate-matched. The resistive load value is accurate for 1-Watt output but the efficiency is lower than the calculated value of 79 % based on (2.7). The equation (2.7) overestimates the efficiency because it neglects parasitic capacitance between the metal layers and between the metal layer and ground plane.

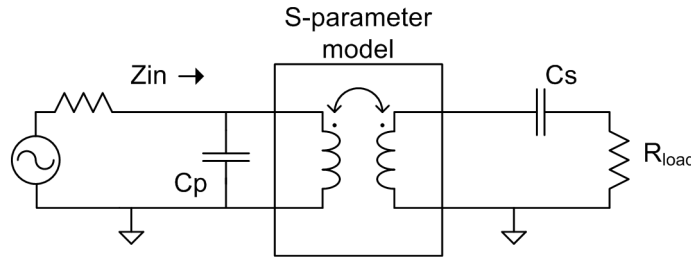


Figure 7-3: S-parameter simulation with the transformer model

4. TR Switch Function

It has been reported that a traditional GaAs TR switch can be replaced by an integrated resonant TR switch [60]. The paper showed that the resonant TR switch can protect an LNA in 3 V process from up to 5 W PA output. It is illustrated in [59] that the resonant TR switch concept also can be integrated into the PA also, and a fully integrated transceiver RF front-end is implemented. With proper design the LNA's input resistance is raised to $1\text{K}\Omega$ during transmit operation and absorbs only 0.2dB of the PA's output power, yielding excellent overall efficiency.

The paper also showed that high resistance output from PA limits degradation of receiver noise figure (NF) to a negligible value at receive mode.

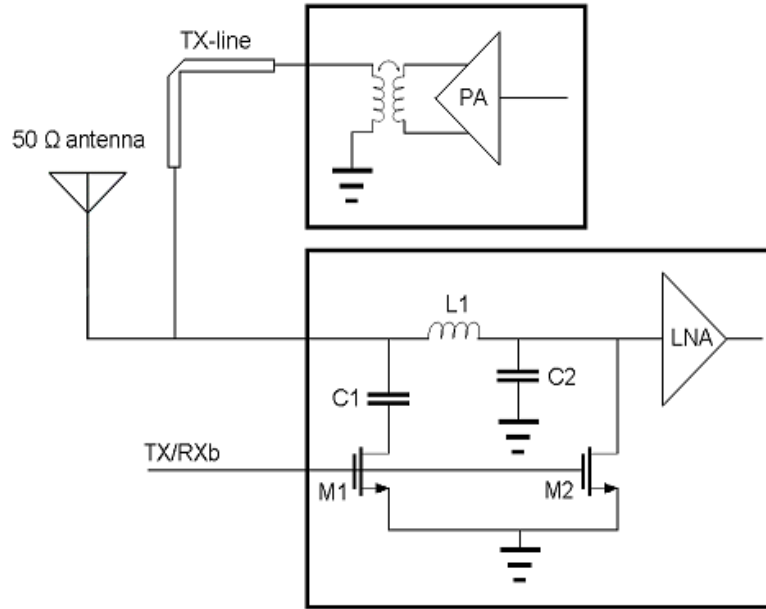


Figure 7-4: The resonant TR switch at the LNA and the PA output transformation by transmission line.

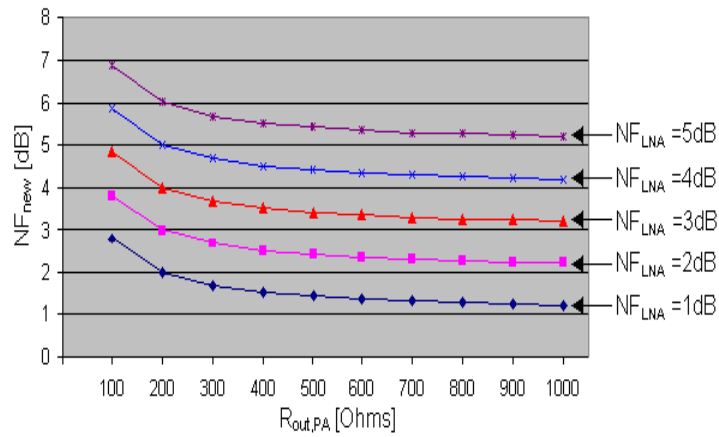


Figure 7-5: NF degradation due to the PA output resistance. NF_{new} is the degraded NF from NF_{LNA} .

In the 1-Watt PA design described in this thesis, the technique is employed to implement a full TR function as shown in Figure 7-4. In transmit mode, TX/RXb control shorts the LNA input to ground and L1-C1 parallel tank presents high impedance toward antenna. Assuming 50 Ω antenna and $Z_{in,LNA} \gg R_{ant}$, most power from the PA is radiated through antenna with little loss. The loss by the switch can be derived as

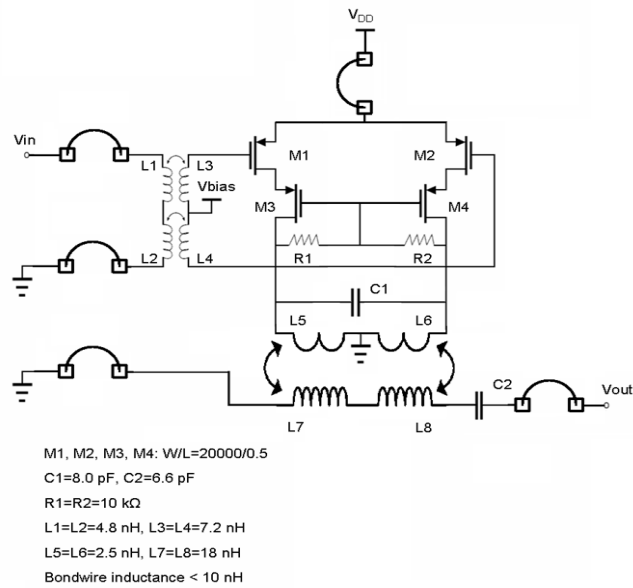
$$\frac{P_{loss}}{P_{out}} = \frac{V_{ant}^2 / R_{in,LNA}}{V_{ant}^2 / (R_{in,LNA} \parallel R_{ant})} \quad (7.3)$$

When the LNA is matched to R_{ant} , the P_{loss}/P_{out} can be held less than 5 % (0.2 dB loss).

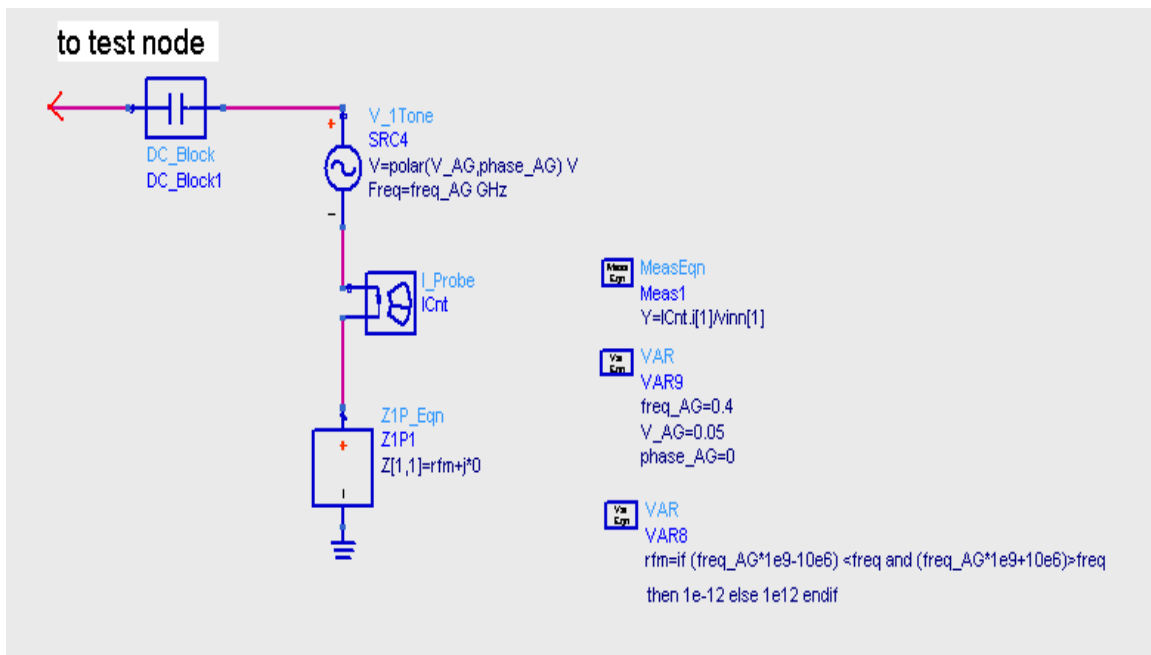
At receive mode all the transistors in the PA are shut down and output impedance at the PA chip is inductive due to the secondary output coil. If the LNA sees very high impedance toward the PA output, signal to noise ratio at the input is affected minimally. Although the PA output is not resonant at the 435 MHz receive frequency, a short transmission-line can be added to bring the impedance to a high value. Thus, NF of the LNA (NF_{LNA}) is not degraded significantly. For instance, when an LNA with 3 dB NF is combined with a PA, which presents 400 Ω resistance toward the LNA, the resultant NF (NF_{NEW}) is 3.5 dB as shown in Figure 7-5. The NF_{NEW} calculation is detailed in Appendix C.

5. Stability Analysis

Auxiliary Generator Method



(a)



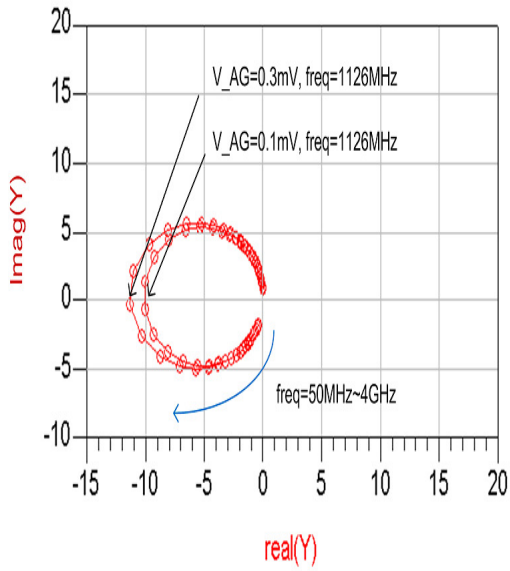
(b)

Figure 7-6: (a) Schematics of the PA and (b) the auxiliary generator method in Agilent ADS.

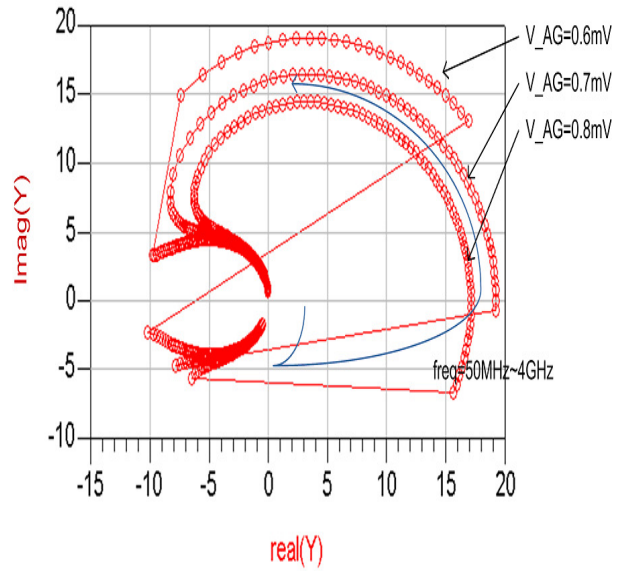
The PA is a highly nonlinear circuit and its stability cannot be determined by k-factors based on small signal S-parameters. Therefore, as introduced in Chapter 4, the auxiliary generator (AG) method is used in Agilent ADS simulation. Supposing admittance of a circuit node is Y_T , oscillation starts up when $Re(Y_T) < 0$ and $Im(Y_T) = 0$. The schematics of the PA (Figure 7-1) are redrawn in Figure 7-6a for convenience. The AG with a frequency selective impedance Z1P1 is attached to the test node of interest as shown in Figure 7-6b. The AG test was carried out at the gate of the common-source transistor (either M1 or M2 in Figure 7-6a). Stability with VDC variation was also tested (Figure 7.8). In both tests, no input signal is provided to observe existence of self-oscillation.

In the first AG simulation at the gates, as shown in Figure 7-7a, frequency and amplitude of the AG (V_{AG}) are varied. Y_T trace crosses $Im(Y_T) = 0$ line, while $Re(Y_T) < 0$, meeting the oscillation start-up condition when $V_{AG} = 0.1\text{mV}$, and then the oscillation amplitude, V_{AG} , grows to 0.3mV at 1126 MHz . However, when the amplitude reaches 0.6mV as shown in Figure 7-7b, $Re(Y_T)$ jumps to positive region without crossing the $Im(Y_T) = 0$ line. Therefore, the node voltage attenuates at 1126 MHz by the positive Y_T . Consequently, the node voltage cannot grow higher than 0.6mV .

Figure 7-8 shows Y_T traces with $V_{AG} = 0.5\text{mV}$ when VDD decreases. The oscillation observed in the former test disappears when VDD is decreased to 2.7 V . As the amplitude grows into 5mV , 10mV and 20mV , no oscillation occurs regardless of VDD as the loci in Figure 7-8b, 7-8c and 7-8d confirm – the size of the loci is reduced as the amplitude of the AG increases but the loci maintain $Re(Y_T) > 0$ when it crosses $Im(Y_T) = 0$.

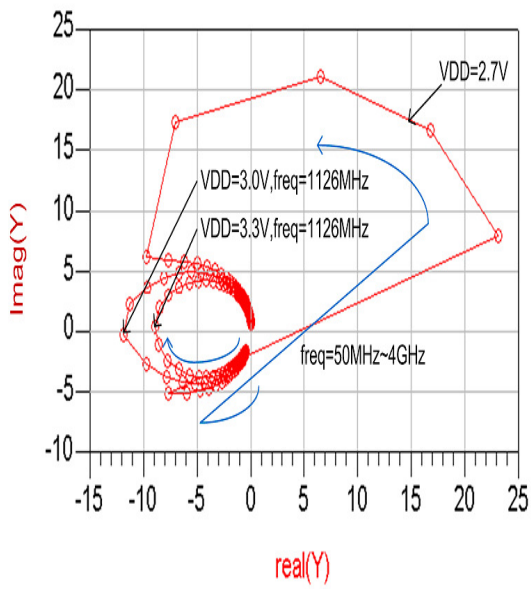


(a)

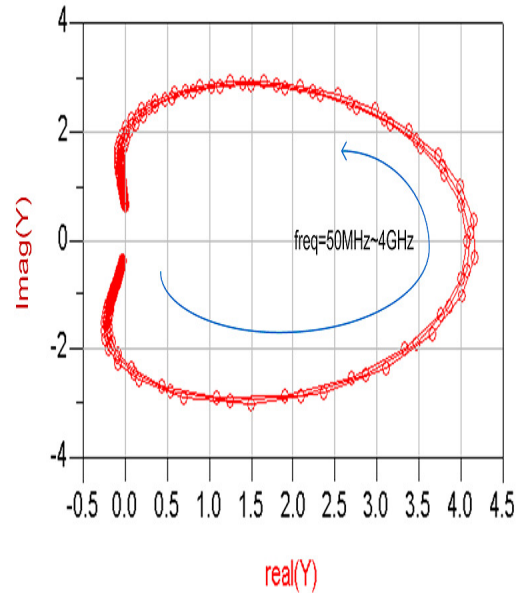


(b)

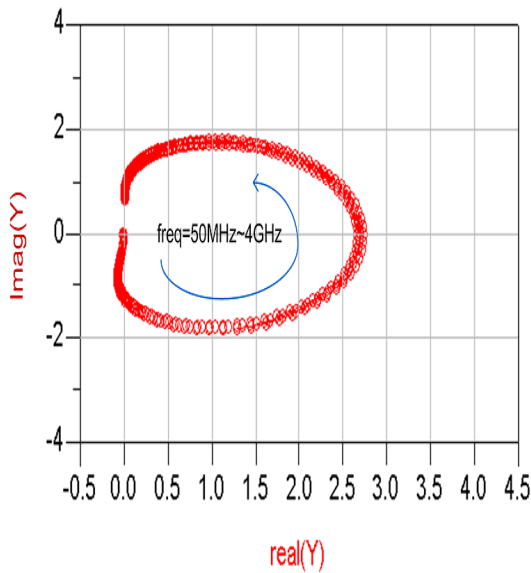
Figure 7-7: Admittance diagram at CS gate, freq=50MHz~4GHz, VDD=3.3V, (a) $V_{AG}=0.1\text{mV}$ and 0.3mV , (b) $V_{AG}=0.6\text{mV}$, 0.7mV and 0.8mV



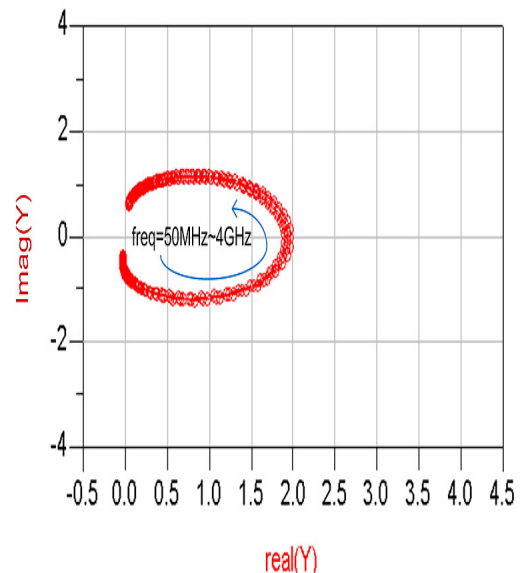
(a)



(b)



(c)



(d)

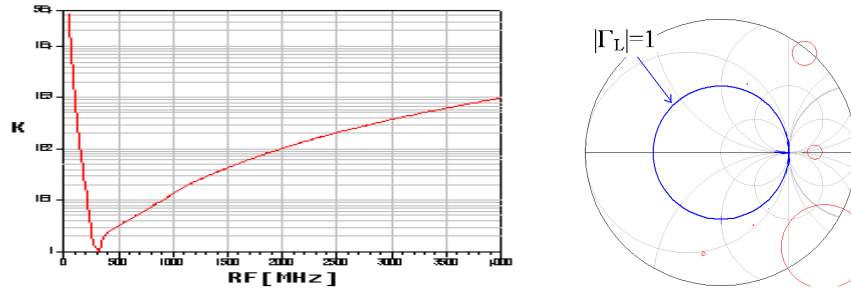
Figure 7-8: Admittance diagram at CS gate, freq=50MHz~4GHz, and VDD=2.7V, 3.0V, and 3.3V (a) V_{AG}=0.5m, (b) 5mV, (c) 10mV and (d) 20mV.

Large-Signal S-parameter method

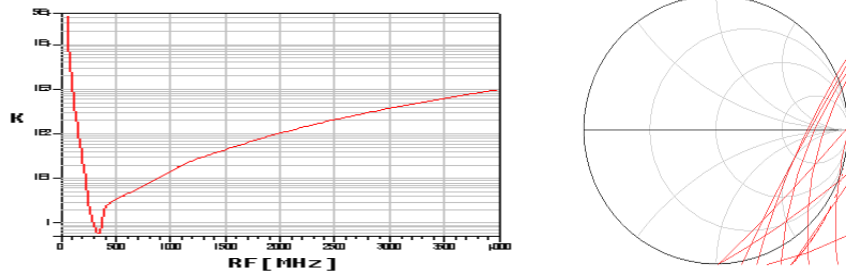
In addition to the AG test, large signal S-parameter simulation is also carried out. While the AG test enlightens the PA's state transitions, k-factor calculation using the large-signal S-parameter verifies whether the PA is unconditionally stable or not.

It is shown by the k-factor and load stability circle in Figure 7-9d that the PA is stable with nominal operating conditions – VDC=3.3V, P_{in}=20dBm and R_L=50Ω – since the unstable region is inside of the load stability circles. However, the PA is only conditionally stable from 300 MHz to 380 MHz when P_{in} is equal to or greater than 10dBm where K < 1 and unstable load condition exists within |Γ_L| = 1 circle (Figure 7-9b, c, and d). Only at P_{in} = 5dBm the PA is unconditionally stable (Figure 7-9a). As the P_{in} increases from 10 dBm to 20 dBm, unstable region of the load impedance retreats from the |Γ_L| = 1 circle in the Smith chart, and the oscillation becomes less likely with load mismatch.

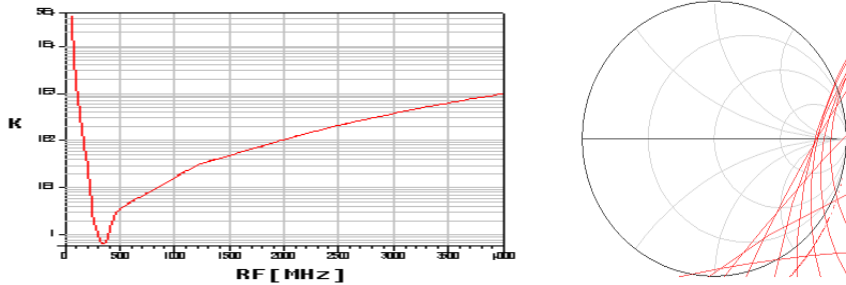
In PA measurement no oscillation was observed when P_{in} was varied with the load open-terminated in contrary to the simulations. It appears that the measured transformer Q is lower than simulated data, and that it stabilized the PA. In addition to the open-termination, various load mismatch such as VSWR of 3, 4.5, 8 and short termination is applied in tandem for the reliability tests in Chapter 8 and the PA did not enter oscillation in any cases.



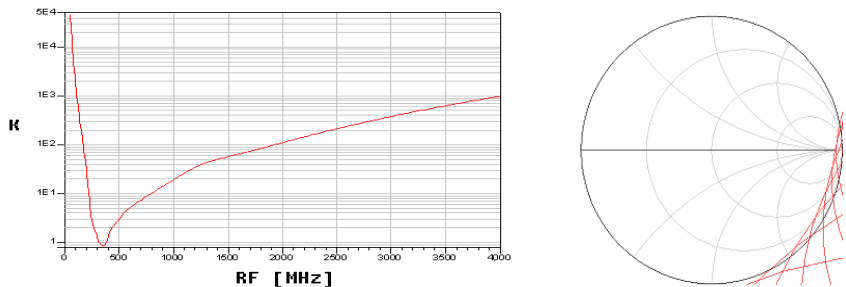
(a)



(b)



(c)



(d)

Figure 7-9: k-factor and load stability circle. Outside of the circle is a stable region. (a) $P_{in}=5\text{dBm}$, unconditionally stable. The load stability circle is out of the $|\Gamma_L|=1$ circle (b) $P_{in}=10\text{dBm}$, conditionally unstable from 300MHz to 370MHz, (c) $P_{in}=15\text{dBm}$, conditionally unstable from 300MHz to 380MHz, and (d) $P_{in}=20\text{dBm}$, conditionally unstable from 320MHz to 380MHz.

6. Thermal Analysis of the 1-Watt PA

Despite many advantages of the SOS process, the thermal conductivity of the sapphire substrate is poor compared to Si, and similar to GaAs [76]. As channel temperature is tightly related to circuit failure by the Arrhenius equation (3.4), thermal analysis of the 1-Watt PA is carried out in this section.

Power Cell Layout

The FET layout is important since junction channels are the hottest spot in the PA and the transistors must be protected from excessive heat localization. A power cell in the 1-Watt PA has 50×16 fingers and each finger's size is $25 \text{ um} / 0.5 \text{ um}$, resulting in total $W/L = 20000 \text{ um} / 0.5 \text{ um}$. Figure 7-10 shows a microphoto of the one side of the differential pair. Two PMOS power cells are stacked and each power cell has 16 large fingers. As shown in the zoom-in figure, each large finger has fifty 25um -long interdigital fingers.

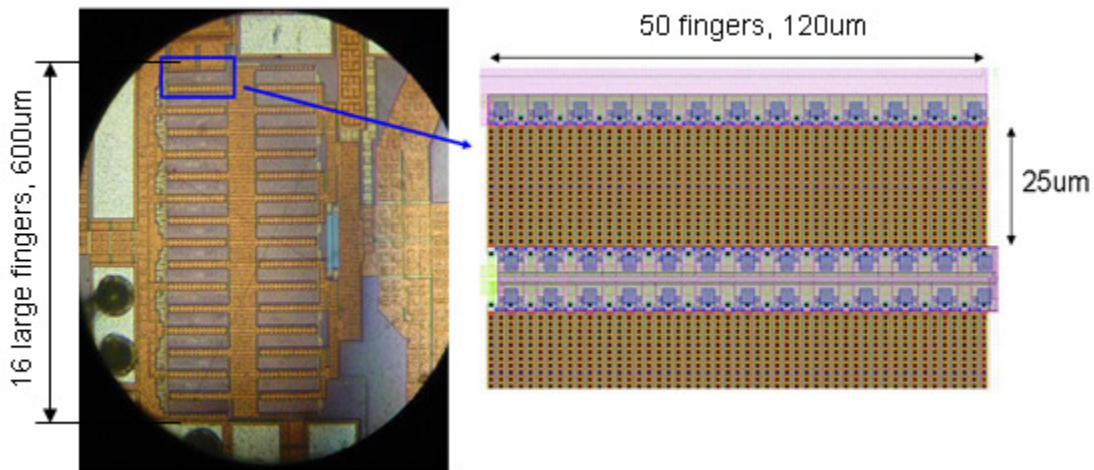


Figure 7-10: Microphoto of the power cell and a zoom-in layout of one of the 16 large fingers

Thermal Simulation of the Power Transistor

The channel temperature of a power transistor can be approximated by the methods mentioned in Chapter 3 such as microstrip-FET analogy and Higashisaka's 45-degree downward conduction assumption, but it is also pointed out that the methods are valid only when average channel temperature among gate-fingers are concerned. Therefore, three-dimensional partial

differential equations must be solved for the complicated power FET used in the 1-Watt PA. A commercial software, ANSYS® TAS™ (Thermal Analysis System) [77], solves the thermal problem by dividing the thermal structure into small resistor/capacitor representations and by equating boundary conditions among them in difference equations.

For the TAS thermal simulation, the power cells of Figure 7-10 were drawn as shown in Figure 7-11. Since it is measured that $P_{in} = 100\text{mW}$, $P_{out} = 850\text{mW}$, $\text{PAE} = 30\%$ and transformer efficiency $\eta_T = 70\%$, approximately 1.3 W and 0.35 W are dissipated in the junction channels and the output transformer, respectively. Therefore, total 1.3 W heat load is applied to the four 50×16 fingers. The heat loads are displayed in red in Figure 7-11b. The heat load's size ($25\text{ um} \times 1.1\text{ um}$) is different from the gate-finger size ($25\text{ um} \times 0.5\text{ um}$) because the channel length is the distance between drain and source regions. The sapphire substrate is surrounded by air except a bottom plate ($z = 0\text{ um}$). The boundary temperature on the bottom plate is fixed at $25\text{ }^\circ\text{C}$. No forced convection is provided in the simulation.

The TAS simulation shows that peak temperature in the channels is $38\text{ }^\circ\text{C}$ with the boundary conditions. Therefore, the thermal resistance from junction channels to the backside of the sapphire substrate (θ_{jb}) is $(38-25)/1.3 = 10\text{ }^\circ\text{C/W}$. As indicated in Figure 7-11c and 7-11d, heat is more concentrated at the center of top and bottom transistor pairs. It is also found that the heat does not spread out horizontally to the entire chip. Instead, it is confined within approximately the chip's height, making 45-degree heat descent a reasonable assumption.

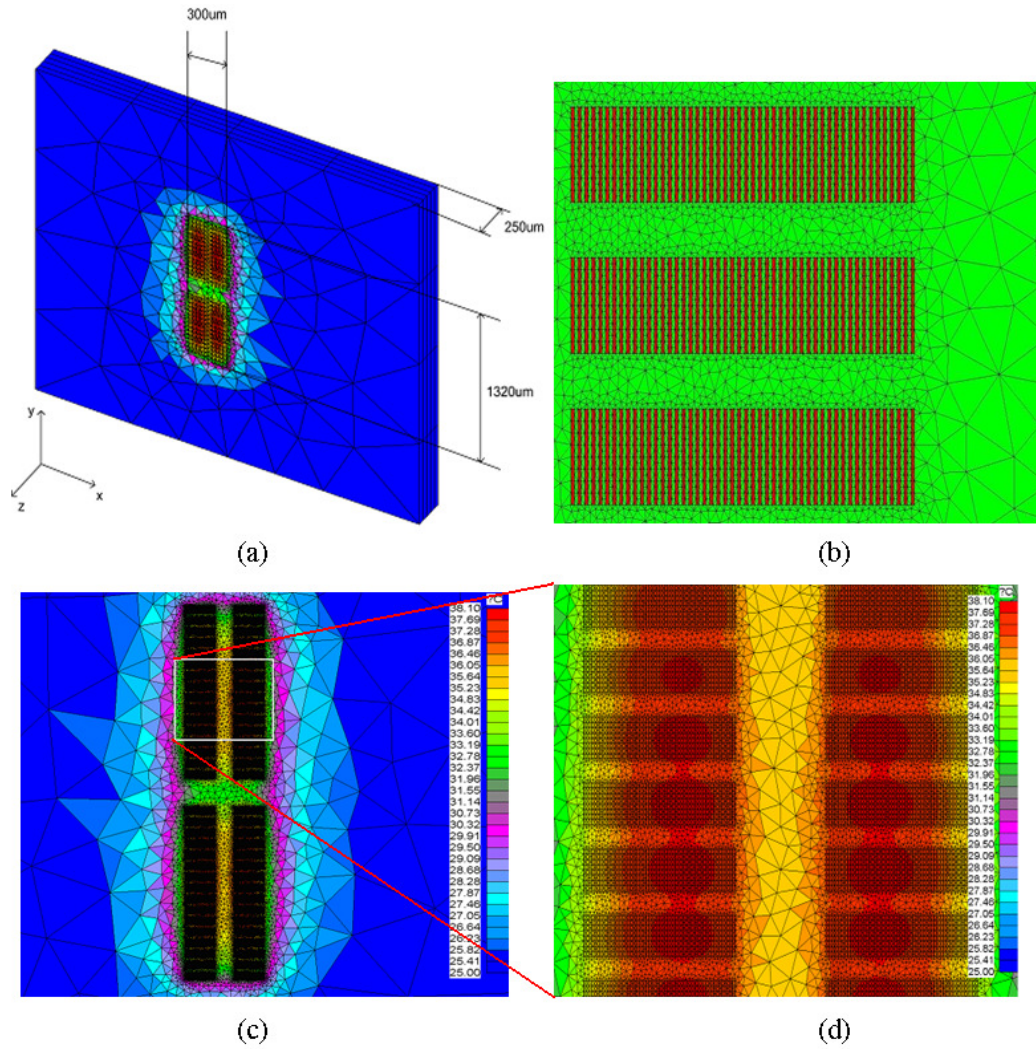


Figure 7-11: Thermal simulation of the power cells on SOS. (a) 3D plot (b) heat load in the junction channels (c) closeup of the transistor cells on the x - y plane (d) closeup at the temperature peak.

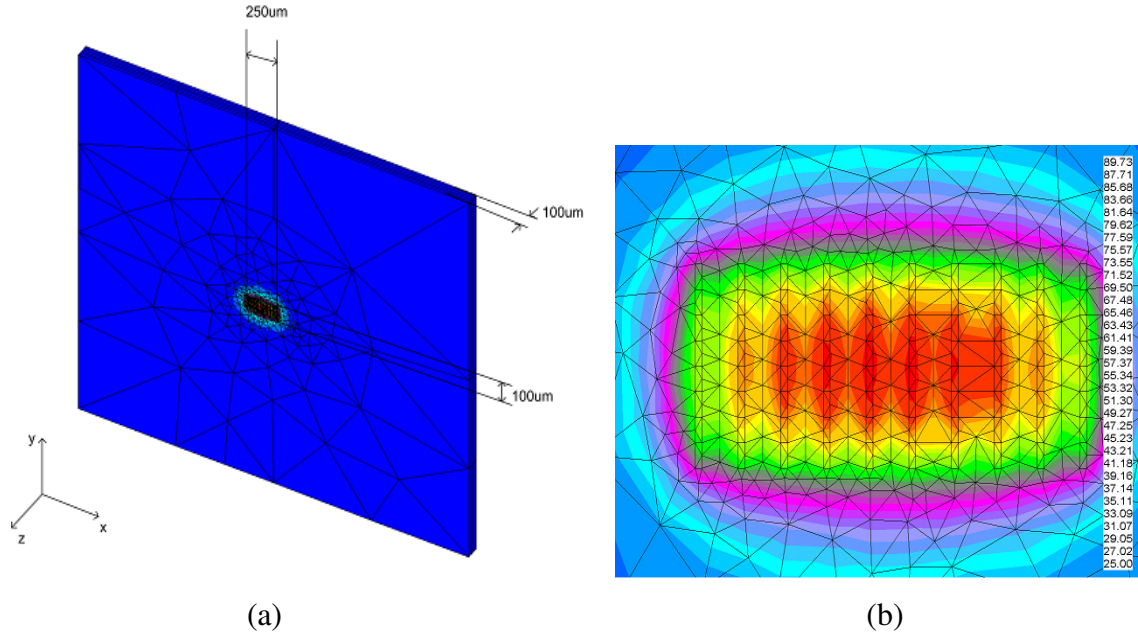


Figure 7-12: Thermal simulation of the power cell on GaAs. (a) 3D plot (b) closeup of the transistor cells

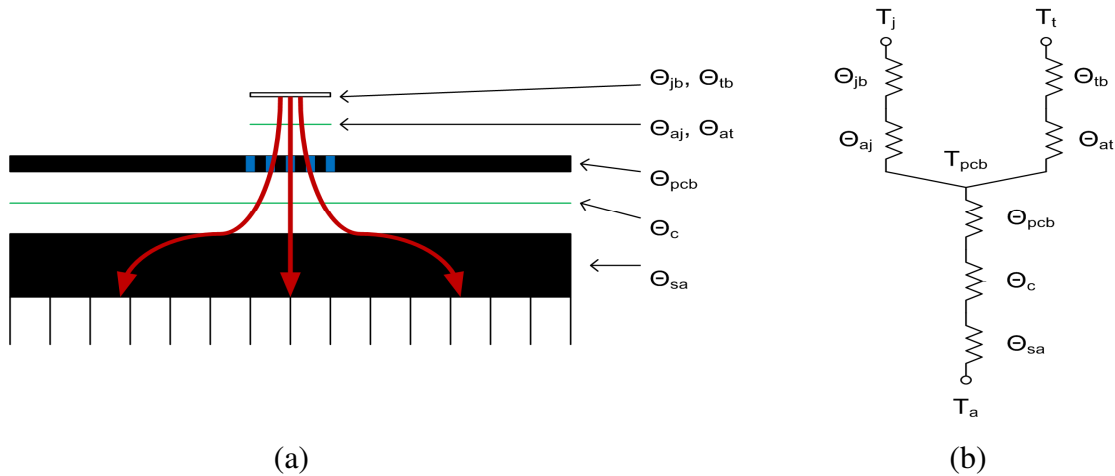
	SOS	GaAs
Area [μm^2]	1320×300	100×250
Thickness [μm]	250	100
K [$\text{W}/\text{m}\cdot\text{K}$]	40	59
Power dissipation [W]	1.3	1.3
ΔT_{max} [K]	13	65

Table 7-1: Thermal dissipation in SOS and in GaAs process

In comparison, a typical GaAs power cell is simulated too. The GaAs power cell is composed of ten fingers of 100um-wide channel on 100um-thick GaAs substrate and source-drain spacing is 4um. Culbertson and Lehmann's program predicted the maximum temperature of the channel $\Delta T_{\text{max}} = 67^\circ\text{C}$ with 1-Watt power load [78]. Similarly, as shown in Figure 7-12, the TAS simulation resulted in $\Delta T_{\text{max}} = 65^\circ\text{C}$ with 1.3 W heat load. The thermal property comparison between the SOS and the GaAs power cells is summarized in Table 7-1. High gain and high V_{bk} of the GaAs process enables a much smaller power cell than in the SOS. However, the ΔT_{max} of the GaAs is five times higher due to the smaller area. Hence, it is concluded that

although the sapphire substrate has lower thermal conductivity, it actually outperforms the GaAs thermally unless the GaAs cell is spread out.

Junction Temperature Calculation



- θ_{jb} : thermal resistance from the junction channels to the backside of the die
- θ_{tb} : thermal resistance from the transformer to the backside of the die
- θ_{aj} : thermal resistance by thermal adhesive from the backside of the die to the PCB under the junction channels
- θ_{at} : thermal resistance by thermal adhesive from the backside of the die to the PCB under the transformer
- θ_{pcb} : thermal resistance of the PCB
- θ_c : thermal resistance by thermal compound from the PCB to the heatsink
- θ_{sa} : thermal resistance from the heatsink to air

Figure 7-13: (a) A simplified thermal model and (b) an equivalent thermal circuit

Since θ_{jb} is predicted by the simulation, the junction temperature (T_j) can be calculated if the temperature on the backside of the die is known. Although thermal resistance from the output transformer to the backside of the die (θ_{tb}) is not simulated together, it is simplified that the chip and the thermal adhesive are substantially thin that heat by the transistors and the transformer arrive at the PCB surface without affecting each other significantly. The thermal equivalent circuit with the separate heat paths to the PCB is shown in Figure 7-13b. Thermal resistance of the PCB (31mil FR4, θ_{pcb}), thermal compound (Wakefield part No. 120-8, θ_c), and the heatsink (Wakefield part No. 528-45AB, θ_{sa}) are 1.4 °C/W, 0.95 °C/W and 8.6 °C/W, respectively. θ_{pcb} is estimated from an equation in reference [79],

$$\frac{1}{\theta_{pcb}} = \frac{1}{\theta_{via}} + \frac{1}{\theta_{sub}} \approx \frac{1}{\theta_{via}}, \quad (7.4)$$

$$\theta_{via} = \frac{t_{pcb}}{\lambda_{cu} \pi (R_{out}^2 - R_{in}^2)} \approx 39^\circ C/W, \quad (7.5)$$

where $t_{pcb} = 31$ mil, PCB thickness,

$\lambda_{cu} = 384$ W/mK, thermal conductivity of top and bottom layer,

$R_{out} = 10$ mil and $R_{in} = 8.6$ mil, radii of via's outer and inner surface using 1-oz. copper.

$$\theta_{pcb} = \frac{\theta_{via}}{28} = 1.4^\circ C/W. \quad (7.6)$$

Since conductivity of via is much higher than that of FR4 substrate, the equation (7.4) is simplified. For heat dissipation, abundant thermal vias are built under the PA die as shown in Figure 7-14. The equation (7.6) is valid when spreading resistance between the 28 vias on the top layer is negligible.

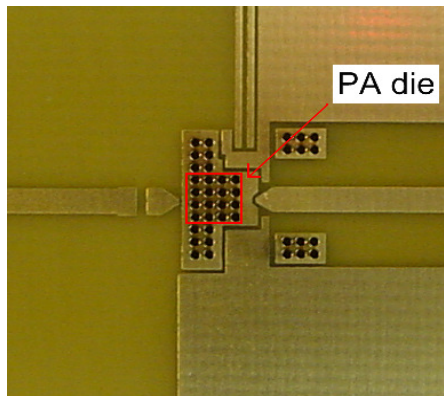


Figure 7-14: Vias in the PCB for heat dissipation

Thermal resistance of the compound at the interface of the PCB and the heatsink θ_c under the vias is

$$\theta_c = \frac{t_c}{\lambda_c A_c} = \frac{0.025 \text{ mm}}{\frac{0.735 \text{ W}}{\text{mK}} (6 \text{ mm})^2} = 0.95^\circ C/W. \quad (7.7)$$

Thus, temperature on the top layer of PCB (T_{pcb}) assuming 25 °C ambient is

$$T_{pcb} = (P_j + P_t)(\theta_{pcb} + \theta_c + \theta_{sa}) + T_a \approx 19 + 25 = 44^\circ C . \quad (7.8)$$

In order to find the thermal resistance θ_{aj} through the conductive epoxy used for bonding the chip to the board, it is assumed that the heat from the channels is spread downward with a 45-degree umbrella. Hence, the effective area of the thermal adhesive has longer sides in both x and y direction by twice the thickness than the power cell's area.

$$\theta_{aj} = \frac{t_{aj}}{\lambda_{aj} A_{aj}} = \frac{0.025mm}{\frac{3.2W}{mK} (300 + 2 \times 250)(1320 + 2 \times 250)um^2} = 5.4^\circ C/W . \quad (7.9)$$

Since ΔT of the chip is known by simulation, the junction temperature T_j in operation can be estimated

$$T_j = \Delta T + P_j \theta_{aj} + T_{pcb} = 13 + 7.0 + 44 \approx 64^\circ C . \quad (7.10)$$

If there is no heatsink, the heat must be dissipated by convection in the air. The thermal resistance of the air convection (θ_{conv}) is

$$\theta_{conv} = \frac{1}{h_{air} A_{pcb}} = 17^\circ C/W , \quad (7.11)$$

where $h_{air} = 15 \text{ W/m}^2\text{K}$: heat transfer coefficient without forced convection,

$A_{pcb} = 6 \text{ cm} \times 6.5 \text{ cm}$: surface area of the PCB, assuming the heat is evenly spread on the backside of the PCB.

Substituting θ_{conv} in θ_{sa} results in $T_j = 78^\circ C$. Considering the maximum junction temperature for Si device is 200 °C [80], the PA is safe from the heat even without a heatsink.

Chapter 8 - Implementation and Measurements

1. Implementation

The PA is fabricated in 0.5 μm Peregrine SOS and the die size is $3.2 \times 3.2 \text{ mm}^2$. A 52-pin standard package and FR4 PCB are used to build a test board. The die microphoto and the test board photo are shown in Figure 8-1 and Figure 8-2, respectively. All the metal layers carrying large rms current observe electro-migration rules. The PA has strong immunity to bondwire parasitics as previously explained, allowing it to be placed in the package instead of chip-on-board. Hence, gold-plated PCB for a chip-on-board was not necessary for this work. Fourteen bondwires to power supply and ten bondwires to ground are connected around the package and are spaced in order to decrease source resistance and mutual inductance. A 4.7pF surface-mount capacitor is added in series at the output to adjust output tuning, but this can be easily moved into the chip in the next version.

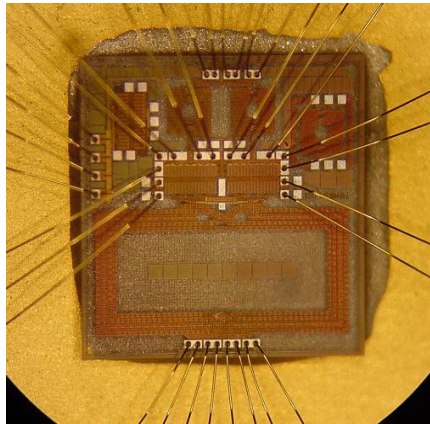


Figure 8-1: Die microphoto of the PA with bondwires.

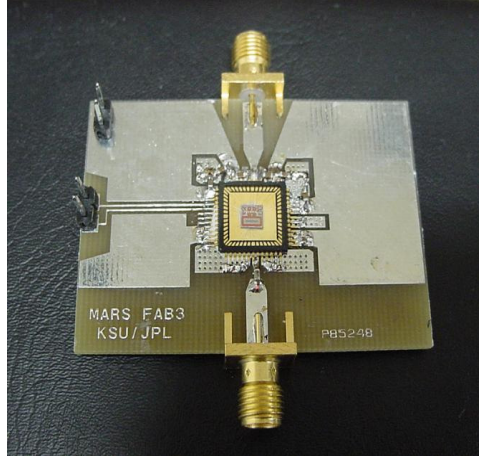


Figure 8-2: Photo of the test board. Bypass capacitors near the package and one tuning capacitor at the output are used.

2. Output Transformer Measurements

As shown in Figures 8-3 and 8-4, a test structure was fabricated and measured. When an extra length (≈ 800 μm) layer for probing was compensated, measured inductance ($L_{\text{pri}} = 4.8$ nH, $L_{\text{sec}} = 36$ nH) had less than 5 % difference from the simulation. However, measured Q was much lower and $Q_{\text{pri}} = 7.3$ and $Q_{\text{sec}} = 8.5$, which are only 73 % and 65 % of the simulation data respectively. The coupling coefficient, $k = 0.68$, is estimated using the equation [81]

$$k = \sqrt{\frac{\text{Im}(Z_{12}) \cdot \text{Im}(Z_{21})}{\text{Im}(Z_{11}) \cdot \text{Im}(Z_{22})}} \quad (6.1)$$

Substituting the measured data into (2.7), the transformer efficiency is 69 % which is lower than the simulation result by 10 %.

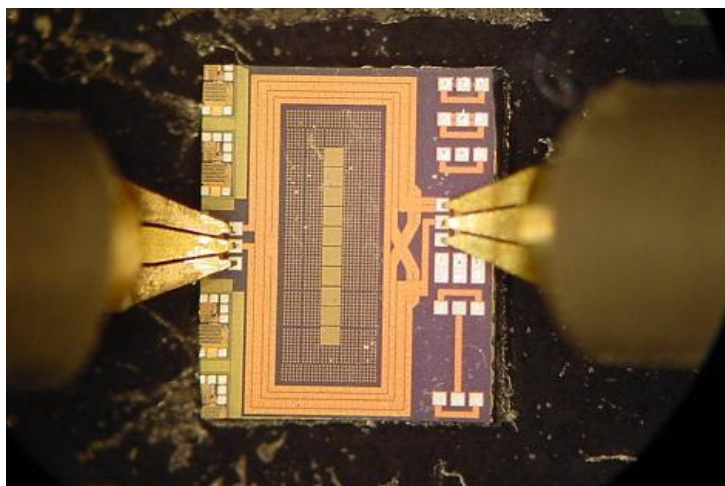
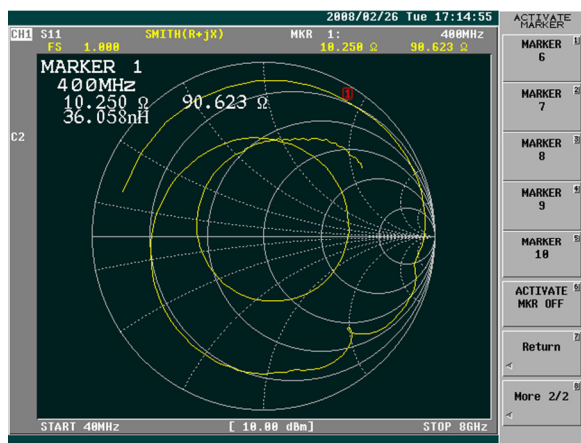
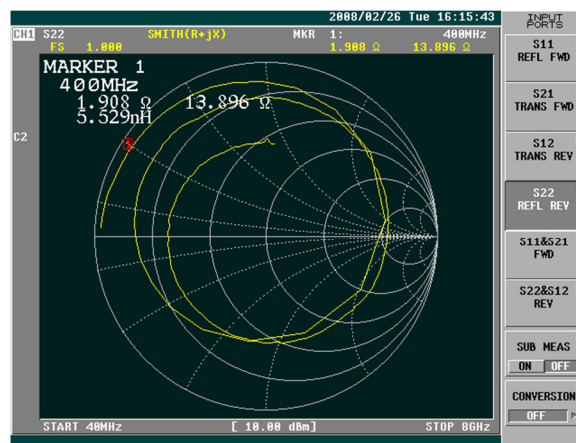


Figure 8-3: Photo of output transformer test



(a)



(b)

Figure 8-4: Output transformer (a) S_{11} and (b) S_{22} plot with the other port open

3. Measurements of the PA

Figure 8-5 shows the PA's output power and PAE with input power variation. When the PA is driven by the 20 dBm output transceiver, 29 dBm P_{out} and 29 % PAE was measured at 3.3 V DC. 30 dBm output is achieved with 24 dBm input with 27 % PAE. The output power was also measured over power supply variation. As shown in Figure. 8-6, the output power monotonically increases up to 31 dBm at $V_{DD} = 4.5$ V.

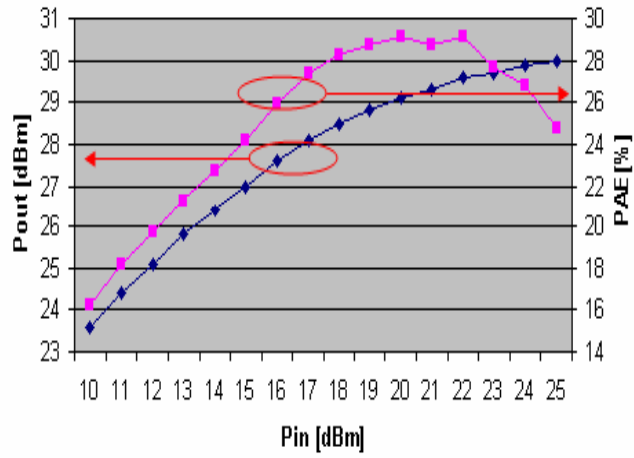


Figure 8-5: P_{out} and PAE with P_{in} variation.

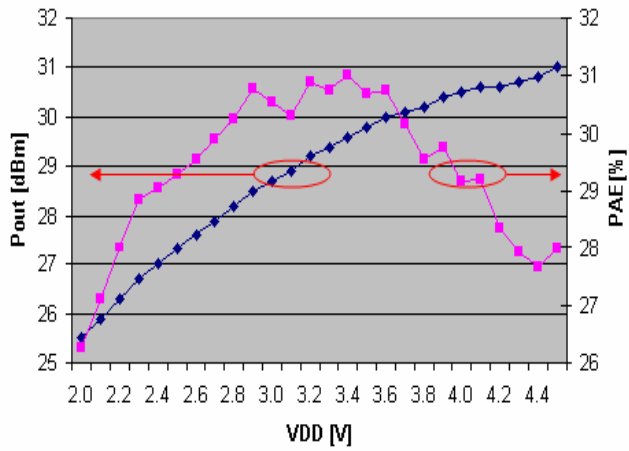
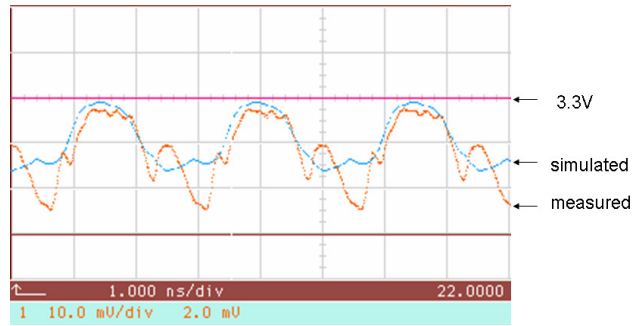
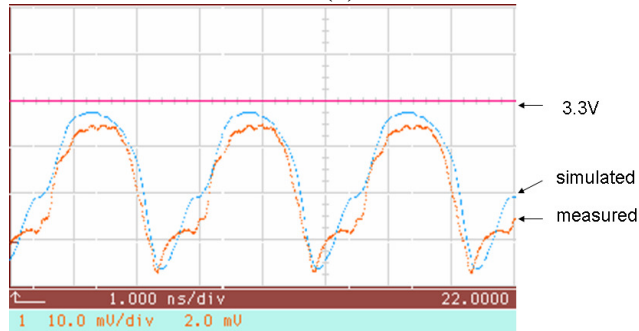


Figure 8-6: P_{out} and PAE with fixed 20 dBm P_{in} and power supply variation.

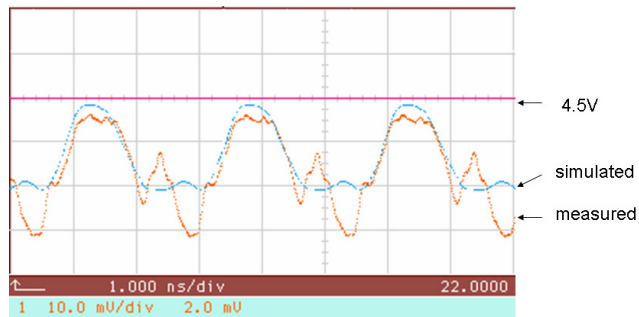


(a)

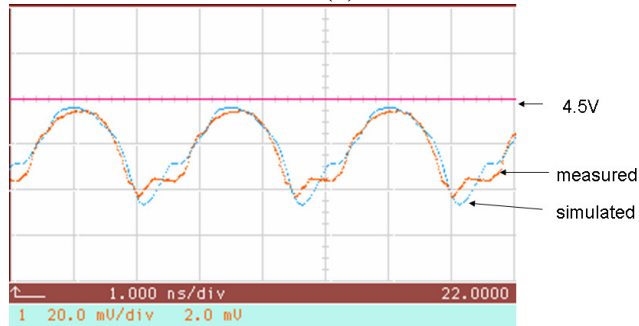


(b)

Figure 8-7: Drain voltage waveforms of (a) common source pair and (b) common gate pair with 3.3 V power supply. After a 1:100 probe and a 6 dB power splitter, the plot shows 1/200 of the actual signal amplitude.



(a)



(b)

Figure 8-8: Drain voltage waveforms of (a) common source pair and (b) common gate pair with 4.5 V power supply. The plot shows 1/200 of the actual signal amplitude.

While increasing the power supply voltage, time-domain waveforms at the drains of the stacked PMOS pairs are probed in order to observe V_{sd} stress. A 1:100 needle probe was used and the probed signal was passed through a 6 dB resistive power splitter to trigger a 20 GHz oscilloscope (HP 83480A). Figure 8-7 shows that V_{sd} is 5 V for the common-source pair and V_{peak} at the primary coil is about 7.5 V at $V_{DD} = 3.3$ V. Waveforms at $V_{DD} = 4.5$ V are also shown in Figure 8-8. While the self-biased stacked PMOS pairs generate 31 dBm output, the maximum V_{sd} stress is 6 V with 4.5 V power supply. No performance setback was observed in continuous time transmission test.

Frequency response is shown in Figure 8-9. At the fixed 20 dBm input power, the PA has very wide bandwidth, approximately 200 MHz, due to low resonance circuit Q at the output network.

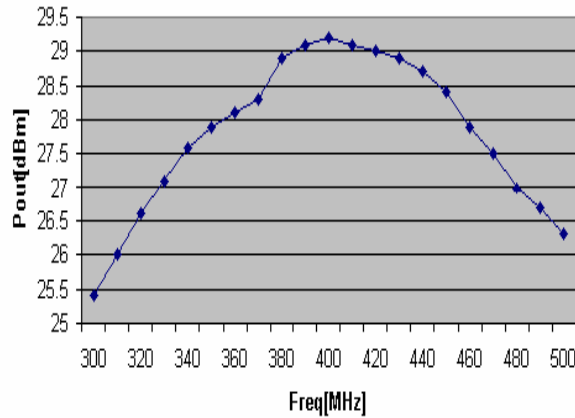


Figure 8-9: Frequency response with fixed 20 dBm P_{in} .

4. Measurements of the TR Switch Function

The output impedance was approximately 360 Ω (Figure 8-10) when transmission line delay is added into vector network analyzer (HP 8753E) calibration. From equation (C.9) this is equivalent to 0.6 dB degradation in NF. Finally, off-state noise contribution of the PA is also measured. The PA's output is amplified by 40 dB LNA (HP 8447A) before it is connected to a spectrum analyzer (Agilent E4402B). As shown in Figure 8-11, no noise floor rising is observed when the power supply is turned on while the PA is at receive mode. A spectrum with a 15 dB ENR source input is also displayed to validate that the test setup is sufficiently sensitive to detect any noise increase that would affect the 3 dB system NF of the microtransceiver.

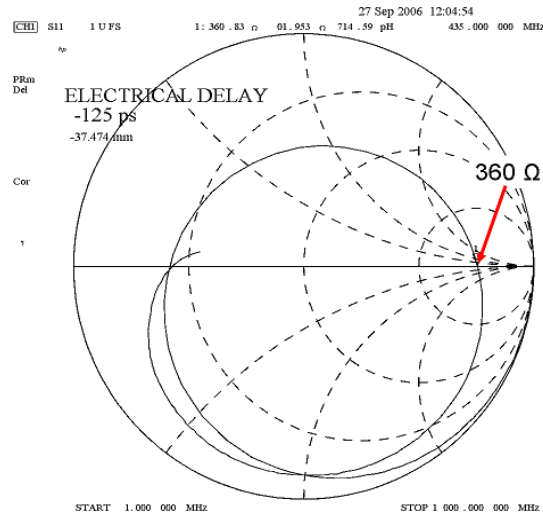


Figure 8-10: The output impedance measured at receive mode with -125 ps delay

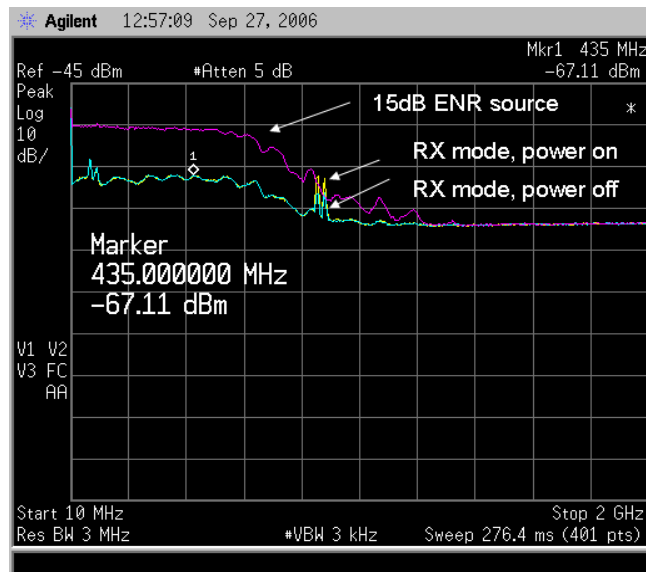


Figure 8-11: The output noise measured with a 40 dB gain LNA before the spectrum analyzer.

5. Pulsed Operation

The PA's performance was measured with pulsed RF input signal as shown in Figure 8-12a. Switching duty cycle was varied from 20 % to 80 % with and without a heatsink (Figure 8-13). At 80 % duty cycle 0.2 dB and 0.4 dB power decline was observed with and without the heatsink respectively. Although quantitative analysis was not pursued, it is suggested that

thermal time constant is greater without the heatsink, and consequently the remnant heat represses the output power more than with the heatsink.

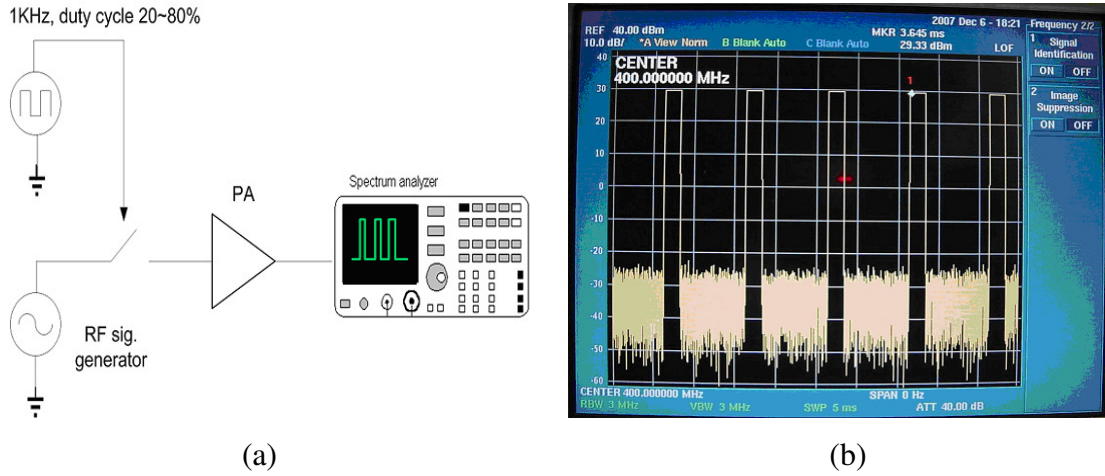


Figure 8-12: Pulsed operation (a) schematics (b) P_{out} in zero-span measurement.

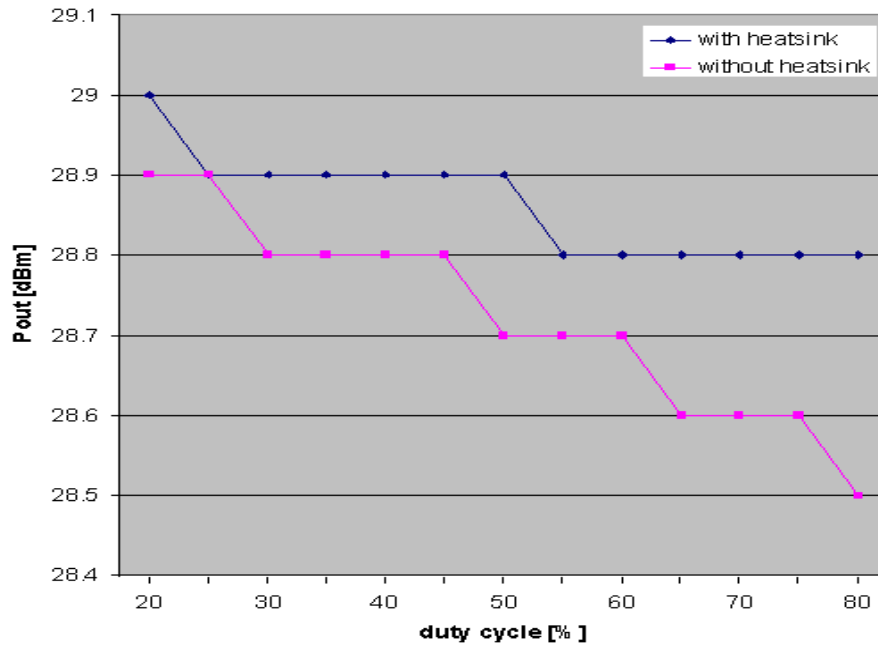


Figure 8-13: Output power variation in pulsed operation with and without heatsink

6. Low Temperature Test

Martian atmosphere is much colder than the Earth's. Average temperature on Mars is -63°C [82] and operational temperature of unheated spacecrafts range from -120°C to -20°C [83]. In order to emulate the environments, the PA was put in a cryogenic chamber as shown in Figure 8-14 and performance was tested. The cryogenic cooling operation procedure is found in [83]. A temperature sensor was attached on the lid of the PA package. In the measurement, as shown in Figure 8-15, both output power and PAE increase as temperature goes down when carrier mobility and the transformer Q enhances. At -100°C , the output power reached 30.5 dBm with 37% PAE.

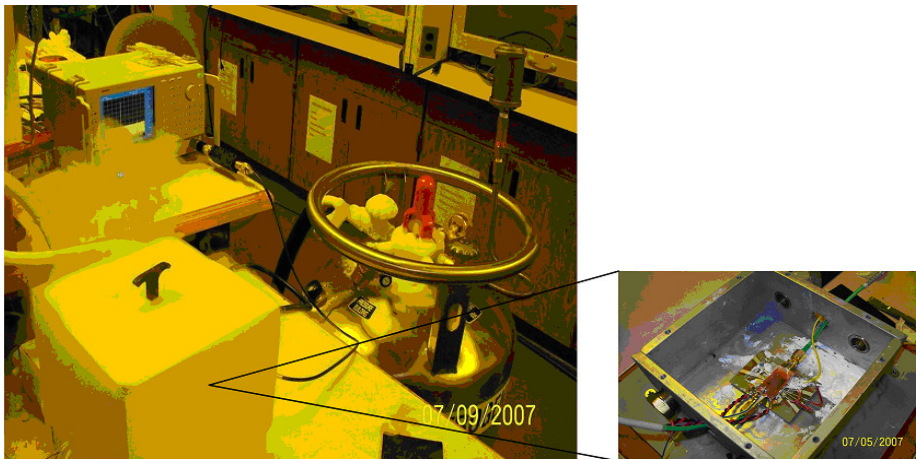


Figure 8-14: Low temperature test scene and the PA in cryogenic chamber.

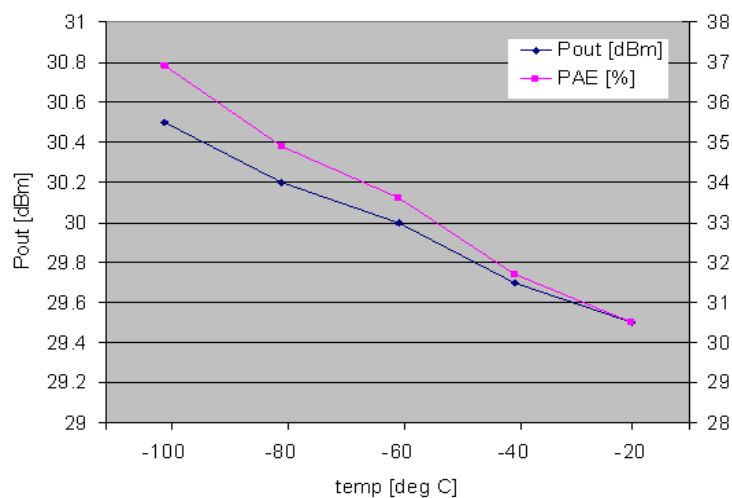


Figure 8-15: P_{out} and PAE measured in sub-zero temperature.

7. Reliability Test

Lastly, the 1-Watt PA was tested in continuous-wave mode with various power supply levels and output terminations. Two PAs, one in a package and the other directly wire-bonded to a PCB, are tested simultaneously. For each test, the PA was kept on for approximately 3.5 days and the entire test took about a month. The test setup schematics and photo are shown in Figure 8-16. The signal generator's output (16 dBm) is split by the power divider and 13 dBm RF input drives commercial amplifier-module (Mini-circuit 258A). Each 258A driver-amplifier provides 19.5 dBm to the 1-Watt PA (PA1 and PA2). The output power is measured by a power meter via a 25 dB attenuator.

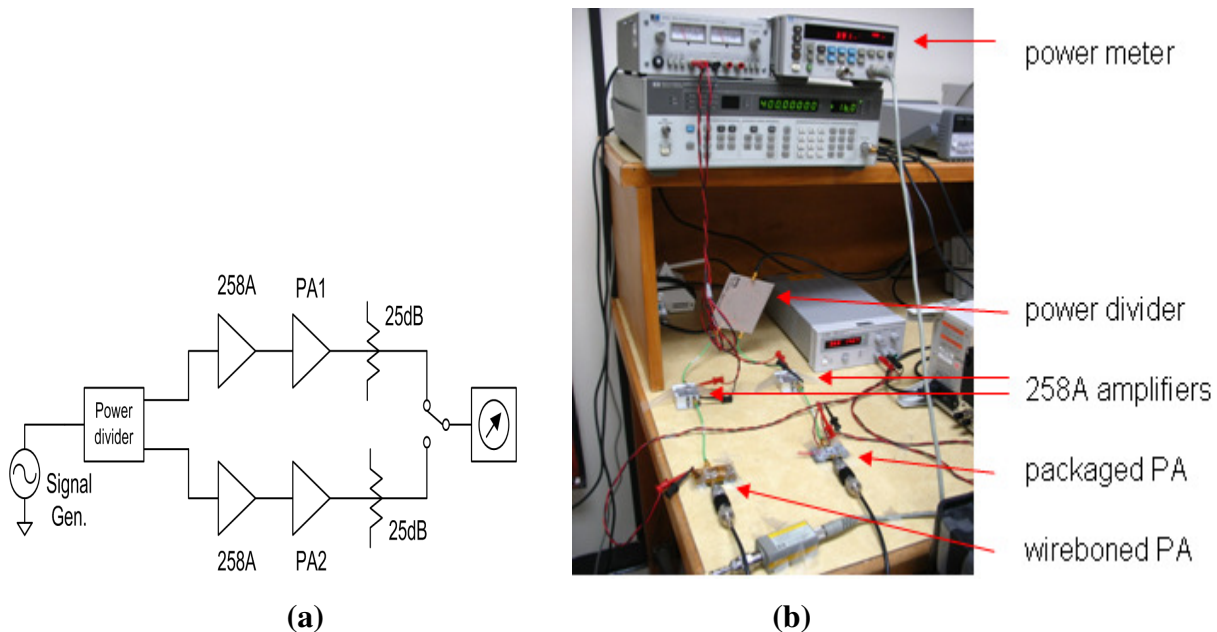


Figure 8-16: Reliability test setup. (a) Schematics, and (b) photo of the test scene.

In the setup in Figure 8-16, the PAs were tested in a continuous-wave mode with 3.3 V nominal supply voltage. Then, the power supply voltage was raised to 4.0 V and then to 4.5 V, which are 121 % and 136 % of the nominal VDC, respectively. For each level of the voltage, the PAs were kept in operation for several days. No damage or degradation in the PAs was observed after the test. The test verifies that the 1-Watt PA can tolerate irregular supply voltage and voltage jumps during the operation.

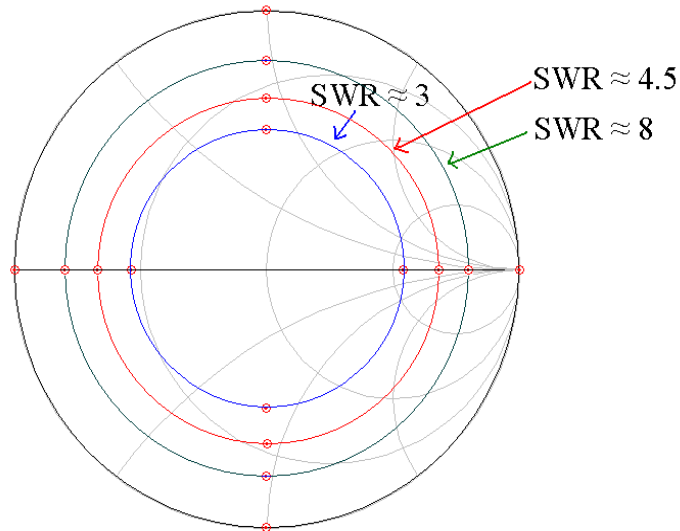


Figure 8-17: Load-pull locations in Smith chart

Also various load-mismatches are provided at the output of the PAs. As shown in the Smith chart (Figure 8-17), open, short, jZ_0 , and $-jZ_0$ terminations are connected. The imaginary loads are devised by transforming the resistive loads along the constant SWR circles with a $1/8$ -wavelength transmission-line. In addition, the PAs were operated with load impedances on a $VSWR \approx 3, 4.5$ and 8 circles by a 3 dB, 2 dB, and 1 dB attenuators respectively and the transmission-lines. The tested output terminations are marked by red dots in the Figure 8-17. The aforementioned situations may occur by mistakes in assembly or by turning on the PA accidentally without a proper termination.

These tests confirm that the PA is robust against the power supply fluctuation and load-mismatches for extended time.

8. Nonlinear Effects of the 1-Watt PA

The 1-Watt PA in a class-E switching-mode topology maximizes efficiency but it suffers from nonlinearity when modulated signal with varying envelope is applied. For demonstration, $4/\pi$ DQPSK modulated signal of NADC was applied to the 1-Watt PA. The input signal constellation is shown in Figure 8-18a. The signal constellation shows abundant envelope information as it moves between dots. However, the envelope information is totally lost and the constellation becomes jittery at the PA output when the 1-Watt PA is strongly compressed as shown in Figure 8-18b. Furthermore, the spectrum in the adjacent channel also grows

significantly, which corrupts the channel. A lower line in Figure 8-18c is input spectrum and the PA output spectrum shows approximately 45 dB increase in the adjacent channel.

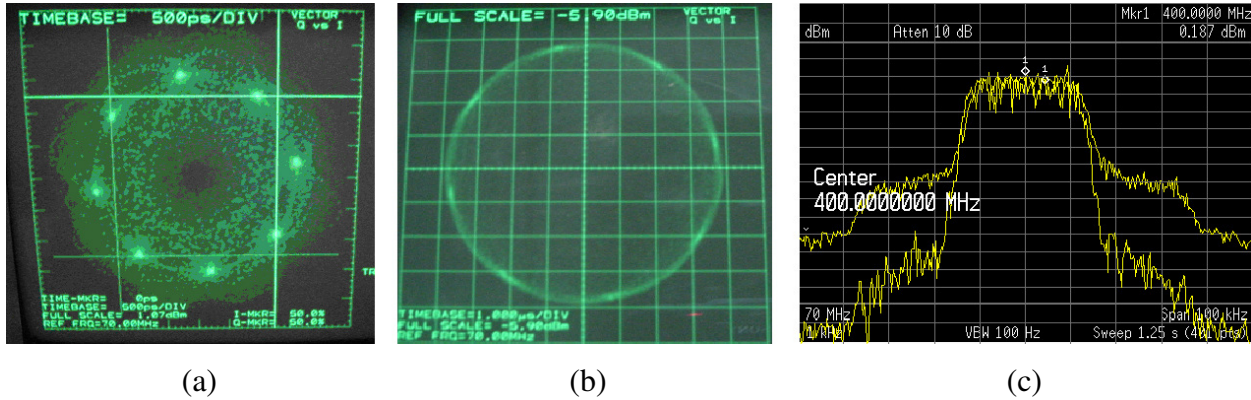


Figure 8-18: Nonlinear effects in $4/\pi$ DQPSK modulation. (a) input signal constellation, (b) PA's output constellation, and (c) spectral re-growth

In order to avoid the nonlinearity effects, class-A and class-B PAs are preferred over the class-E PA but the class-A and B PAs have very low efficiency in power backed-off operation. In the worst case, the PA occasionally needs to generate peak output power but most of the time it is in low power mode such as 6 dB backed-off from the peak power. Various linearization techniques of nonlinear PAs are previously explained in Chapter 2. Particularly the EER (Envelope Elimination and Restoration) can be applied to the 1-Watt PA by substituting a controlled voltage regulator or a DC-DC convertor for the power supply.

Chapter 9 - Extending the Technique to Multi-Watt PA Design

Leveraging the 1-Watt PA circuit design, a multi-Watt CMOS PA is demonstrated. The 1-Watt design provides 50-Ohm single-ended input and output. A 5-Watt extrapolation is created by reworking the I/O circuits (transformers) of the 1-Watt design. Each PA sees 12.5-Ohm and generates 1.25-W output that is power combined by series-connected secondary coils as shown in the schematic of Figure 9-1 below. Hence, only a single 1.25-W die is fabricated for the prototype, limiting cost. Four copies of the dies are connected with bondwires to form the 5-Watt output-stage design. The fifth copy is then used as a drive amplifier. It is important to note that the layout was done to allow a fully-integrated 5-Watt PA to be developed from the same design in later fabrications. The current design employs five copies of a core 1.25-Watt tiles with bondwire interconnects only to save prototyping cost.

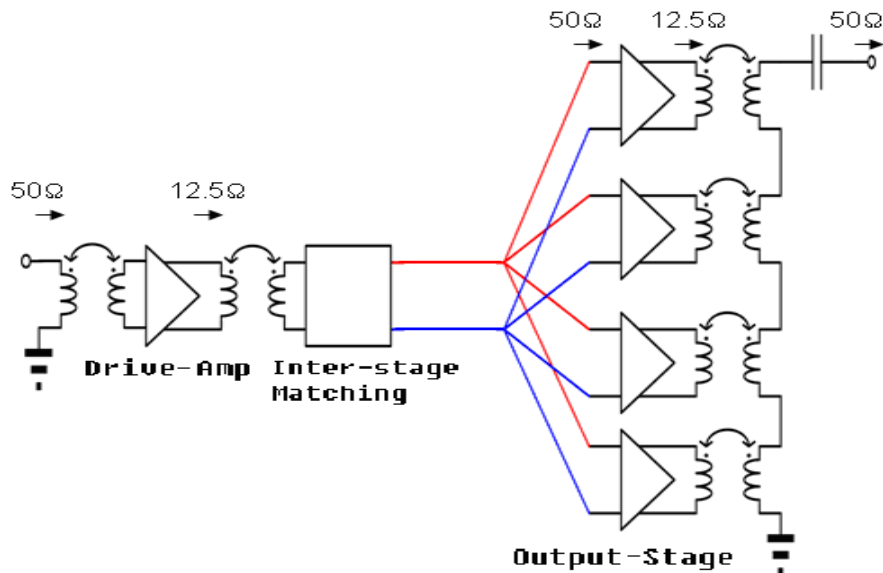


Figure 9-1: SOS five-chip configuration employing power-combining

1. PA Design and Simulation

A 1.25-Watt PA tile's schematics are shown in Figure 9-2. A few changes are made from the Mars 1-Watt PA for the power-combining. In order to minimize phase difference at each unit

PA's input and output, a pair of transistor cells is located in the corner of the chip in the layout as shown in Figure 9-6a. Since the differential power cells do not abut physically, the gates of M3 and M4 are biased via wire-bonds to off-chip ground instead of the resistive voltage-divider self-biasing in the Mars 1-Watt PA. C2 also provides the signal ground for the gates. The output balun has lower inductance values than in the Mars 1-Watt PA both in primary and secondary coils because the PA is matched for 12.5-Ohm load and the balun must not self-resonate when four of them are connected. The stacked PMOS pairs and the class-E/ F_{odd} topology are kept for high V_{bk} and high efficiency.

The 5-Watt two-stage PA's schematics are shown in Figure 9-3 with PCB layout consideration. In the Agilent ADS simulation the PA is capable of 4.6 W output power with PAE of 37 % at 400 MHz, and 20 dBm input as shown in Figure 9-4 and 9-5. 80 MHz 1dB-bandwidth and 180 MHz 3dB-bandwidth are also achieved.

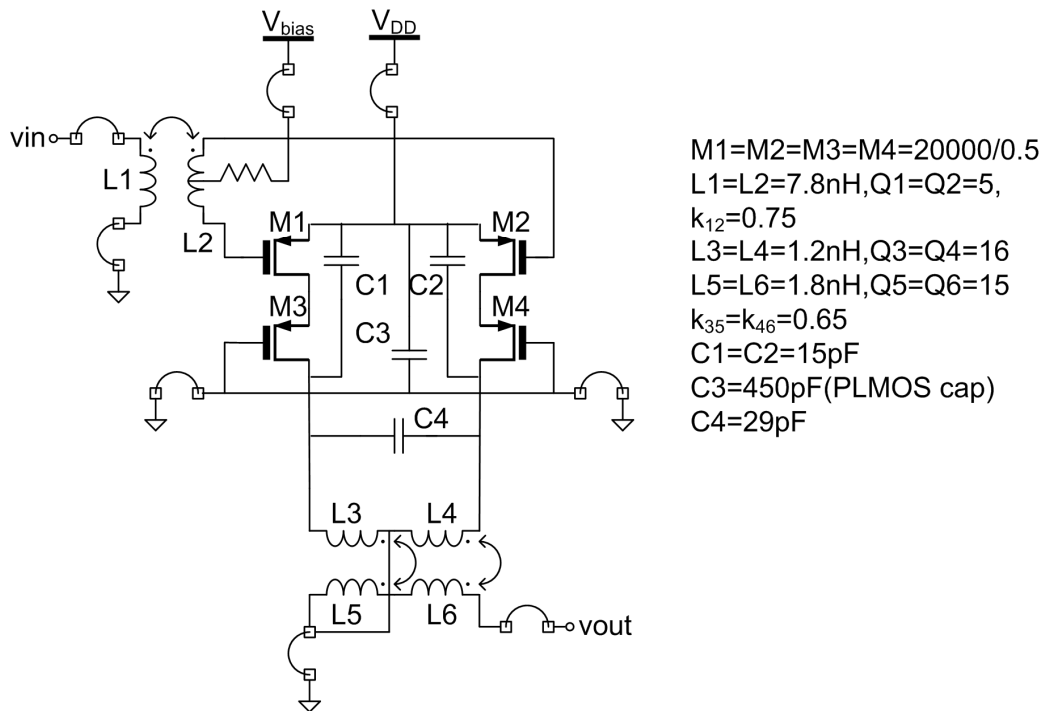


Figure 9-2: Schematics of a single PA chip

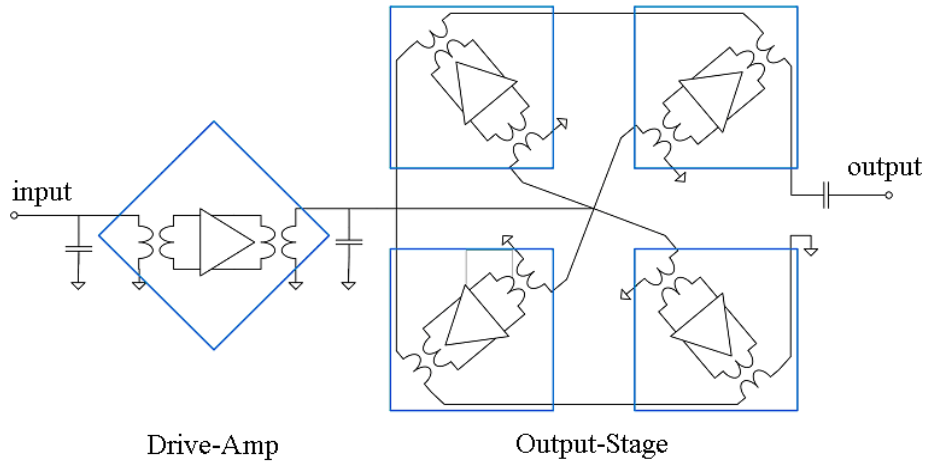


Figure 9-3: Schematics of a five-chip two-stage PA.

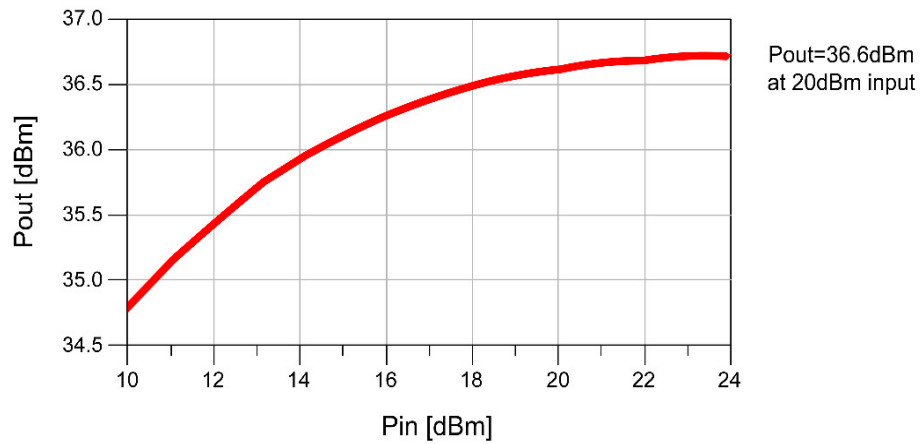


Figure 9-4: P_{out} and P_{in} relation in SOS PA simulation

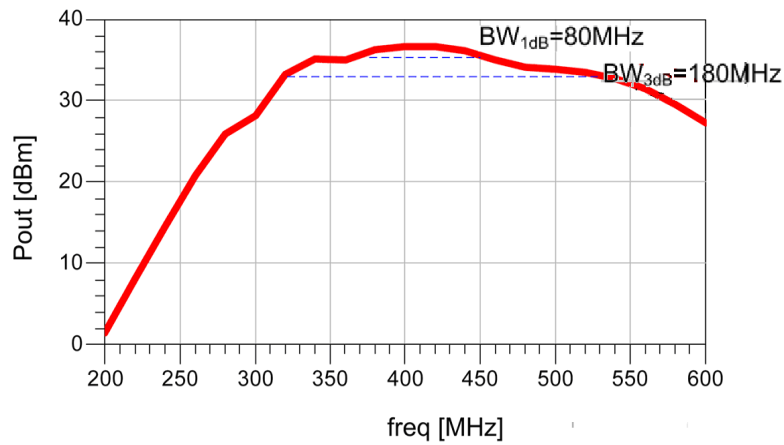


Figure 9-5: P_{out} and frequency relation in SOS PA simulation

2. Implementation and Measurements

Figure 9-6 shows pictures of the wire-bonded 5-Watt PA. In Figure 9-6b, the chip on the left hand side drives the four-chip output-stage PA on the right hand side. Capacitors between the stages are small-valued and can be integrated with ease when a $7 \times 10 \text{ mm}^2$ die is granted for the whole PA integration. Figure 9-6a shows the closeup of the single tile.

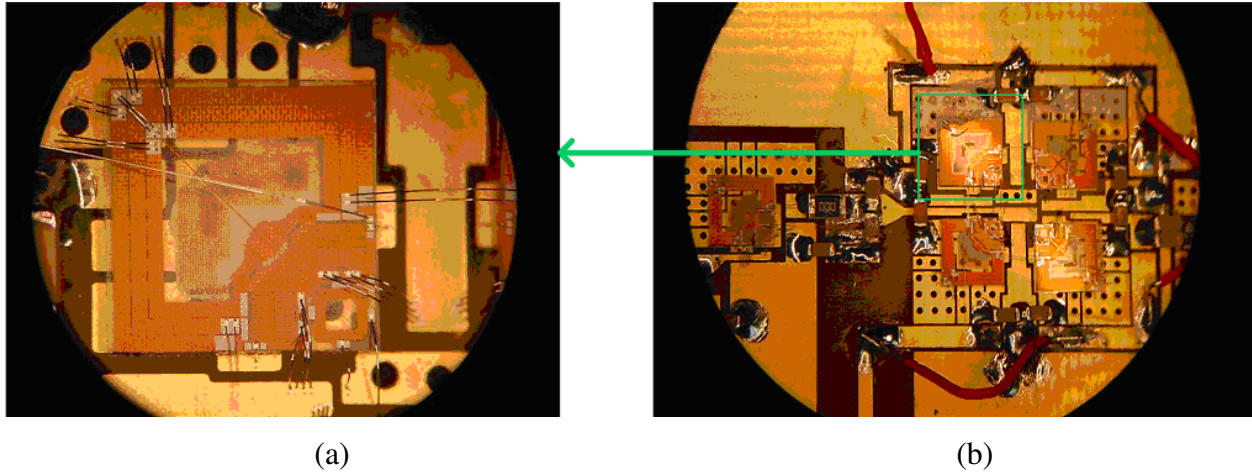


Figure 9-6: Photo of (a) the PA unit and (b) the five-chip PA assembly

Four-chip Output-Stage

Prior to building up the full five-chip PA, only the four-chip on the left was tested with 28 dBm input power by an external power amplifier and 4.5 V power supply. Since the output-stage is designed with the 31 dBm (1.25-Watt) drive-amp and 3 dB attenuation in the inter-stage matching as shown in Figure 9-1, the external input is set at 28 dBm. In the measurements, the PA generates 4.3-Watt at 520 MHz with 19 % drain efficiency and 17 % PAE. Gain of the PA is 8.4 dB. When P_{in} is 30 dBm, P_{out} is 5.1-Watt as shown in Figure 9-7 with 21 % drain efficiency and 17 % PAE. Figure 9-8 shows that its 1dB BW is greater than 20 %. The 120 MHz frequency offset from the intended 400 MHz center frequency is caused by a layout mistake, but the reason of two dips at 450 MHz and 550 MHz are not known. It is possible that they will disappear once the frequency offset is corrected. However, more investigation is required. Figure 9-9 depicts linearly increasing output power in the power supply sweep, suggesting feasibility of power control by supply modulation.

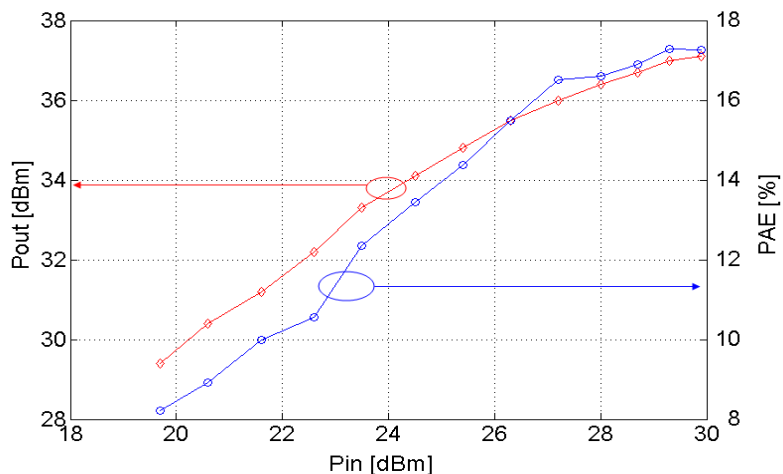


Figure 9-7: P_{out} and PAE measurement in P_{in} sweep by the external PA

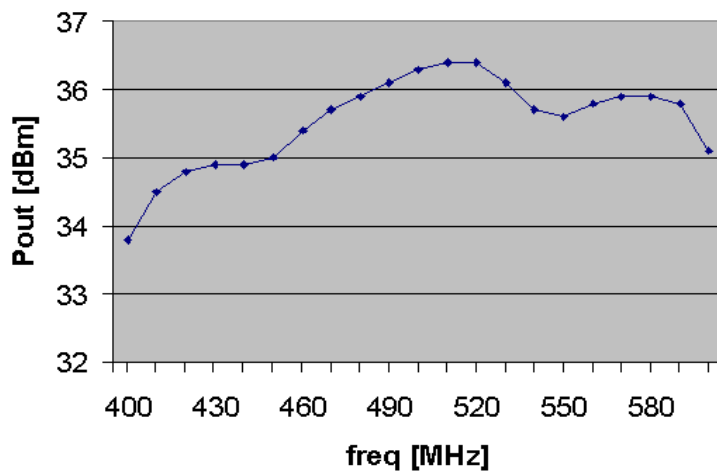


Figure 9-8: Output power in frequency sweep

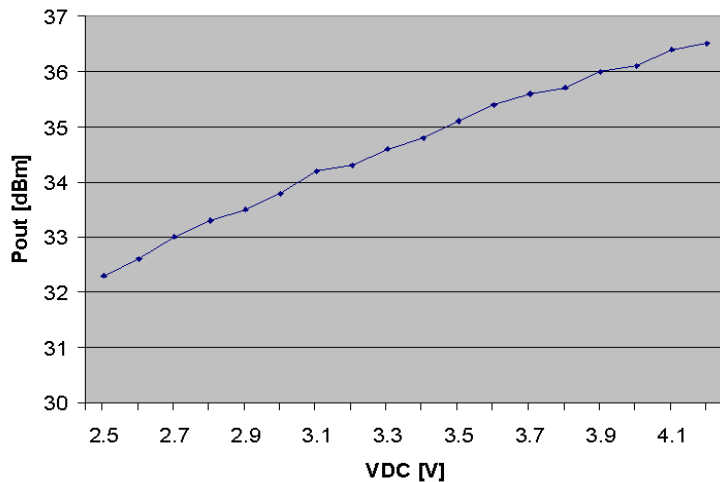


Figure 9-9: Output power in power supply sweep

Load-pull and Inter-Stage Matching

A load-pull test was carried out in order to validate the drive-amplifier's output capability and to design the inter-stage matching.

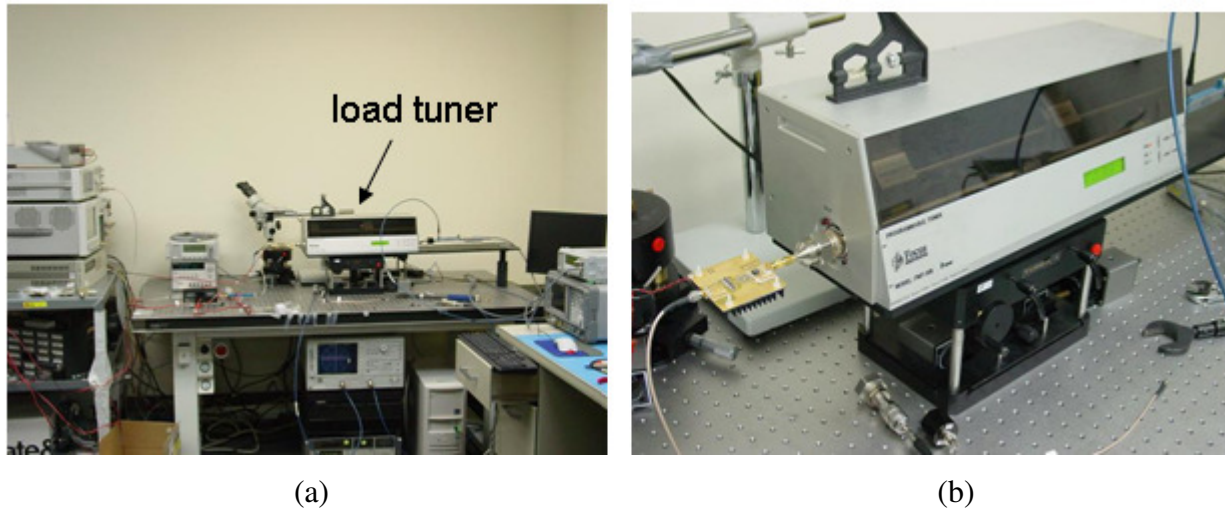


Figure 9-10: (a) The load-pull measurement setup and (b) load tuner with the PA attached

Figure 9-10 shows the load-pull measurement setup. The PAs are connected to output load tuner and output power is measured with varying load impedance on the Smith chart. A computer program draws output power contours as shown Figure 9-11 and the center point of the contours conditions the maximum output power case.

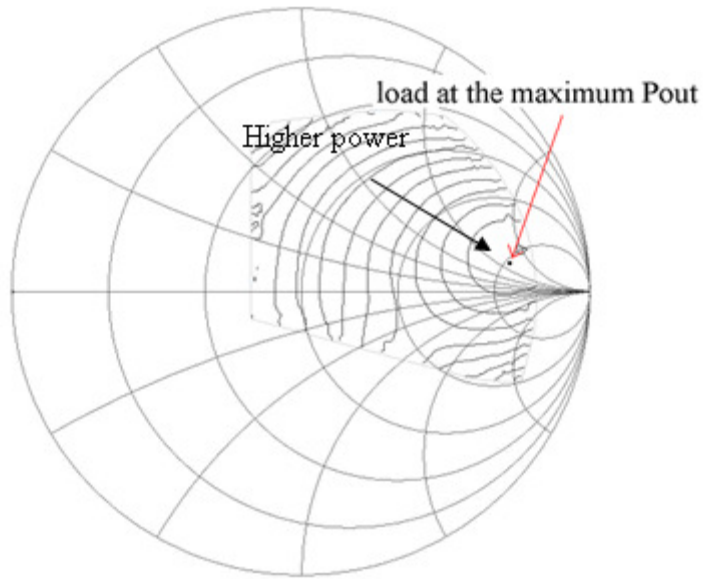


Figure 9-11: Output power contours by the drive-amplifier

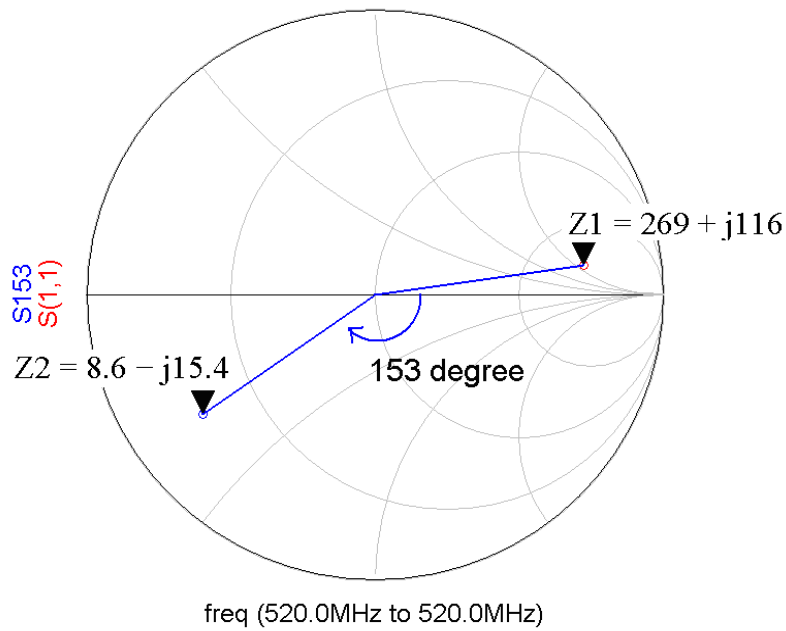


Figure 9-12: Load tuner connectors and transmission-line compensation in ADS simulation

The drive-PA generates 28.8 dBm output at $Z_{load} = 269 + j116$ as shown in Figure 9-11. The plot can be misleading since the output power increases as magnitude of the load increases. However, this load-pull plot is not compensated for an electric length of connectors and the

transmission-line between the tuner and the PA chip. Actual connection for the test is shown in Figure 9-10b. When the extra length is measured alone, it was equivalent to 153° phase rotation and the compensation is depicted in Figure 9-12. Therefore, the load impedance at the edge of the drive-PA chip $Z_{P_{max}}$ is $8.6 - j15.4$ for the maximum power, which is close to the initial design assumption, 12.5-Ohm driving.

The input impedance of the output-stage was measured and $Z_{in,out-stage} = 58 + j10.4$. A shunt capacitor of 25 pF is used for the inter-stage matching to drive the output-stage with the maximum power. The PCB layout of the two-stage PA with matching networks is shown in Figure 9-13.

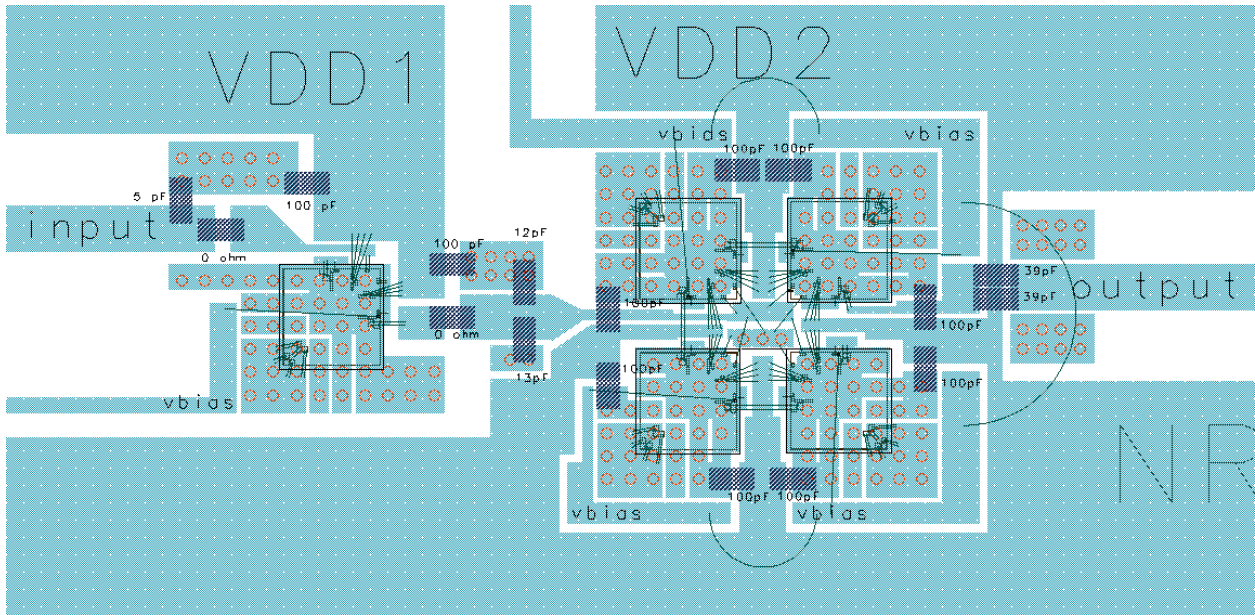


Figure 9-13: PCB layout of the two-stage PA

3. Two-Stage Five-Chip PA and Future Work

Finally, preliminary measurement results from the whole five-chip PA in Figure 9-1 were obtained. As shown in Figure 9-14, the output power of this prototype was 5.1-Watt (37.1 dBm) at 480 MHz with 17 % PAE when 20.6 dBm was provided to the drive-amplifier. To the author's knowledge, the 5.1-Watt output power is the highest ever reported by an integrated CMOS PA. Figure 9-15 shows that the PA has approximately 75 MHz (16 %) 1-dB bandwidth.

However, the center frequency is off-tuned and PAE is low. The frequency offset is an easy fix in layout but the low efficiency problem needs further investigation. It is suspected that part of bias circuitry is damaged by inaccurate wire-bonding. We believe that bonding with smaller contact area will solve the problem. Finally, the bonding is not an issue after all if $7 \times 10 \text{ mm}^2$ die is given for full integration in the future project.

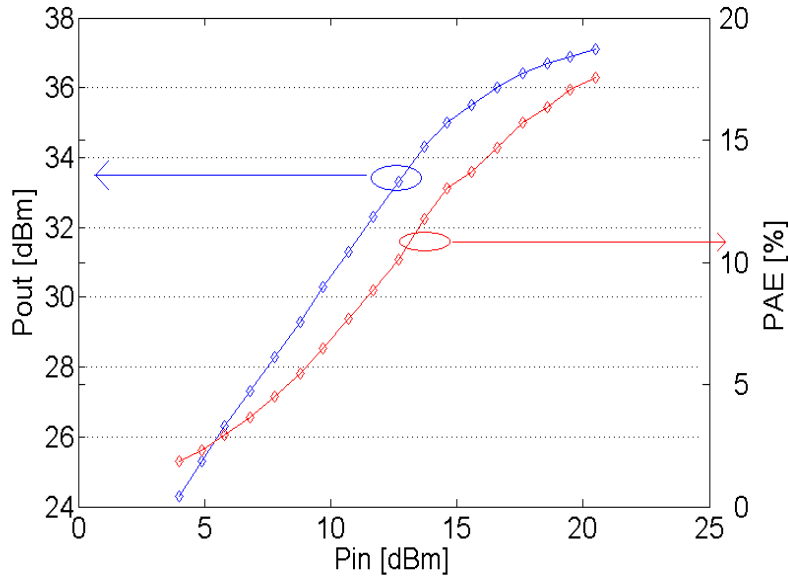


Figure 9-14: PA measurements: P_{in} Vs. P_{out} and PAE.

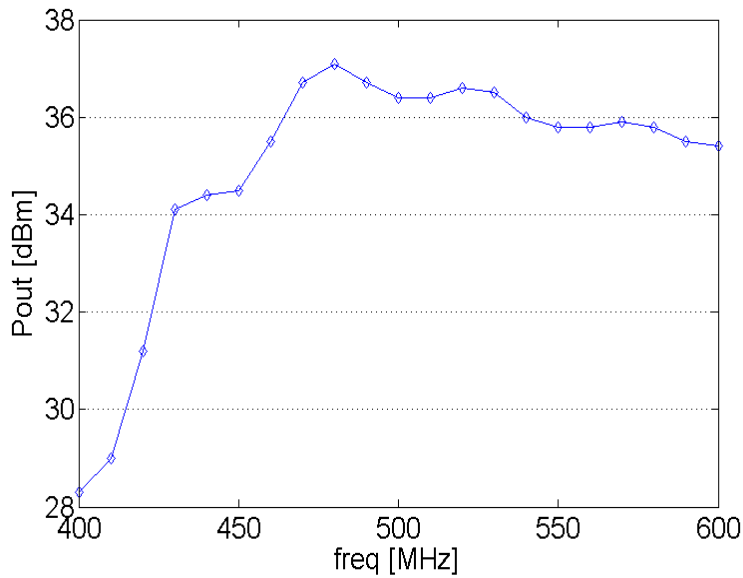


Figure 9-15: PA measurements: frequency Vs. P_{out} .

Chapter 10 - Conclusions

A fully-integrated Watt-level CMOS PA has been a tough hurdle to overcome due to the process's digital-oriented characteristics. Although successful Watt-level PAs have been reported, many depend on off-chip components such as bondwires and transmission lines, while others are not easily scaled to lower frequencies. In order to achieve high reproducibility and to pursue a single chip radio, the off-chip components must be avoided. This thesis discusses design challenges and provides solutions of Watt-level UHF CMOS power amplifiers, demonstrating a fully integrated UHF 1-Watt CMOS PA in a CMOS SOS process.

For 1-Watt PA design, high V_{bk} PMOS transistors are stacked up instead of NMOS to deliver high output without lowering power supply. High Q transformer/balun on SOS process eliminates the needs for off-chip output matching network and a balun. The PA in standard package delivers 29 dBm with 29 % PAE at 20 dBm input and 3.3 V power supply. Over 1-Watt output with 27 % PAE is also measured either with higher input power or higher power supply. It can also be combined with the resonant TR switch without significant NF degradation at receive mode. The transceiver in conjunction with the 1-Watt PA features less than 5 % transmission power loss and 0.6 dB NF degradation from LNA's original 3.4 dB NF. The PA's stability is analyzed by large-signal S-parameter k-factor and an auxiliary generator method. Furthermore, thermal analysis using commercial software has shown that the PA's maximum junction temperature is 78 °C. Despite the sapphire substrate's moderate thermal conductivity, the large power cells area mitigates heat elevation. The PA is the first fully integrated 400 MHz band CMOS 1-Watt PA to the author's knowledge.

Extending the design techniques in the 1-Watt PA, a multi-Watt PA is demonstrated in SOS process using multiple copies of the identical chips. The Mars 1-Watt PA is modified in order to power-combine four output baluns in series. A preliminary two-stage five-chip PA generates 37.1 dBm with 20.6 dBm input at 17 % PAE. The output power is the highest ever reported by an integrated CMOS PA to the author's knowledge. Although the efficiency is low due to damaged bias circuits, the design implies the feasibility of high gain and high output power amplifier in SOS process in the future project.

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Appendix A - Output Power as a Function of Breakdown Voltage

It is assumed in the following derivations that push-pull transformer-coupled PAs are in ideal conditions and v_D is driven up to V_{bk} . Therefore, knee voltage, switch loss, and transformer loss are neglected ($V_k = 0$, $R_{on} = 0$, and $\eta_T = 100\%$). A 1:1 output transformer ratio is assumed as $1/2$ is substituted for m/n in the following equations. The schematic of the transformer is shown in Figure A-1.

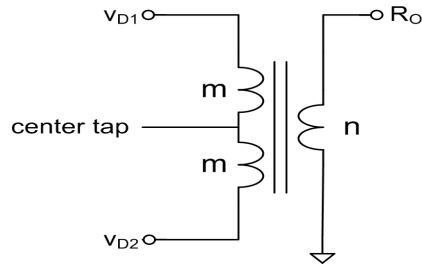
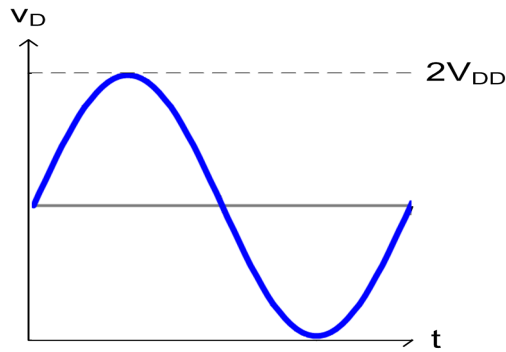


Figure A-1: Schematic of the output transformer.

Class-A, B, AB and C



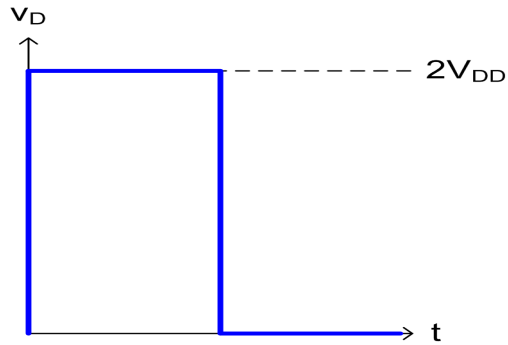
$$P_o = \frac{V_{DD}^2}{2 \left(\frac{m^2}{n^2} \right) R_o} = \frac{2V_{DD}^2}{R_o},$$

$$V_{DD} = \frac{V_{bk}}{2},$$

$$P_o = 0.5 \frac{V_{bk}^2}{R_o},$$

Figure A-2: Drain voltage waveforms in class-A, B, AB and C PAs

Voltage-switching Class-D and Class-F



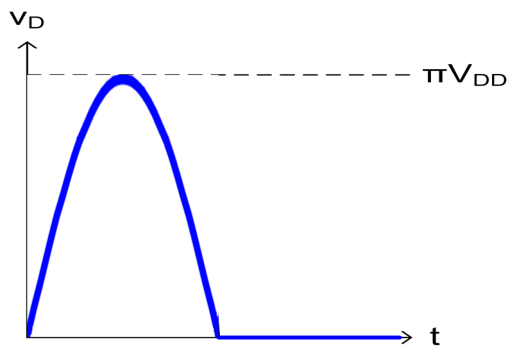
$$P_o = \frac{8}{\pi^2} \frac{V_{DD}^2}{\left(\frac{m^2}{n^2}\right) R_o},$$

$$V_{DD} = \frac{V_{bk}}{2},$$

$$P_o = \frac{8}{\pi^2} \frac{V_{DD}^2}{R_o} \approx 0.81 \frac{V_{bk}^2}{R_o}$$

Figure A-3: Drain voltage waveforms in voltage switching class-D and class-F PAs

Current-switching Class-D and Class-F⁻¹



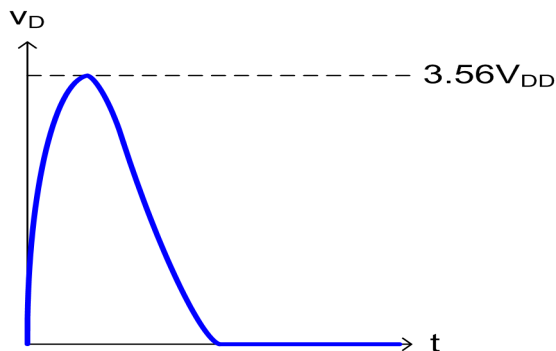
$$P_o = \frac{\pi^2}{8} \frac{V_{DD}^2}{\left(\frac{m^2}{n^2}\right) R_o},$$

$$V_{DD} = \frac{V_{bk}}{\pi},$$

$$P_o = 0.5 \frac{V_{bk}^2}{R_o}$$

Figure A-4: Drain voltage waveforms in current voltage switching class-D and class-F⁻¹ PAs

Traditional Class-E (Shunt C)



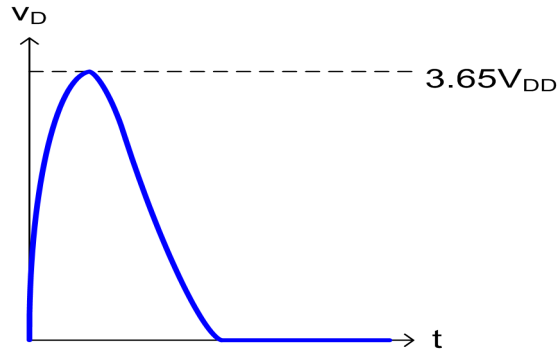
$$P_o = 0.577 \frac{V_{DD}^2}{\left(\frac{m^2}{n^2}\right) R_o},$$

$$V_{DD} = \frac{V_{bk}}{3.56},$$

$$P_o = 0.18 \frac{V_{bk}^2}{R_o}$$

Figure A-5: Drain voltage waveforms in traditional class-E PAs

Parallel circuit Class-E (Finite RFC)



$$P_o = 1.365 \frac{V_{DD}^2}{\left(\frac{m^2}{n^2}\right) R_o},$$

$$V_{DD} = \frac{V_{bk}}{3.65},$$

$$P_o = 0.41 \frac{V_{bk}^2}{R_o}$$

Figure A-6: Drain voltage waveforms in parallel circuit class-E PAs

Appendix B - Input Impedance at the Transformer Primary

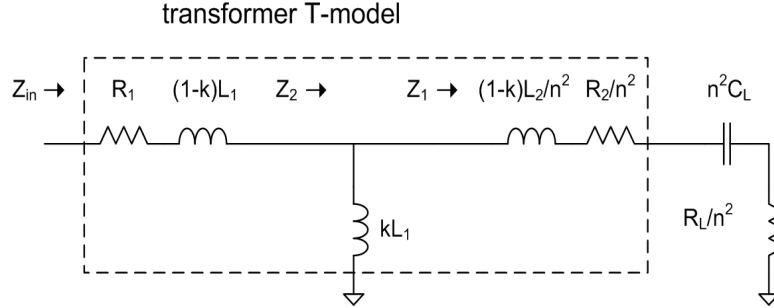


Figure B-1: Transformer T-model with a load resistor and a series capacitor.

When the transformer secondary is terminated with a load resistor (R_L) and a series capacitor ($1/\omega C_L = \omega L_2$), the input impedance at the primary can be calculated by the following equations.

$$\begin{aligned} Z_1 &= \frac{j\omega(1-k)L_2}{n^2} + \frac{R_2}{n^2} + \frac{1}{j\omega n^2 C_L} + \frac{R_L}{n^2} \\ &= \frac{1}{n^2} (R_2 + R_L - jk\omega L_2) \end{aligned} \quad (\text{B.1})$$

$$\begin{aligned} Z_2 &= j\omega kL_1 \parallel Z_1, \\ &= \left(\frac{1}{j\omega kL_1} + \frac{n^2}{R_2 + R_L - jk\omega L_2} \right)^{-1} \\ &= \frac{(k\omega)^2 L_1 L_2 + j\omega kL_1 (R_2 + R_L)}{R_2 + R_L}, \quad L_2 = n^2 L_1 \end{aligned} \quad (\text{B.2})$$

Therefore,

$$\begin{aligned} Z_{in} &= R_1 + j\omega(1-k)L_1 + j\omega kL_1 + \frac{(k\omega)^2 L_1 L_2}{R_2 + R_L} \\ &= R_1 + j\omega L_1 + \frac{(k\omega)^2 L_1 L_2}{R_2 + R_L}. \end{aligned} \quad (\text{B.3})$$

Appendix C - NF Calculation

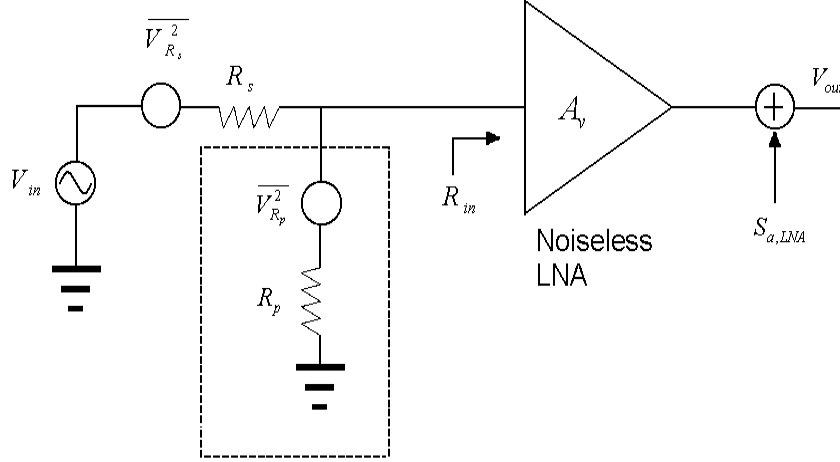


Figure C-1: Noise model of the TR switch. Added noise $S_{a,LNA}$ is separated from the ideal LNA

NF of an LNA before a PA is attached can be calculated directly from Figure C-1 excluding the dotted box. The results are

$$\left(\frac{S_i}{N_i} \right)_{LNA} = \frac{V_{in}^2 \left(\frac{R_{in}}{R_s + R_{in}} \right)^2}{V_{R_s}^2 \left(\frac{R_{in}}{R_s + R_{in}} \right)^2} \quad (C.1)$$

$$\left(\frac{S_o}{N_o} \right)_{LNA} = \frac{V_{in}^2 \left(\frac{R_{in}}{R_s + R_{in}} \right)^2 A_v^2}{V_{R_s}^2 \left(\frac{R_{in}}{R_s + R_{in}} \right)^2 A_v^2 + S_{a,LNA}} \quad (C.2)$$

$$F_{LNA} = \frac{(S_i/N_i)_{LNA}}{(S_o/N_o)_{LNA}} = 1 + \frac{S_{a,LNA}}{\overline{V_{R_s}^2} A_v^2 \left(\frac{R_{in}}{R_s + R_{in}} \right)^2}. \quad (C.3)$$

R_s is source resistance and also equivalent to R_{ant} in (C.1). The LNA is composed of a noiseless LNA and added noise $S_{a,LNA}$. The LNA has voltage gain A_v and its input resistance is R_{in} . Noise model of the PA's output is a parallel resistance R_p at the LNA input. New noise factor with PA (F_{new}) can be found as

$$\left(\frac{S_i}{N_i} \right)_{new} = \frac{V_{in}^2 \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2}{\overline{V_{R_s}^2} \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2} \quad (C.4)$$

$$\left(\frac{S_o}{N_o} \right)_{new} = \frac{V_{in}^2 \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2 A_v^2}{\overline{V_{R_s}^2} \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2 A_v^2 + \overline{V_{R_p}^2} \left(\frac{R_s \parallel R_{in}}{R_p + R_s \parallel R_{in}} \right)^2 A_v^2 + S_{a,LNA}} \quad (C.5)$$

$$F_{new} = \frac{(S_i/N_i)_{new}}{(S_o/N_o)_{new}} = \frac{\overline{V_{R_s}^2} \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2 + \overline{V_{R_p}^2} \left(\frac{R_s \parallel R_{in}}{R_p + R_s \parallel R_{in}} \right)^2 + \frac{S_{a,LNA}}{A_v^2}}{\overline{V_{R_s}^2} \left(\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} \right)^2}$$

$$= 1 + \frac{R_s}{R_p} + \frac{\frac{S_{a,LNA}}{A_v^2}}{\overline{V_{R_s}^2} \left(\frac{R_s \parallel R_p \parallel R_{in}}{R_s} \right)^2}. \quad (C.6)$$

where

$$\frac{R_s \parallel R_{in}}{R_p + R_s \parallel R_{in}} = \frac{R_s \parallel R_p \parallel R_{in}}{R_p}, \quad (\text{C.7})$$

$$\frac{R_p \parallel R_{in}}{R_s + R_p \parallel R_{in}} = \frac{R_s \parallel R_p \parallel R_{in}}{R_s}. \quad (\text{C.8})$$

Using (C.3) and assumption that $R_s=R_{in}$,

$$F_{new} = 1 + \frac{R_s}{R_p} + \frac{\left(\frac{R_s}{R_s + R_{in}}\right)^2 (F_{LNA} - 1)}{\left(\frac{R_s \parallel R_p \parallel R_{in}}{R_s}\right)^2} = 1 + \frac{R_s}{R_p} + \frac{(F_{LNA} - 1)}{\left(\frac{R_p}{\frac{R_s}{2} + R_p}\right)^2}. \quad (\text{C.9})$$

Figure 7-5 depicts the NF degradation due to the PA. For a fixed R_p , the NF_{new} is nearly a sum of NF_{LNA} and a constant in the plot. When R_p is comparable to R_s , the NF_{new} is much worse than NF_{LNA} but as R_p becomes much bigger than R_s , the degradation becomes unnoticeable. The microtransceiver's LNA has 3.4 dB NF and the PA's output resistance is 360 Ω . Hence, from (C.9) NF_{new} is expected to be 4.0 dB. If $R_s/2R_p \ll 1$, which is true with the high Q output transformer, F_{new} can be further simplified to

$$F_{new} \approx 1 + \frac{R_s}{R_p} + (F - 1) \left(1 + \frac{R_s}{R_p}\right) = F \left(1 + \frac{R_s}{R_p}\right). \quad (\text{C.10})$$