DESIGN AND IMPLEMENTATION OF A COTS-BASED FLIGHT COMPUTER

by

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ABSTRACT

Instead of designing new proprietary hardware to replace aging, obsolete systems, the defense industry is looking towards Components Off The Shelf (COTS). COTS are attractive for a number of reasons. First, by using COTS, nonrecurring design costs are divided among all costumers. Second, because COTS suppliers have an economy of scale, the suppliers are able to reduce the cost of components, making systems more affordable than low-volume, proprietary solutions. Third, using COTS accelerates the time to market by reducing the time required for design and making extensive design verification unnecessary. Fourth, COTS hardware produces a scalable solution, as one COTS systems could easily be replaced with a different COTS system that would more readily meet the customer's unique demands.

This thesis attempts to explain the implementation of a COTS-based flight computer. The PCI Mezzanine Card (PMC) standard has been selected because it is both rugged and widely accepted by industry. The PMC is a common standard with a variety of COTS parts, making it easily exchangeable. While the COTS solution reduces design overhead, it does not eliminate the need for design altogether. Although the contractor would no longer be required to design the features provided by the COTS, they would be required to design the overall system and the integration of the COTS.

This thesis documents the design of a system that takes two PMC cards – the COTS – and integrates those cards together and interfaces them with the flight systems. The interfacing of COTS components is also extended to provide a high-speed serial link in order to connect two PMC carrier boards for a total of four COTS PMCs. Further, the testability of the final system is explored to provide an end product that is verifiably sufficient.

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CHAPTER 1: INTRODUCTION

In the fall of 2003, the Missile Navigation Guidance and Controls (NGC) department of Sandia National Laboratories invited Kansas State University to participate in research of various aspects in the design of a new flight computer. The specific research topic eventually settled on was the design for both a single and double Peripheral Component Interconnect (PCI) Mezzanine Card (PMC) carrier that could potentially be used as a new flight computer. The custom carrier would provide limited functionality and hold Comercial Off The Shelf (COTS) PMC cards to perform processing and meet interfacing input/output (IO) needs. The single PMC carrier is referred to as the IMPACCT 1 and the dual PMC carrier the IMPACCT 2.

Given the immediate need for a flight computer, Sandia's NGC group enlisted the help of two other groups. First, the flight computer group at Sandia created their own dual PMC carrier with much greater functionality. Also, existing commercial solutions were considered. While these solutions provided an alternative that was immediately available, the form factor and lack of configurability were drawbacks.

A. Sandia's Outmoded Flight Computer

SANDAC, Sandia's outmoded flight computer, is being replaced by the new IMPACCT design. The SANDAC was a proprietary, complex, multiprocessor computer based on the Motorola 68040. The system's computational and interfacing resources were expandable by adding custom modules onto a proprietary “global” bus. The physical size of the SANDAC was dependent on the number of modules required to perform the task.

After several of the components where made obsolete by their respective manufacturers, Sandia decided to stop investing considerable sums of money to maintain and update the proprietary flight computer.

B. COTS and IMPACCT

After many discussions within Sandia, a consensus was reached to pursue a flight computer based on COTS. This is becoming a common practice in the defense industry, as more

contractors are working tighter budgets and stricter deadlines. Using commercially available components reduces nonrecurring engineering costs, enables faster time to market, and allows for a product which can upgrade more easily as the commercial market continually evolves.

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Within the COTS market, several different technologies exist to connect components to create complex systems. Within these interconnect technologies there are several physical form factors that exist to accommodate the physical environments where they must function. Sandia decided on the PMC standard described in[1][2]. This standard describes a small mezzanine card that uses the PCI bus to interconnect I/O and/or a processor.

C. KSU Involvement

Throughout the past two years, Kansas State University has been involved in many aspects of the development of a new flight computer for Sandia's NGC department. Initially, KSU was charged with benchmarking the prospective CPU that would be used on the Processor PMC (PrPMC) in order to evaluate its potential to replace the SANDAC. It was quickly verified that the newer single processor overwhelmingly out-performed the multiprocessor SANDAC.

Later, it was decided that there might be a need for an FPGA (Field Programmable Gate Array) customizable PCI target for configurable I/O on the new flight computer. Such a configurable target could connect to the COTS system via the PCI bus and provide a large variety of functionality to the flight computer that could not be obtained easily from a commercial vendor. KSU, in the spring of 2004, built a simple PCI target that could be altered to interface with various I/O solutions. While KSU's attempt to implement the PCI target was successful, interest in an FPGA PCI target waned.

In the summer of 2004, Sandia's NGC department, while in discussions with the flight computer group at Sandia, concluded that a custom carrier was desired to house the COTS PrPMC card and interface to other PMC I/O cards. The custom carrier would be known as IMPACCT.

While using COTS greatly reduces system costs and design and implementation time, there is still need for a carrier which glues the COTS together and provides an interface to the missile.

The need was first addressed when KSU was asked to perform the initial design of the IMPACCT family by creating a simple single PrPMC carrier called the IMPACCT 1. The initial design was a board which a PrPMC could plug into for power and for I/O connections along with basic flight computer monitoring.

Finally, in the fall of 2004, Sandia became interested in having KSU extend the IMPACCT 1 into a dual PMC carrier with added functionality. Despite the fact that Sandia's own flight computer group was working on a more complex version of IMPACCT 2, the customer, NGC, decided to pursue KSU's version of the IMPACCT 2. Sandia determined that KSU's version of the IMPACCT 2 had a more appealing form-factor and was more expandable because of its use of StarFabric. StarFabric is a protocol standard created by Stargen for expanding bus technologies, such as PCI, to accommodate larger, physical links and complex topologies. This thesis documents the development of the IMPACCT 1 and the IMPACCT 2 PMC carriers, which are a major part of Sandia's new IMPACCT flight computer line.

CHAPTER 2: BACKGROUND

Three major technologies should be introduced before detailing the design and implementation of both versions of the IMPACCT flight computers. The first major technology is the PCI bus. Used in the embedded and consumer computing market, the PCI bus is the interconnect technology used to connect the COTS boards together and is facilitated on the carrier board. The second technology, the PMC form factor, is used for the COTS PCI cards. The PMC specification was an important factor in the design of the IMPACCT carriers, as it provides a rugged COTS systems. Finally, a major advantage of the IMPACCT 2 over competing designs is the ability to connect two carriers together for increased I/O while spanning a substantial physical distance. StarFabric is the technology responsible for this connection.

A. The PCI Bus

A.1 PCI Bus History

A major component of the early IBM-PC, the open standard of personal computers that forever changed the computing industry, was the Industry Standard Architecture (ISA) bus. The 8-bit ISA bus was created in the early 1980s by IBM. The simple bus with minor changes provided the personal computing industry with its primary high-speed system interconnect for more than ten years, allowing a variety of third-party devices to be created for the PC. However, as processing speeds increased and computing peripherals' need for bandwidth increased, the older ISA standard was no longer able to keep up with demand, even with an expanded 16-bit bus width. Intel proposed a new standard called the Peripheral Component Interconnect to prevent the industry from being segmented with various bus architectures. Their proposal addressed the major issues of ISA speed and device configurability. A special interest group was founded in 1992 to maintain the PCI specification. Shortly after the founding of the PCI Special Interest Group, the first PCI specification version 1.0 was released. Since PCI's inception four additional versions, 2.1, 2.2, 2.3, and 3.0 of the specification have been released.

A.2 PCI Basics

The PCI bus is a parallel 32/64-bit synchronous bus. Usually, the device is mapped into the processor's memory address space by the operating system or by firmware through a

configuration transaction. Any device on the PCI bus can then be accessed by simply reading/writing to the appropriate address. PCI devices are grouped into two families: the master and the target. Master devices can initiate transactions on the bus and respond to requests for access, while targets only respond to requests.

Certain functions needed by a PCI bus that are not provided by PCI masters or targets must be provided by some other system. This system is referred to as the central resource. The central resource provides clocking, reset, and bus arbitration.

The host processor serves an important role as a master. More than one processor can exist on a PCI bus; however, to prevent conflicts, only one processor should allocate resources and map PCI devices into a single memory space. The processor responsible for PCI bus initialization is referred to as the system monarch.

Table 1 lists the required signals when implementing a master or target PCI device. The PCI bus uses a technique called reflective wave switching. Reflective wave switching is unlike the traditional incident wave switching of the digital electronics world. Incident wave switching drives enough current onto a line in order to assert a logic 1 or 0 in a single step. Reflective wave switching relies on the transmission line properties of the signal's trace and its termination in order to ring up the line to obtain the desired logic level. A special driver is used to drive the line partially to the desired logic level. The signal reaches the end of the transmission line and is reflected back, doubling the voltage present on the line. After completing the round trip, the wave front is absorbed by the driver. It is at this time that the line is said to be settled. The round trip must occur in less than 1 PCI clock cycle. Therefore, on the rising edge of the PCI clock, the logic levels are evaluated on the signal lines and the correct logic level is obtained [6].

While designing and conforming to a reflective wave switching scheme is more complex than incident wave switching, the implementation is simplified because termination resistors are unnecessary. Reflective wave switching allows the driver to be half the size and the switch half the current when compared to the incident wave driver. However, the benefits of reflective wave switching do not come without costs. Running the PCI at 33 MHz puts physical limits on the

bus in order to guarantee that its signal lines settle in the appropriate time frame. For example, propagation delay for signals is specified to be 10ns so that the signal line has settled well within the 30ns clock cycle of the PCI bus. The clock skew is also important to guarantee a valid signal is on the bus when the signal is latched and is specified to be a max of 2ns [6][8].

Table 1. PCI Signal Definitions [8].

Signal(s)	Master	Target	Description
Access/Data and Command			
AD[31:0]	IN/OUT	IN/OUT	Contain address and data for bus transactions
C/BE#[3:0]	OUT	IN	Contain command type for transaction and valid byte lanes for AD signal lines
Interface Control			
PAR	IN/OUT	IN/OUT	Provides even parity across AD and C/BE# lines
FRAME#	IN/OUT	IN	Identifies the beginning of a bus transaction
TRDY#	IN	OUT	Indicates when the PCI target is ready to complete the bus transaction
IRDY#	IN/OUT	IN	Indicates when the PCI bus master is ready to complete the bus transaction
STOP#	IN	OUT	Indicates the target wants to end the transaction without the master completing any or all accesses
IDSEL	IN/OUT	IN	Indicates master is accessing targets configuration space
DEVSEL#	IN	OUT	Indicates the target has decoded the address on the AD lines and claims the bus transaction
Arbitration			
REQ#	OUT	NA	Request to the bus arbitrator for bus ownership
GNT#	IN	NA	Response from bus arbitrator granting bus access
System			
CLK	IN	IN	Driven by central resource; all synchronous signal lines are sampled on rising edge of clock with a maximum frequency of 33.3Mhz or 66.6Mhz
RST#	IN	IN	Driven by central resource; causes all PCI devices to reset
Error Reporting			
PERR#	IN/OUT	OUT	Indicates an error in data parity in the AD, C/BE#, PAR and PAR64
SERR#	OUT	OUT	Indicates an error in the address parity in AD, C/BE#, PAR and PAR64
Interrupt Request			
INTA# - INTD#	OUT	OUT	Indicates that PCI target requests service from CPU
J-TAG			
TDI	IN	IN	J-TAG input port
TDO	OUT	OUT	J-TAG output port
TCK	IN	IN	J-TAG clock reference
TMS	IN	IN	J-TAG TAP controller input
TRST#	IN	IN	J-TAG TAP controller reset
Power Management			

PME#	OUT	OUT	Signals central resource that a PCI device is requesting a power management event
64-Bit Extension			
AD[63:32]	IN/OUT	IN/OUT	32 additional AD signal lines for 64 bit operation
PAR64	IN/OUT	IN/OUT	Provides even parity across 64 bit extension of AD and C/BE# lines
C/BE#[7:4]	OUT	IN	4 additional C/BE# signals for 64 bit operation

B. The PMC Standard

The PMC standard is a specific implementation of the broader physical form factor standard referred to as a Common Mezzanine Card (CMC), which is defined in [1]. The more specific standard, IEEE 1386.1-2001, specifies the PCI bus as the interconnect standard for the CMC creating the PMC. The mezzanine card was originally specified to create a broad market of interchangeable I/O expansion devices for use in a variety of computing applications. Figure 1 shows how the CMC was originally intended to attach to a host card. Figure 2 shows the physical layout of a CMC, in this case a PMC card.

The PMC standard like PCI allows for either 3.3V or 5V signaling. Some devices are capable of tolerating either voltage. However, for devices that are not tolerant of both voltage standards, a physical key is required to be present to ensure that cards with mismatched voltage levels will not be inserted into the incorrect slot. This ensures that intolerant PMCs or carriers are not damaged [2].

The original PMC specification was written only with PMCs as I/O expansion cards attaching to larger host systems in mind. More recently, due to size reduction, the ability to design complete computing systems in relatively small form factors, and the desire for more distributed computing power, VMEbus International Trade Association (VITA) issued an addition to the PMC standard. This addition allows a Central Processing Unit (CPU) to be on a PMC, which is referred to as a Processor PMC (PrPMC) [4]. The description implied by the terminology of "host card" is somewhat misleading because of the IMPACCT implementation, which uses a PrPMC as the system monarch and general purpose CPU. The carrier provides only basic PCI central resources, power, and system monitoring; it does not contain the host processor. The CPU for the system and the majority of the I/O are provided by the PMCs themselves.

Therefore, the board connecting the I/O PMC to the PrPMC is merely a carrier and is referred to as such.

The PMC standard is widely accepted, and multiple vendors provide COTS PMC solutions for various applications. The physical form factor also provides ruggedization for harsh environments. Within the PMC specification, details are given for conduction-cooled PMC boards as opposed to convection-cooled PMC boards. The conduction-cooled specification mandates certain board features to allow for heat removal from the PCB and electronic devices to the enclosure through metal sinks. This is a much more effective way to remove heat, than convective methods.

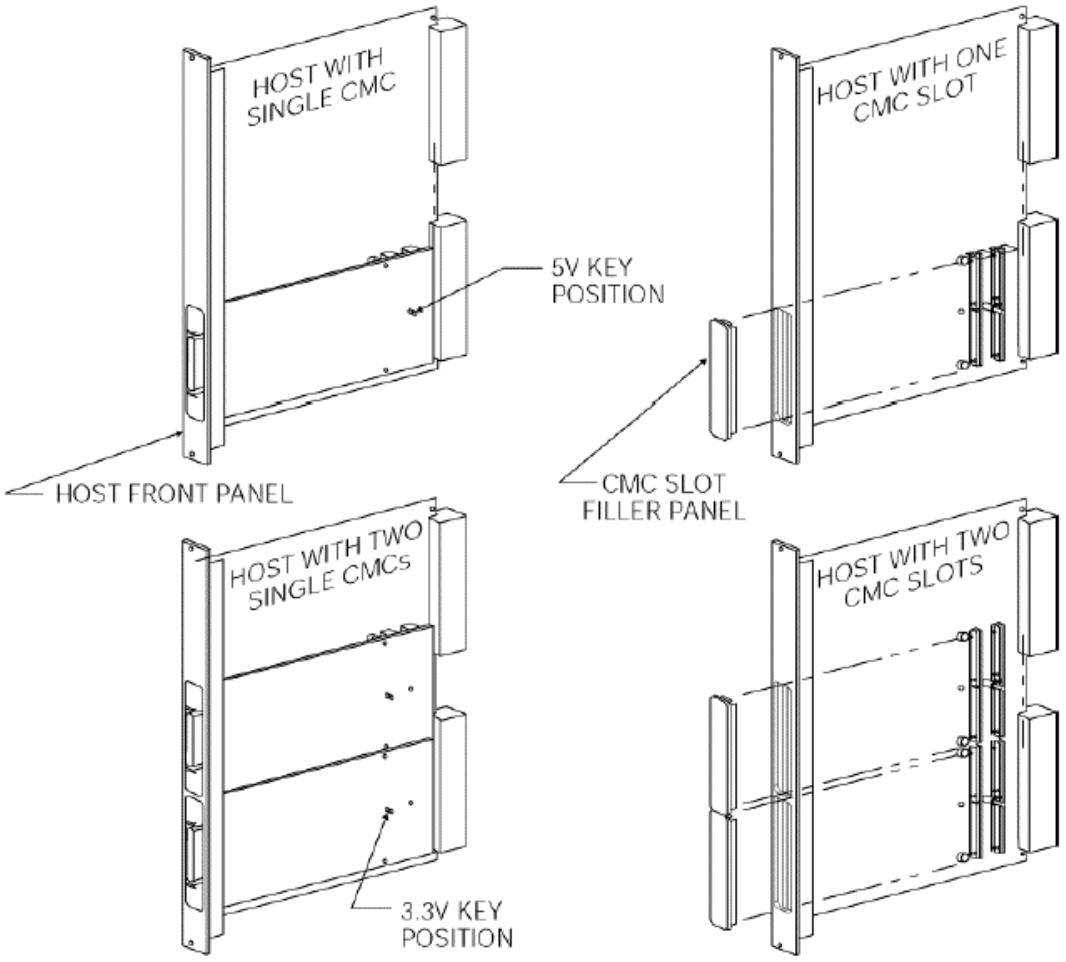

Figure 1. Commun Mezzanine Card mounted on host card [5].

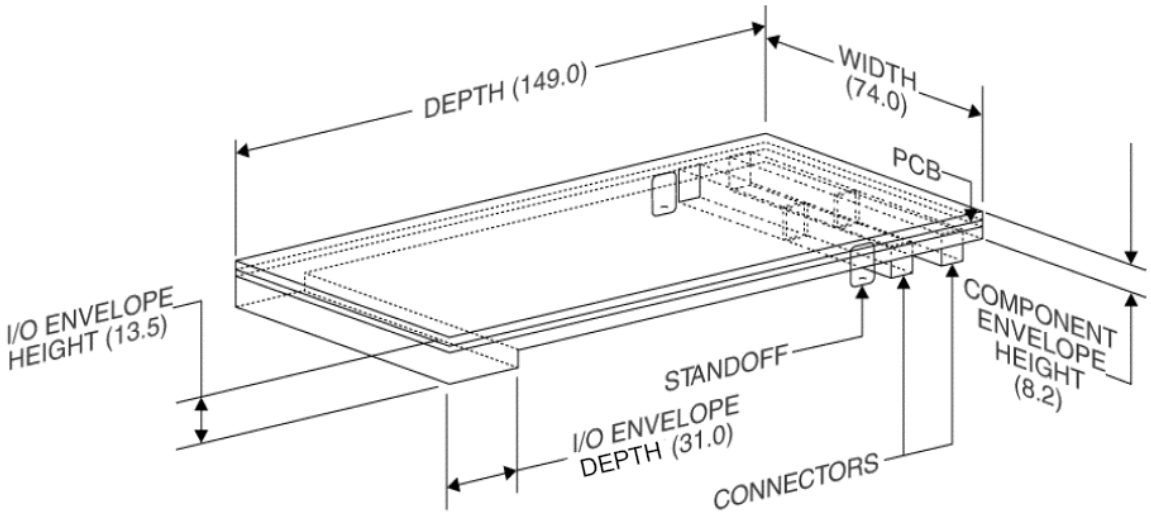

Figure 2. PMC/CMC standard dimensions [1].

C. StarFabric

Stargen's StarFabric is an interconnect technology specifically designed to bridge bus technologies, such as PCI buses, with a serial packet-based switched fabric. This bridging allows a system designer to overcome some of the limitations of a PCI-based architecture, such as bus loading limitations and physical distance. Because it is packet-based fabric, StarFabric also allows quality of service routing. This is where each packet can be given a different priority and routed according to that priority.

As implemented for the purpose of this thesis, the PCI bus is bridged to StarFabric using Stargen's SG2010 ASIC. The serial link is achieved using Low-Voltage Differential Signaling (LVDS) over twisted pair wire, specifically Electronic Industries Alliance/Telecommunications Industry Association's category 5 cable. While StarFabric is a switched fabric interconnect that allows for complex topology, the current implementation of the IMPACCT 2 is a simple point-to-point connection with a transparent serial link for optimal PCI compatibility. This allows for one IMPACCT 2 flight computer configured as a root and populated with a monarch enabled PrPMC to be connected directly to another IMPACCT 2 configured as a leaf without the need for

extra hardware. A StarFabric switch would be required to accommodate more complex topologies.

CHAPTER 3: IMPACCT 1

In the summer of 2004, the first of the new family of flight computers was created. The IMPACCT 1 is a single PMC carrier designed to support a single PrPMC and to interface with the flight platform. The IMPACCT 1 provides power, voltage monitoring, temperature monitoring, and I/O connections for the PrPMC. The design progressed simultaneously on four fronts; KSU's board design was one of the four. First, the design requirements were given by members of Sandia's NGC department, who were responsible for commissioning the design and would be considered the end user. This group had specific requirements and desires for nearly every detail of the design. Second, KSU was the given the task of selecting components and creating schematics for the design which would meet the specified requirements. The schematic was generated using OrCAD schematic capture. Third, the schematic was given to a contractor to layout and fabricate the PCB. Finally, a mechanical engineer in Sandia's flight computer group was responsible for the mounting and enclosure of the PCB. Communication was vital between all groups, as an issue could be propagated to other groups if it was encountered by one group.

This chapter provides a description of how NGC's specifications where interpreted and implemented in the IMPACCT 1. The majority of the interpretation, part selection and design were performed by Kyle McDowell. Jared Simon was a vital part in ordering components and checking the design before fabrication.

Figure 3. IMPACCT 1 in Sandia enclosure next to a 9 inch ruler.

A. Design

A.1 Form Factor and Environment

Volume of internal components must be kept at a minimum for flight applications. Some flight applications require minimum I/O which can be met with a single PrPMC. This is the role of the IMPACCT 1. Designed to support a single PrPMC, the IMPACCT 1 is one of the smallest flight computers used by Sandia.

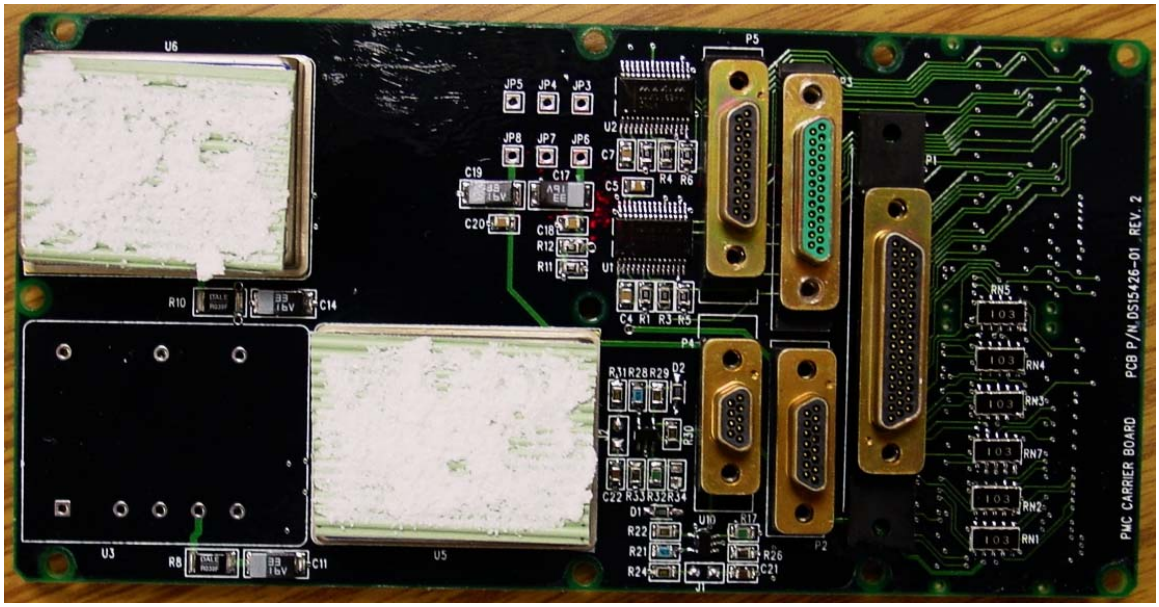

Figure 4. IMPACCT 1 carrier board.

As with any design, there were many constraints when designing the new family of flight computers. For instance, size was a major consideration. The IMPACCT 1 is packaged only slightly larger than the processor PrPMC that it was built around. The PrPMC is conduction-cooled, and the aluminum spacer between the carrier and the PrPMC is machined to touch the processor and other heat generating components. The heat is then dissipated through the enclosure.

The flight qualification process was fairly harsh. The I/O components were required to withstand temperatures ranging from -40C to +85C. Components were mounted securely on the board so that their connections would survive the shock, vibration, and G-loading tests.

A.2 Power

The PrPMC specification requires four voltage supplies; the designer must determine power needs for each voltage is not specified. The main supplies are 3.3V and 5V, while auxiliary supplies mainly used in certain analog I/O card applications are +/-12V. The IMPACCT 1 provides both 3.3V and 5V and leaves the +/-12V for an external 28V supply. The power ratings for the 3.3V and 5V supplies were obtained by meeting the requirements of the specific PrPMC intended for use. The PrPMC required 10W at 5V, the PrPMC did not require a 3.3V supply;

however, the IMPACCT 1 included an 8W 3.3V supply in order to maintain flexibility in carrying latter generations of the PrPMC, which could require the additional voltage.

Keeping with the COTS mentality, a DC-DC converter was chosen to meet the specifications rather than designing a custom switching power supply. A DC-DC converter is preferred when compared to a linear regulator based on the power needed to be supplied and heat issues that would be caused by using a linear regulator. For example, a linear voltage regulator producing 5V from 28V while providing just 1A must dissipate 23W in heat, while a DC-DC converter at 85% efficiency in the same application would waste 0.88W as heat. Finding a linear regulator capable of withstanding such requirements would be difficult and produce too much heat to dissipate within the IMPACCT 1. The IMPACCT 1's DC-DC converter is powered from a 28V system power bus. A matching EMI filter was placed between the DC-DC converter and a 28V bus to prevent the converter from contaminating the 28V supply with high frequency switching noise generated by the converter.

A.3 PCI

The PCI bus is not used in the IMPACCT 1; however, it remains important for PrPMC compatibility reasons that the PCI signals are parked in a legal PCI configuration. Each PCI signal had to be evaluated at the state at which it should be parked to ensure that the PrPMC had a proper environment.

Table 2. IMPACCT 1 PCI Terminations

Signal(s)	Termination
Access/Data and Command	
AD[31:0]	5V
C/BE#[3:0]	5V
Interface Control	
PAR	5V
FRAME#	5V
TRDY#	5V
IRDY#	5V
STOP#	5V
IDSEL	GND
DEVSEL#	5V
Arbitration	

REQ#	5V
GNT#	5V
System	
CLK	33.3MHz Clock
RST#	5V
Error Reporting	
PERR#	5V
SERR#	5V
Interrupt Request	
INTA# - INTD#	5V

A.4 Monitoring

To help diagnose problems during flight, some of the operating conditions of the flight computer are monitored. The IMPACCT 1 provides the means to monitor voltage levels used to power the flight computer, current consumption, and two temperature probes.

A.4.1 Voltage Monitoring

To help determine the condition of the flight computer the major supply voltages 3.3, 5, +12V are monitored by an external telemetry unit. This unit accepts 0 to 5V inputs encodes the analog signal and transmits the information to launch facilities for monitoring. A simple voltage divider is used to scale down both the 5V and +12V supplies to detect over voltage conditions without saturating the telemetry units 0 to 5V analog inputs.

A.4.2 Current Monitoring

The current being sourced from the 5V and 3.3V converters are monitored by measuring the voltage across two parallel resistors in series with the current path. Two resistors are used in parallel to achieve low resistance and to allow the current to be split between two loads, reducing the power rating needed for a single resistor. The voltage across the resistors is amplified by a MAX4073 for a reading of 1.0V/A, which is then output through a Micro-D Connector to the telemetry unit.

A.4.3 Temperature Monitoring

Two probes based on Analog Devices'AD590 are used to attach to the processor and case to monitor the flight computer's operating temperatures. The AD590s generate current based on temperature 1uA/K and are laser trimmed and calibrated to 298.2uA at 298.2K. Current sensors are more immune to noise issues than are voltage sensors. The current is converted to a 0 to 5V signal by a single op-amp circuit where the 70F-180F reads as 0-5V approximately. This output is also fed through a MICRO-D Connector to input into the telemetry unit.

A.5 Input/Output

The IMPACCT 1 provides no additional I/O other than what the PrPMC has on board. The IMPACCT 1 merely routes the I/O from the PrPMC to MICRO-D Connector for connection to the outside world. However, the IMPACCT 1 does provide a means to convert two RS232 channels on the PrPMC to the more commonly used (in flight computers) RS422. This is accomplished by means of two MAX3162 chips.

The I/O connections are good examples of the IMPACCT 1 being based on a specific COTS PrPMC. While minimal changes need to be implemented for a new or alternative COTS PrPMC, changes in the IMPACCT 1 carrier must occur nonetheless.

B. Testing

B.1 Initial Testing

Testing of the first version of the IMPACCT 1 consisted of two phases. The first phase was carried out by KSU and consisted of the construction of a prototype and verification that the power components and monitoring circuits were correct. It was at this point an error was determined to be present in the selected resistor values for the temperature monitoring circuit. The PMC connection was verified to ensure that all signals were as expected. This was achieved by probing the board at various connections with an oscilloscope and verifying the signals present were compatible with the PMC specification.

Second, KSU installed the PrPMC and applied power to verify that it functioned when connected to the IMPACCT 1 and that the PCI termination was accurate. Having the PrPMC boot correctly was almost a sure sign the carrier functioned as desired. The prototype was passed on to Sandia for further testing.

B.2 Environmental Testing

Environmental testing was performed at Sandia by their engineering staff and to their specifications for flight qualified hardware. The details of the testing are purposefully omitted. However, while the details are not divulged, the IMPACCT 1 passed the following tests: heat cycling, shock, vibration, and G-loading.

C. IMPACCT 1 Summary

The IMPACCT 1 was later revised by Sandia to fix a problem with the temperature monitoring circuit and to address mechanical issues in the PCB layout for mounting in its enclosure. However, KSU's contribution in the design remained unchanged. This second revision of IMPACCT 1 is scheduled for first flight in the fall of 2005. Sandia's NGC group was pleased with the IMPACCT 1 and has viewed the project as a success.

CHAPTER 4: IMPACCT 2

The IMPACCT 2 expands on the idea of the IMPACCT 1 and offers an important addition to the feature set: expandability. There are applications that demand more I/O and processing than the IMPACCT 1 can provide, and IMPACCT 2 meets these demands.

The IMPACCT 2 was created through a process similar to the IMPACCT 1. Again, NGC provided requirements; KSU designed a system to meet those requirements. The mechanical enclosure design and board layout were performed by other groups.

The following chapter provides a description of how NGC's requirements were met in the implementation of the IMPACCT 2. Unlike the IMPACCT 1, more research had to be performed in various technologies to meet the requirements set forth by NGC. Also, a greater understanding of the PCI bus was needed to validate the system and to ensure its correctness. The research and design tasks for IMPACCT 2's implementation to meet NGC's requirements were performed by Kyle McDowell of KSU.

A. Design

A.1 Form Factor

Space remains a significant concern for the IMPACCT 2. The new design retains a width and length that are very close to those of the IMPACCT 1. This allows the IMPACCT 1 and IMPACCT 2 to have the same bolt pattern for mounting, allowing easy interchanges to be made between the two flight computers. The additional volume required by the added functionality of IMPACCT 2 is achieved by expanding the height dimension. Within the enclosure, the IMPACCT 2 is divided into four boards: two COTS PMCs, a PCB designed to carry the two PMCs and to provide a link for serial PCI bus expansion, and a board responsible for power and I/O connectors.

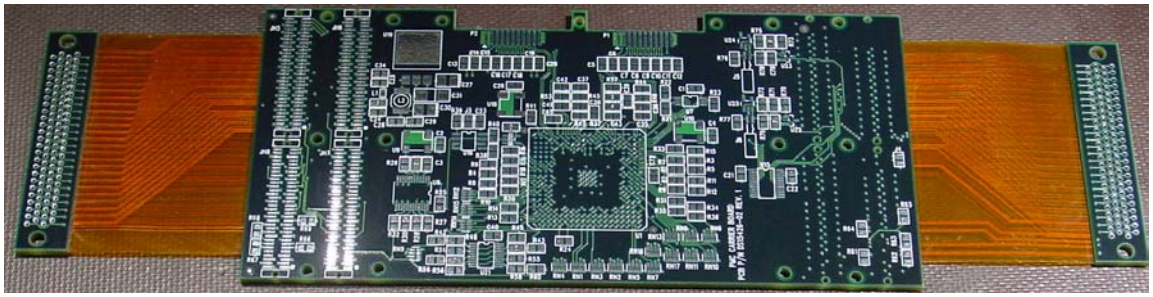

Figure 5. Carrier board for IMPACCT 2.

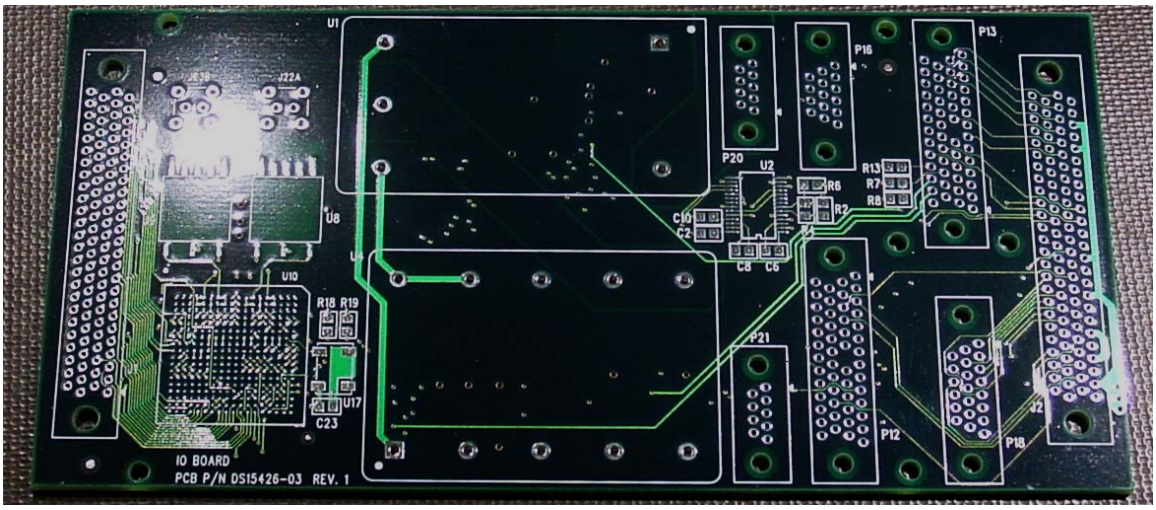

Figure 6. Top connector and power board for IMPACCT 2.

A unique approach was used in KSU's design to connect the carrier and power board within the IMPACCT 2. The boards are connected by flexible PCB. The carrier board on both ends contains a section of flexible PCB material that allows the board to fold up and back to connect to the top power board. This method requires less volume than using traditional connectors.

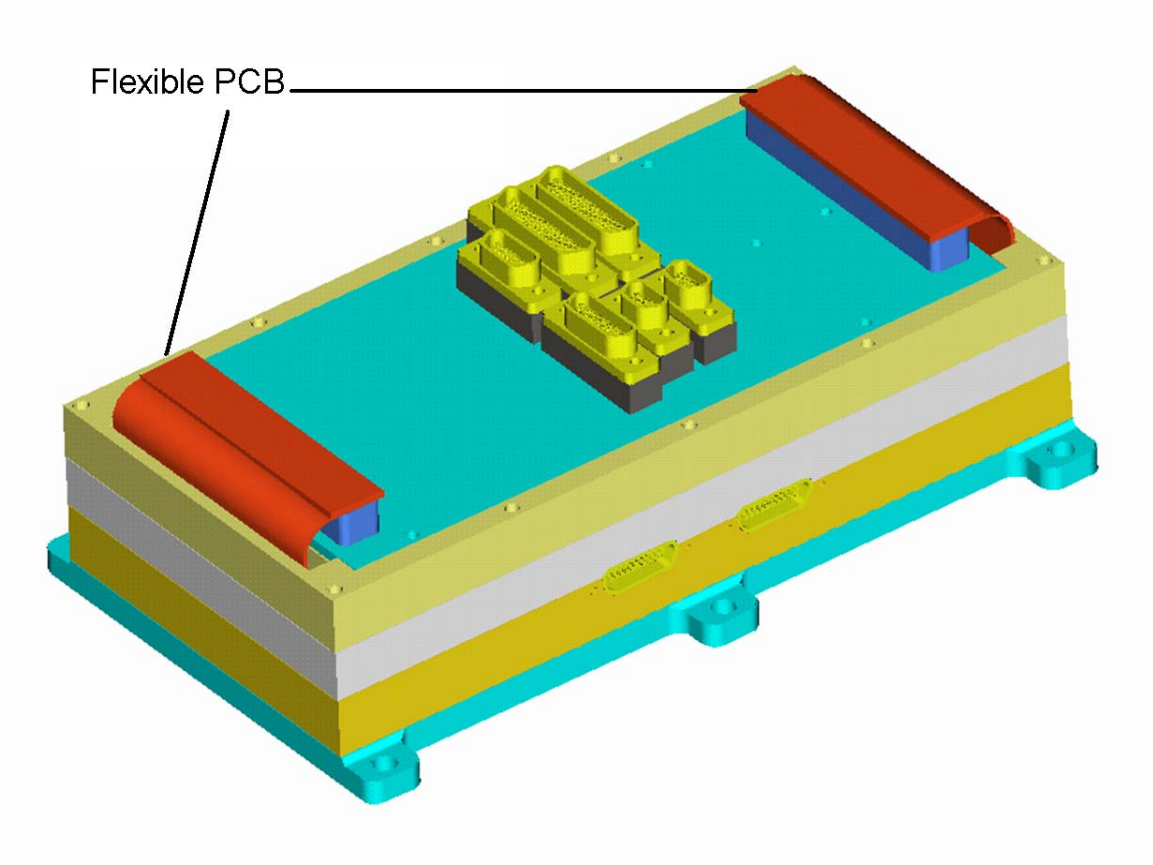

Figure 7. Flexible PCB connects the carrier board to the top borad.

The carrier board is designed to support slot one as either a monarch, which is the PCI device responsible for bus initialization, or as a standard master/target PMC slot. Slot 2 does not have the appropriate signals on the PMC connector to support a monarch.

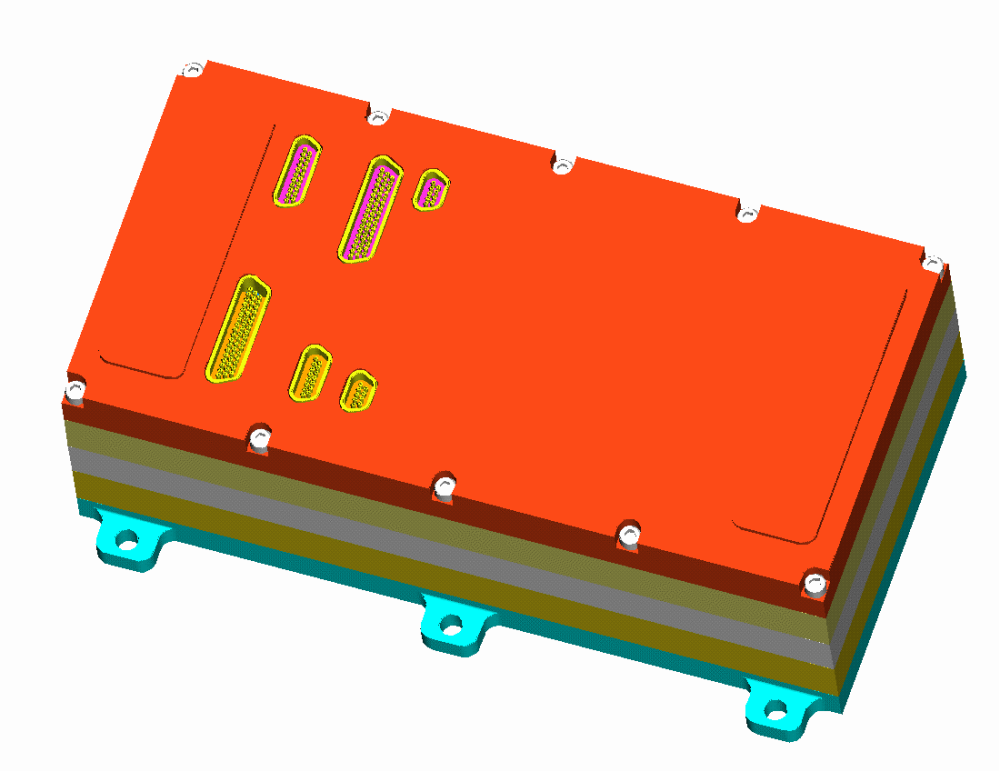

Figure 8. Assembled rendering of IMPACCT 2.

A.2 Power

Powering the IMPACCT 2 is achieved in a fashion similar to powering the IMPACCT 1. However, due to the added PMC card and support circuitry for PCI expansion, more power and the +/-12V supplies are now required. No single DC-DC converter met all voltage and power requirements for the IMPACCT 2. Rather, a DC-DC converter in conjunction with voltages regulators provides the necessary power. The converter supplies 5V at 20W and +/-12V at a total of 10W. The high power 5V supply not only powers 5V devices, but is used to derive additional voltages using linear regulators at 3.3V and 1.5V. The SG2010 ASIC responsible for PCI to StarFabric requires its 3.3V and 1.5V supplies to be exceptionally clean for various on-chip functions. A low-pass filter using inductors and capacitors is used to reduce high-frequency noise at the 1.5V supply.

PCB placement and the use of power and ground planes are crucial to the effectiveness of the power filtering scheme. Communication of these special layout requirements between KSU and the layout engineer were extremely important to ensure that the design functioned correctly.

A.3 PCI with StarFabric Expansion

Unlike on the IMPACCT 1, the PCI bus is a critical part of the IMPACCT 2 design, and a considerable amount of time went into its implementation. At the heart of the PCI bus design is the SG2010, which provides bus arbitration and PCI bridging to the StarFabric interconnect. Other technologies where considered, but StarFabric's specification and immediate availability solidified its selection for the IMPACCT 2.

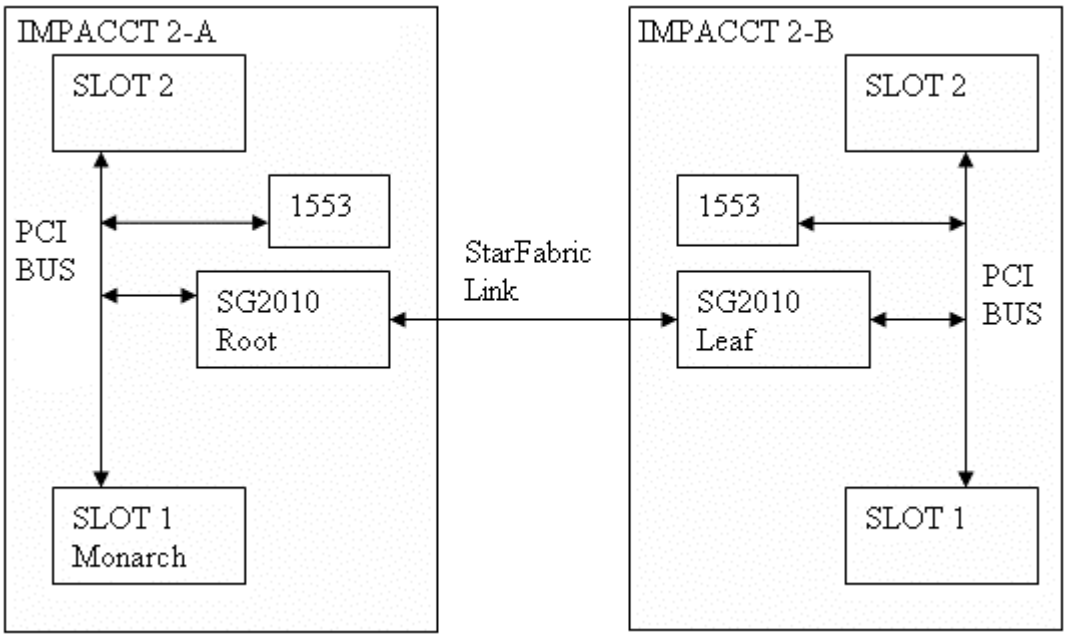

Figure 9. System diagram showing two IMPACCT 2 fligh computers connected with StarFabric.

A.3.1 StarFabric vs. PCI Express

One of the alternatives to StarFabric is extremely attractive both technically and aesthetically, and is worth mentioning. Currently, in the desktop computing and communications industries conventional PCI has reached its scalable limit and is being replaced by the next generation of I/O interconnect called PCI Express. Deigned from the ground up to be compatible with PCI from a software standpoint, PCI Express has a totally different approach to the physical layer of its implementation. PCI Express contains 1-32 links of a high-speed differential signaling in order to achieve an effective data bandwidth for 32-bit addressing of approximately 210.5MB/s

to 6736.8MB/s given that the data bytes payload per packet are 128. The serial links are switchable, enabling quality of service routing and can be cabled over several meters. This solution for PCI expansion was extremely attractive, but due to time constraints and product availability, StarFabric was chosen over PCI Express [7].

A.3.2 Extended temperature considerations

By default, the SG2010 functions in the 0 to 70C temperate range. To extend the temperature range to the desired -40 to 85C an extra clock must be provided with tight timing specifications. Normally the SG2010 needs only a single clock at 62.208Mhz to provide clocking for both clock data recovery from the serial link and to provide clocking for internal logic. However, in the extended temperature range the phase lock loop used to derive 78Mhz for internal logic is not guaranteed to function correctly. A work-around exists using strapping pins to configure the SG2010 to accept an external clock at 77.76Mhz with 150ps max peak-to-peak jitter and a duty cycle of 45/55% min/max for internal logic clocking [5].

A.3.3 PCI clock

In order for the PCI bus to function properly, all devices on the bus must receive the 33Mhz PCI clock signal at virtually the same time. This concept is also known as low clock skew. The PCI specification for skew on a 33Mhz system is 2ns. It is undesirable to overload the driver by connecting all clock lines to a single oscillator output; rather, a clock driver is used. The clock driver accepts a single oscillator input and drives ten clocks out with a skew of 0.6ns max between each output. The low impedance of the clock driver allows each clock line to be terminated in order to achieve a cleaner clock by reducing ringing and sharpening transitions [3]. Again, communication between the circuit designer and board designer were important to ensure similar electrical length between clock lines was maintained during layout to keep skew within the 2ns limit.

A.3.4 IDSEL Signals

At system power-on, PCI devices have not yet been mapped into the CPUs address space. Instead, the configuration space on each PCI device only contains information on which

resources the PCI device will need for operation. It is the job of the system monarch to select each device, read configuration space, allocate the requested nonconflicting resources, and write back the allocated resources into configuration space. Future accesses to the device usually take place as memory or I/O space reading and writing. However, the initial access before the device is mapped into memory requires the use of the IDSEL line. Each PCI device has its own separate IDSEL line unlike all other signals on the PCI bus that can be shared (even interrupts can be shared). In the IMPACCT 2 implementation, as with most other systems, each IDSEL line is mapped to one of the uppermost 21-bits of the address/data lines. That is to say the monarch sets only one bit on AD[31:11] when AD[1::0] is [0::0] to access a single device's configuration space.

A.3.5 SG2010 operating mode

The SG2010 is capable of several configurations. Currently, the IMPACCT 2 is designed to function in only two of the three basic modes. There is a desire for the expansion of the PCI bus to be as transparent as possible when the IMPACCT 2 is connected point-to-point with another IMPACCT 2. The serial link should be viewed from the PCI bus as being separated by a traditional PCI-to-PCI bridge, instead of a PCI-to-StarFabric gateway. This is achieved by soldering strapping resistors in a configuration on the monarch populated IMPACCT 2, where the PCI bus of the monarch is considered the primary bus so that the SG2010 is in root mode with the bridge function enabled. Root mode is Stargen terminology for the StarFabric node which contains the host or monarch CPU. On the opposite side of the StarFabric link, the SG2010 is strapped to be in leaf mode with bridge enabled. Leaf mode refers to a StarFabric node in which the PCI bus connects only PCI masters and targets. This root and leaf configuration allows the PCI configuration accesses to be forwarded from the monarch over StarFabric to PCI targets and masters for initialization.

A.3.6 High-speed serial link

StarFabric uses multiple high-speed LVDS links that conform to IEEE 1596.3 for the physical layer of the interconnects. Each pair is capable of transmit rates of 622Mbps. A StarFabric connection using the SG2010 has two links, consisting of four transmit pairs for each link and two links consisting or four receive pairs in each link. The overall connection is redundant as

only one receive link and one transmit link are needed. The SG2010 is properly terminated with an internal 100 Ohm resistor for the correct signaling voltage of 400mV across the differential pair. For robustness, the IMPACCT 2 uses AC coupling to protect the SG2010 from differences in ground potential when connected via a category 5 cable. AC coupling requires the addition of a receiver reference to recover a DC reference for the differential pair.

Given the high speed and the low-voltage swing of LVDS, special steps are taken to ensure that signal integrity is maintained. First, skew between the positive and negative signals of each LVDS pair is 25ps max. Second, the skew between any given pair in a link is no more than 300ps. Third, the LVDS signals are routed on the top and bottom layers of the eight-layer printed circuit board in a microstrip fashion to ensure the specified impedance of 50 Ohm or 100 Ohm differential +/-5%. The LVDS routing also is spaced at least 30 mils from other digital logic to prevent cross-talk. Figure 4 shows the microstrip configuration where W equals 8 mils and S is 1-3 mils given 5 mils of FR4 between signal and ground plane [5].

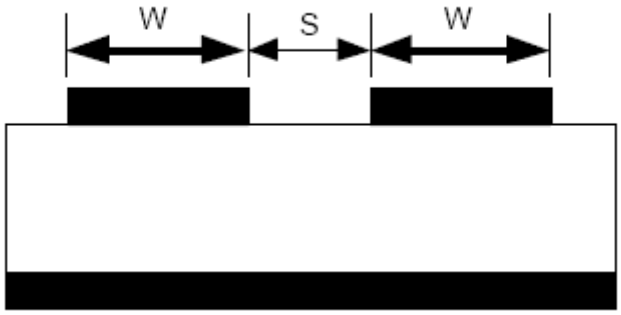

Figure 10. Microstrip configuration for 100 Ohm Differential Pair [5].

Communication was important not only between the board designer and circuit designer to meet design requirements on the board level, but also between circuit designer and technical staff. The technical staff was responsible for creating cables for connecting StarFabric devices. Given the high-speed signaling of the serial connect quality, cables consisting of four copper twisted pairs with an impedance of 100 Ohms are needed for reliable connection.

A.3.7 SG2010 PCI interrupt filter

Interrupts are an important part of the functioning of many PCI devices, and special care must be taken for the SG2010 to detect and forward interrupts properly in leaf mode. Almost hidden in the documentation is information that interrupts must transition within four PCI clock cycles in order for the SG2010 to cleanly detect the interrupt. While it seemed unlikely that the assertion of an interrupt would take longer than four PCI clock cycles, caution was exercised by inserting a flip-flop filter to insure quick transitions occur at the SG2010 interrupt input pins.

A.5 Input/Output

As with the IMPACCT 1, the majority of the I/O is provided by the PMCs. Again, the PrPMC specific RS232 conversion to RS422 conversion is achieved by two MAX3162 chips. However, the SG2010 provides an additional four general-purpose I/O pins. Rather than waste these pins by leaving them unconnected, the pins' 3.3V signals are level shifted through a Texas Instrument 74LVC8T245 to more usable 5V signaling, and are brought out through the Micro-D connectors to the outside world.

Late in the design of the IMPACCT 2 NGC requested that a MIL-STD 1553 interface be provide on the IMPACCT 2 because of a mission specific application. After several discussions with NGC, an IC capable of residing on the PCI bus and providing two 1553 connections was selected for use. It was decided that the IC would be placed on the top connector board due to space limitations on the carrier. Another attractive feature of mounting the IC and routing PCI signals to the top board was that for other mission specific applications only the top board would need to be revised. The IC could be removed or replaced with an FPGA to meet mission specific I/O requirements.

B. Testing and Future Revision

Due to part availability and time constraints, only the carrier portion of the IMPACCT 2 was tested. The carrier board represents the majority of functionality of the IMPACCT 2.

B.1 Initial Testing

Initial testing of the IMPACCT 2 was very discouraging. After receiving the PCB from the manufacturer and populating the board at Sandia, initial testing produced a nonworking system. Visual inspections and board probing revealed no errors. However, when the PrPMC was placed on the carrier the PrPMC failed to boot. After several days of debugging the power-on-reset circuit was diagnosed as the culprit for the PrPMC not booting.

Unfortunately, after the power-on-reset circuit was by-passed and the PrPMC could boot the StarFabric and PCI bus connections were not functioning correctly.

A Stargen, StarFabric, PCI card containing an SG2010 was connected to a PC. This card allowed the StarFabric and PCI bus functionality to be evaluated quickly. The PC is a great example of a host system that must be PCI compliant and therefore provides a quick solution for initial testing. With the StarFabric PCI card and IMPACCT 2 carrier configured properly, the StarFabric link should be transparent, and both SG2010 should work as a PCI to PCI bridge. However, the first several test failed when trying to connect the IMPACCT 2 to the PC. The board was probed to verify intended signals were present and the intentions where check against documentation to verify proper interpretation for the design. No errors where found. However, after careful reconnection with the StarFabric PCI card the link worked. The conclusion reached was that the cable and/or the power supply in the first non-functioning trials must have been miswired.

After the StarFabric link began functioning the IMPACCT 2 carrier was populated with I/O cards. The carrier's PCI bus was tested with the PC through the StarFabric link. During the PC boot process all PCI devices are initialized. In this case the PC initialized not only the local devices, but the devices on the other side of the StraFabric bridge on the IMPACCT 2 were initialized. A PCI to PCI bridge had been created by the StarFabric PCI card's SG2010 and IMPACCT 2's SG2010. Commercial software running on the PC was used to verify the IMPACCT 2's I/O PMC cards where present and configured properly. This verified that the StarFabric link and PCI bus on the IMPACCT 2 were indeed functioning correctly.

B.2 Future Testing

Due to time constraints, only a very shallow testing of the IMPACCT 2 was performed for this thesis. While this testing does seem to reveal that the major components function correctly there is still much more testing that should be carried out to verify the that the design is sufficient for flight hardware. That work will be continued at Sandia.

First, another IMPACCT 2 configured as a root device should be built in order to replace the PC as the PCI monarch, as in the previous test setup. This would verify that the PrPMC running the desired real-time operating system can perform the necessary monarch functions across the StarFabric link. Next, bandwidth testing across the StarFabric link should be conducted to verify StarFabric's bandwidth is adequate and latency is low enough to operate in a real-time environment. After these functional tests the standard flight qualification with environmental testing should be executed to ensure the steps taken to operate in a harsh environment were sufficient.

B.3 Testing and Design Revision

Given no major issues in the flight qualification process the IMPACCT 2 should be ready to fly in its desired applications in a form very close to the one presented in this thesis. Testing has revealed an issue with the power-on-reset circuit which should not be too difficult to repair, and will not affect other systems on the IMPACCT 2. As in all designs, part availability and changing applications will drive future revisions. However, given the enthusiasm for the architecture in it current state and its inherent flexibility, revisions should be minor while providing a long service life.

CHAPTER 5: FUTURE WORK

A. Reconfigurable I/O

At various stages in development for both the IMPACCT 1 and IMPACCT 2, the idea of including a Field Programmable Gate Array on the carrier arose. The main reason for its inclusion is the ability to reconfigure the FPGA to perform various I/O tasks for a given mission. However, several drawbacks were presented which kept the FPGA out of both of the IMPACCT flight computers. First, flight computers are subjected to higher than normal levels of radiation. KSU raised concern for the susceptibility of FPGA's SRAM to radiation induced upsets and their potential for cause of functional failure. Second, even though the FPGA is easily reconfigurable, the support circuitry must be redesigned in order to support the changing I/O. Third, the desired timeline from design to flight qualified hardware was tight, and no immediate need for the FPGA was presented. Therefore, the unneeded hardware was omitted from the design. Future work could address these issues and include an FPGA to take on the functionality of the SG2010, providing reconfigurable I/O and even allowing more processing power with on-board PowerPC processors or soft-core processors. These features will no doubt have application in the future as more is demanded from flight hardware.

B. PCI Express and StarFabric

While StarFabric meets the requirements given to the IMPACCT 2, it is not as widely accepted as the PCI Express interconnect, which is gaining popularity everyday. New solutions, in the form of intellectual property cores for FPGAs and ASICs for PCI to PCI Express bridging, are now becoming available. While PCI Express could not be included in the first version of IMPACCT 2, PCI Express expansion could become an important upgrade.

C. Architecture

Finally, the requirement of PCI expansion remains in question. Traditionally, Sandia's NGC group has approached software development in a shared memory method, where different sections of software share information by means of a common global declared variables. It is no doubt that this is why PCI was chosen to interface to I/O. However, information should be exchanged in the more modern method of limiting shared memory and by passing information

through messaging. This type of architecture improves code reuse and robustness. Other cheaper and easier interconnects could then be applied, such as Controller Area Network, Ethernet, USB, and Firewire to name only a few. This requires a paradigm shift from the NGC group, however, and because NGC commissioned the design, it remains only a suggestion.

CHAPTER 6: CONCLUSIONS

Facing the task of creating a new flight computer, Sandia National Laboratories invited Kansas State University to participate in the creation of such a flight computer. The IMPACCT 1 and IMPACCT 2 are the products of that invitation and represent input from many individuals and groups.

The design of the IMPACCT 1 and IMPACCT 2 proved to be an economical and timely solution when compared to a proprietary flight computer. Also, the use of COTS components allows for feature updates to occur often, quickly, and cheaply.

Research is on-going at Kansas State University for Sandia National Laboratories in the quest for new technologies in flight hardware.

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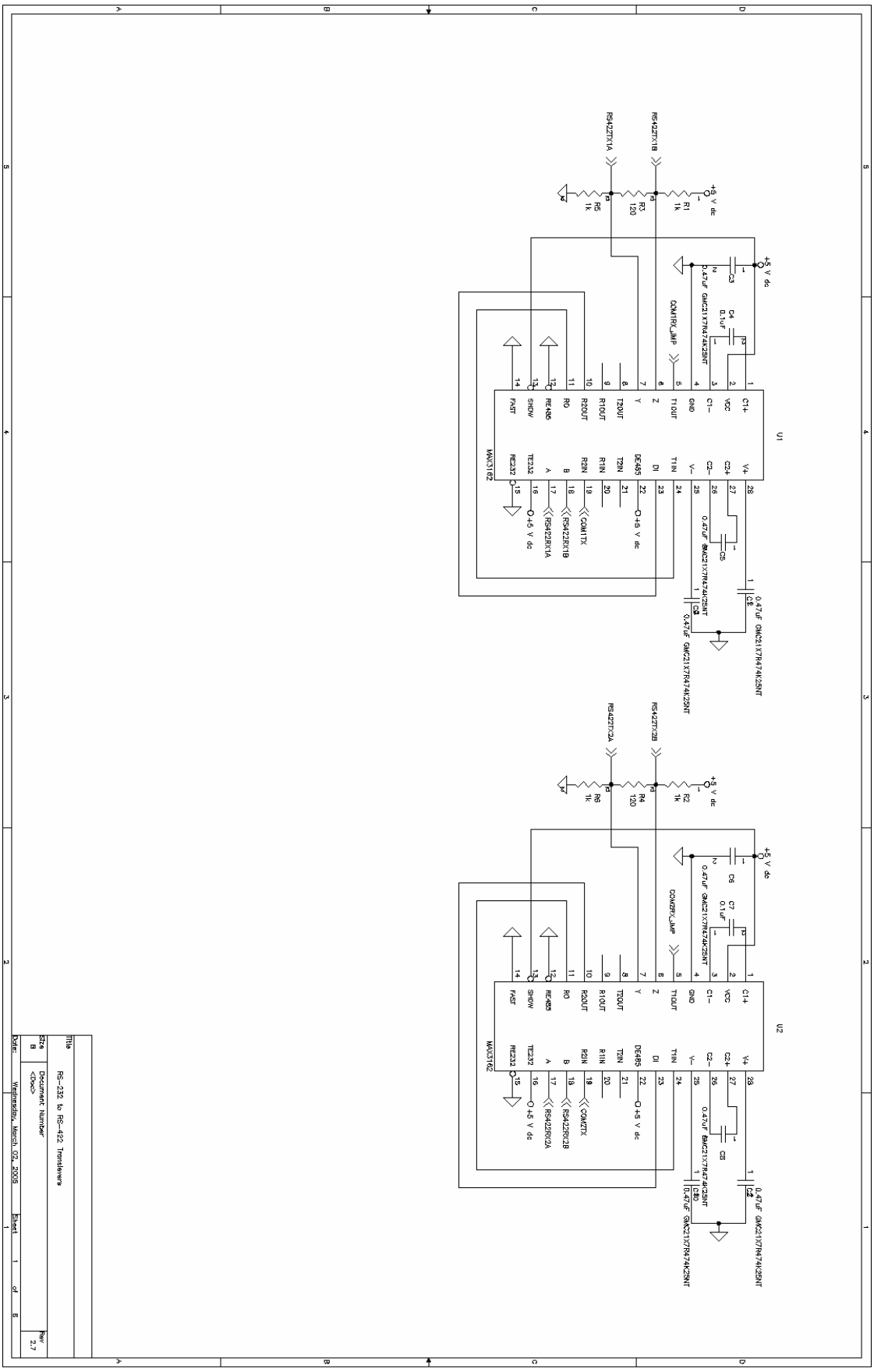
APPENDIX A : IMPACCT 1 SCHEMATICS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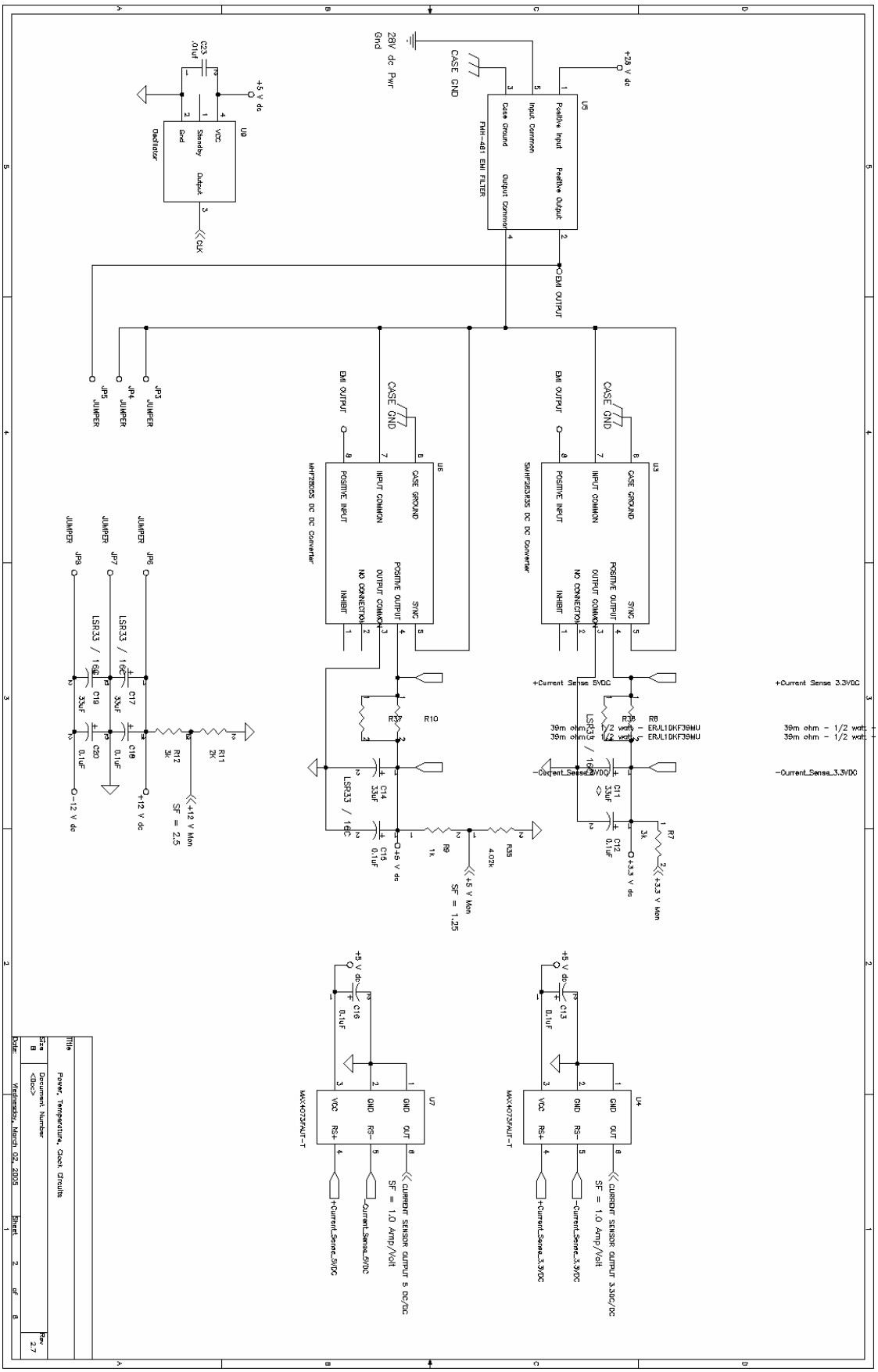
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U5
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Input Common
Case Ground
Output Common
Positive Output
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C23 .01uF
+5 V dc
U8
Oscillator
Vcc
Stand-by
Gnd
Output
CLK
JP5 JUMPER
JP4 JUMPER
JP3 JUMPER
EMI OUTPUT
CASE GND
U3
CASE GROUND
INPUT COMMON
POSITIVE INPUT
OUTPUT COMMON
NO CONNECTION
POSITIVE OUTPUT
SYNC
INHIBIT
SMHF28S05S DC DC Converter
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-Current_Sense_5VDC
R8
39m ohm - 1/2 watt - ER/L1DKF39MU
LSR33 / 1GC
C11 33uF
C12 0.1uF
R7 3k
+3.3 V dc
+3.3 V Mon
+Current Sense 3.3VDC
-Current_Sense_3.3VDC
U6
MHF28S05 DC DC Converter
R10
R9 1k
R35 4.02k
C14 33uF
C16 0.1uF
+5 V dc
+5 V Mon
SF = 1.25
JUMPER JP8
JUMPER JP7
JUMPER JP6
LSR33 / 1GC
C18 33uF
C17 33uF
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R11 2K
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+12 V Mon
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U7
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VCC
RS+
RS-
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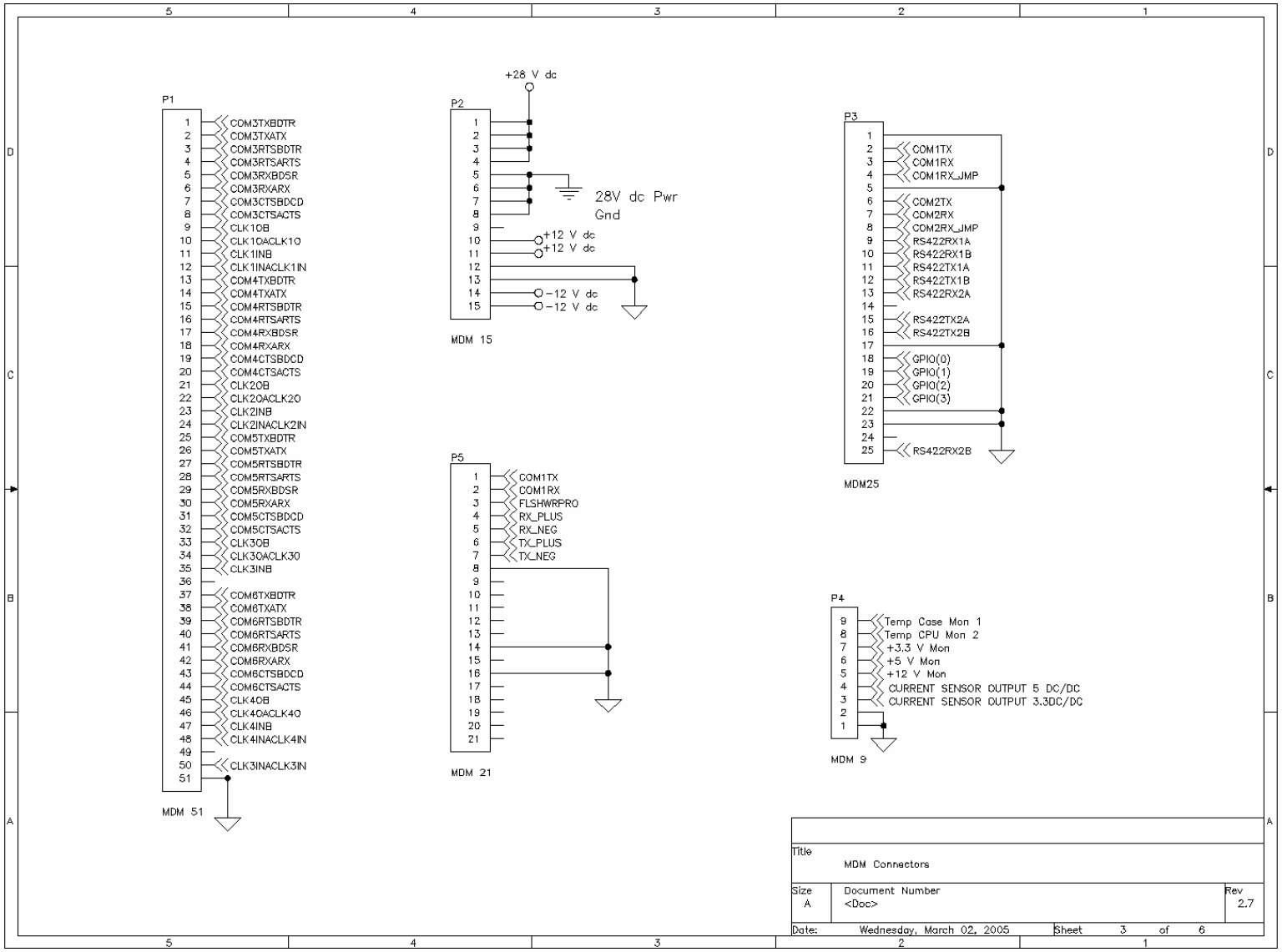
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15
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Gnd
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+12 V dc
−12 V dc
−12 V dc
MDM 15
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6 COM2TX
7 COM2RX
8 COM2RX_JMP
9 RS422RX1A
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2 COM1RX
3 FLSHWRPRO
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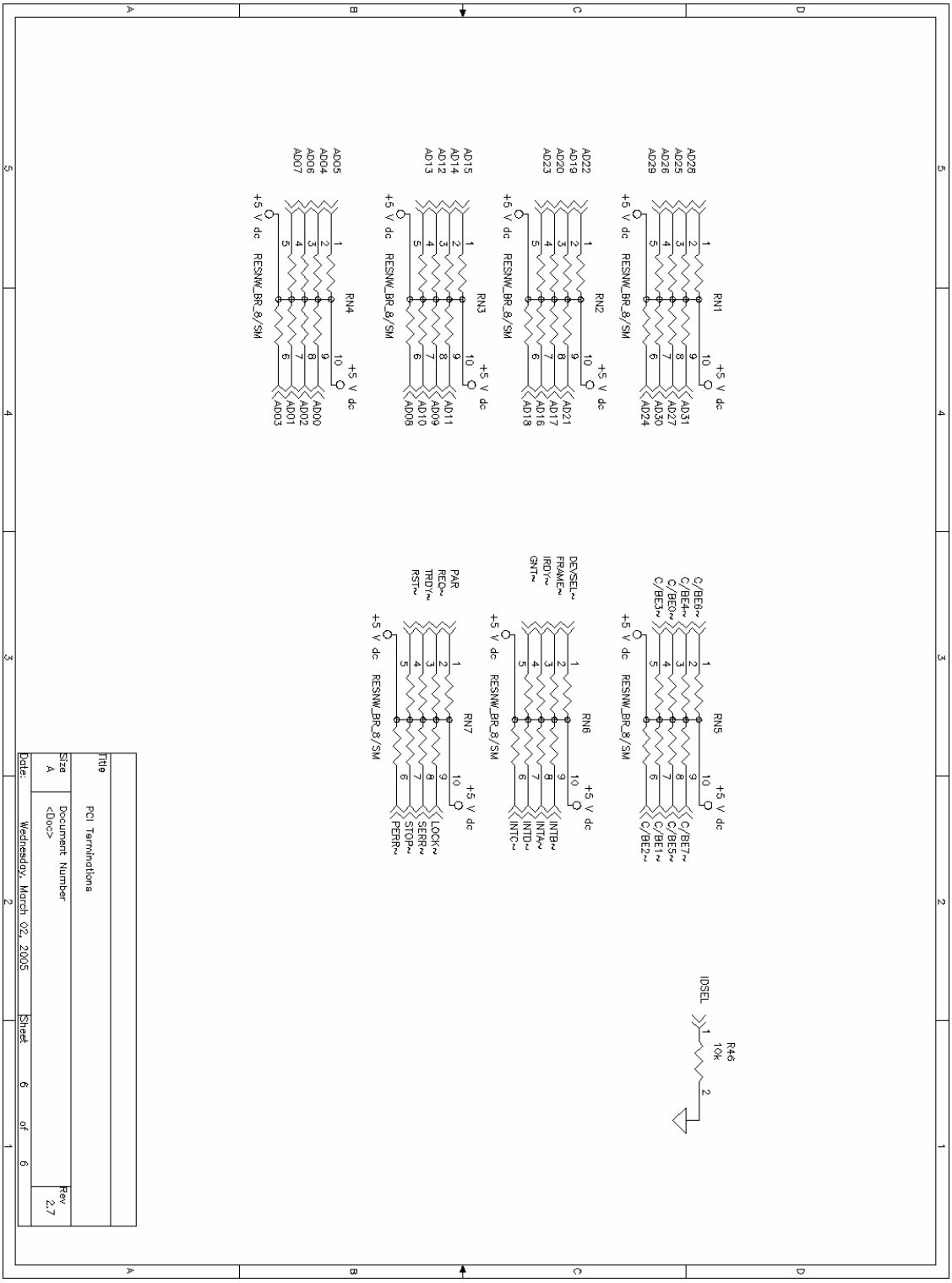
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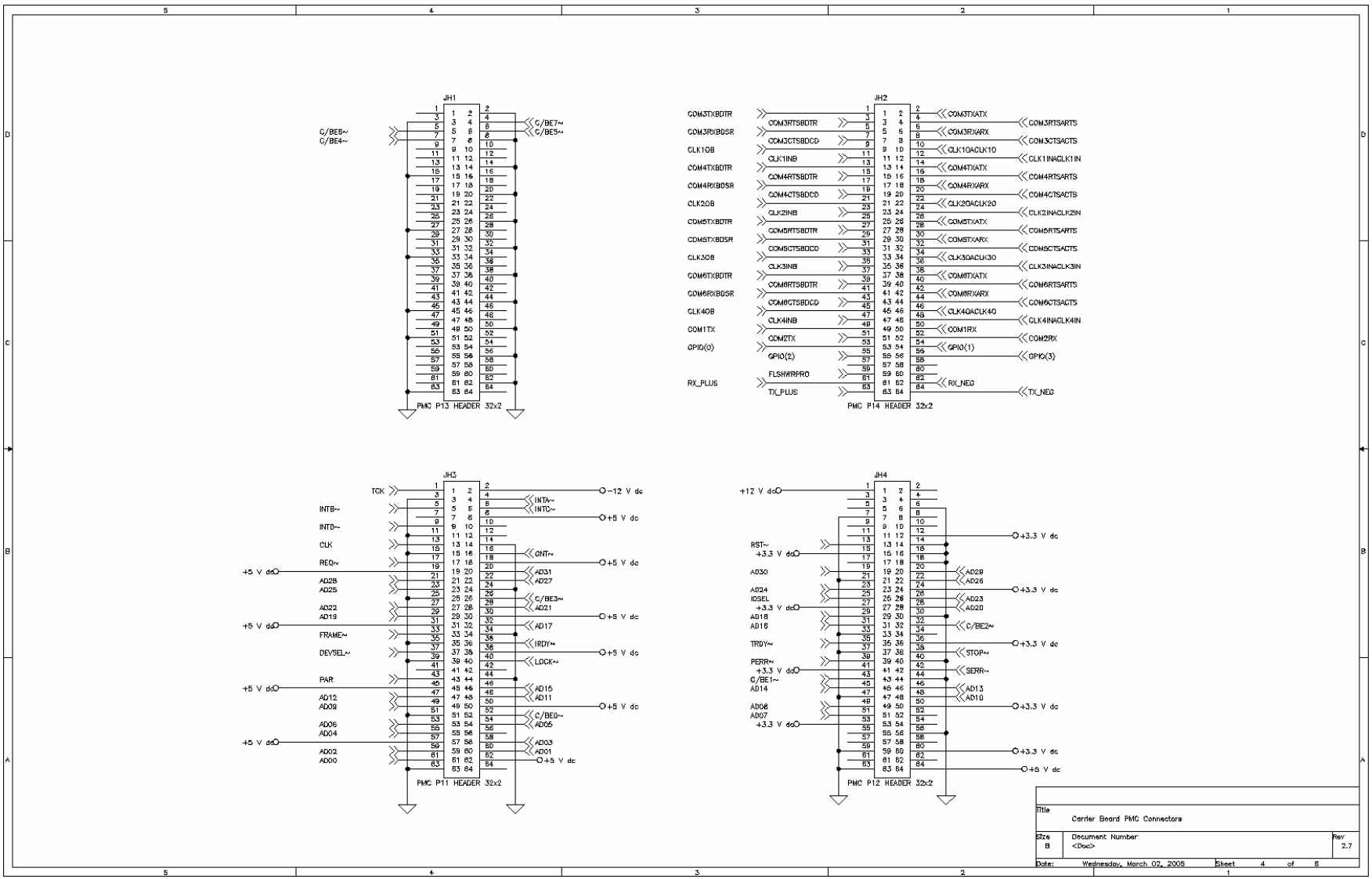
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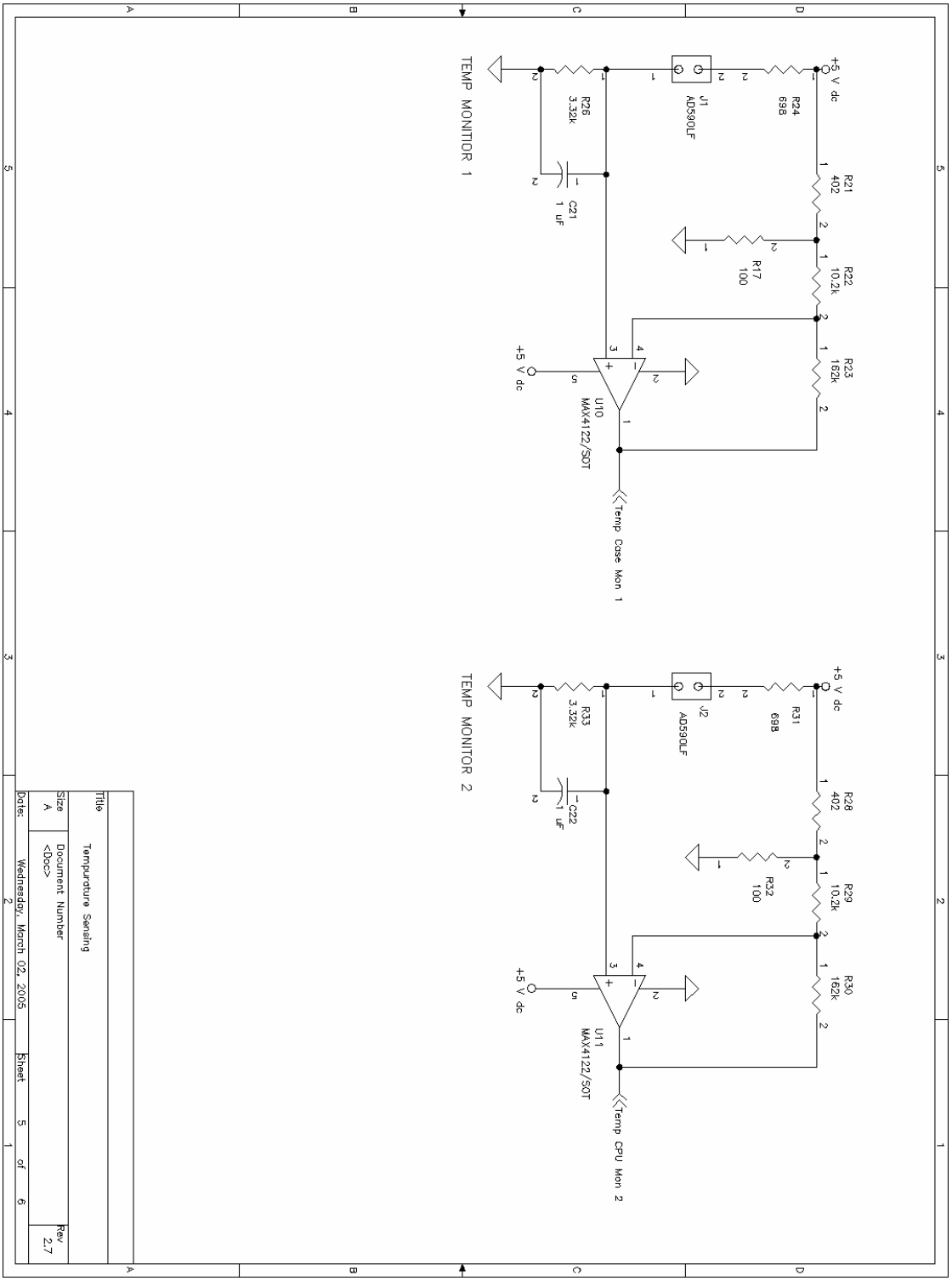
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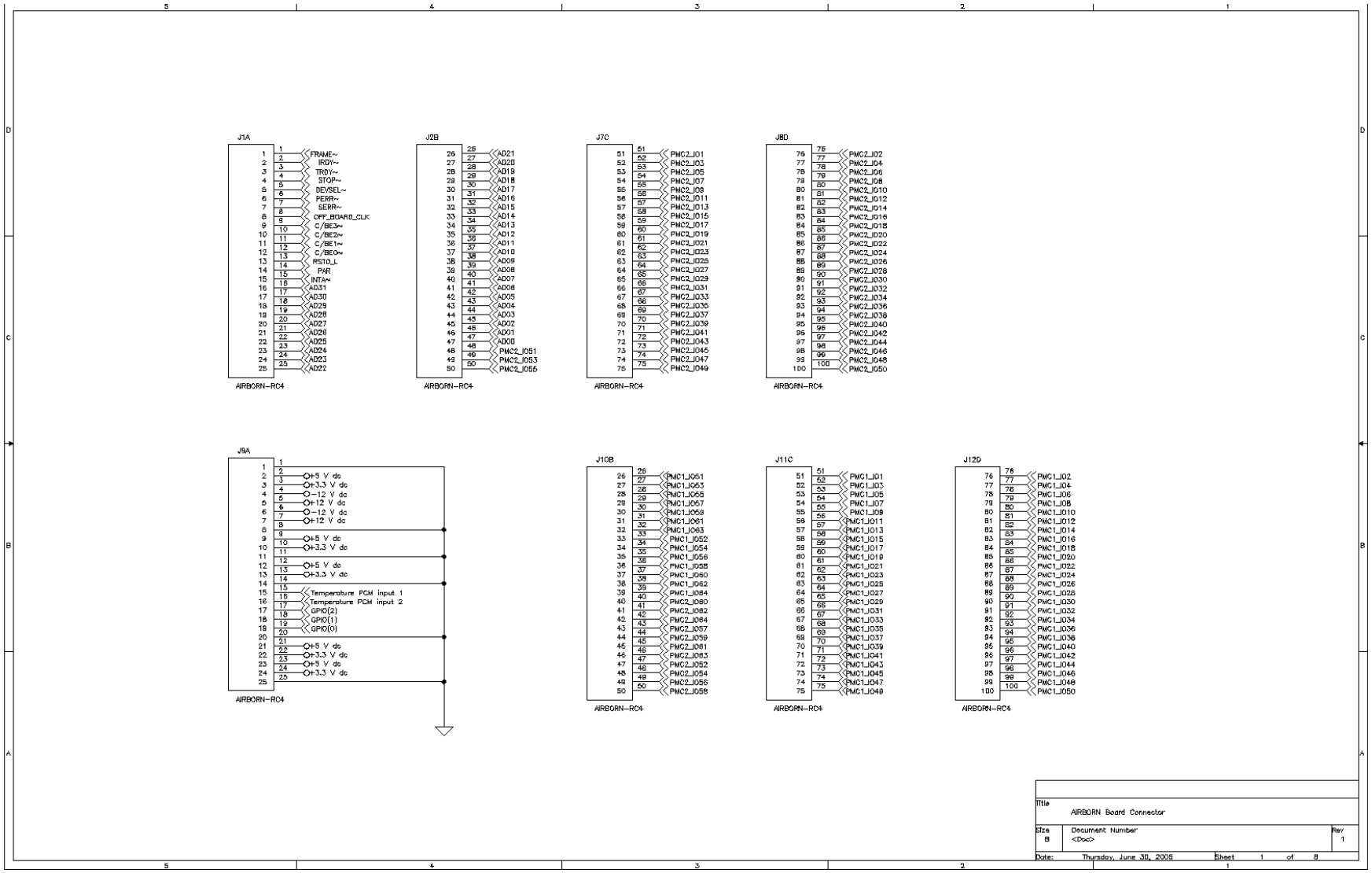
AD590LF
R24
698
R21
402
R22
10.2k
R17
100
R23
162k
R26
3.32k
C21
1 uF
U10
MAX4122/SOT
Temp Case Mon 1
TEMP MONITOR 2
+5 V dc
J2
AD590LF
R31
698
R28
402
R29
10.2k
R32
100
R30
162k
R33
3.32k
C22
1 uF
U11
MAX4122/SOT
Temp CPU Mon 2
Title
Tempurature Sensing
Size
A
Document Number
<Doc>
Rev
2.7
Date:
Wednesday, March 02, 2005
Sheet
5
of
6

APPENDIX B: IMPACCT 2 CARRIER BOARD SCHEMATICS


J1A
AIRBORN-RC4
FRAME~
IRDY~
TRDY~
STOP~
DEVSEL~
PERR~
SERR~
OFF_BOARD_CLK
C/BE3~
C/BE2~
C/BE1~
C/BE0~
RSTO_L
PAR
INTA~
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
J2B
AIRBORN-RC4
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD09
AD08
AD07
AD06
AD05
AD04
AD03
AD02
AD01
AD00
PMC2_J051
PMC2_J053
PMC2_J055
J7C
AIRBORN-RC4
PMC2_J01
PMC2_J03
PMC2_J05
PMC2_J07
PMC2_J09
PMC2_J011
PMC2_J013
PMC2_J015
PMC2_J017
PMC2_J019
PMC2_J021
PMC2_J023
PMC2_J025
PMC2_J027
PMC2_J029
PMC2_J031
PMC2_J033
PMC2_J035
PMC2_J037
PMC2_J039
PMC2_J041
PMC2_J043
PMC2_J045
PMC2_J047
PMC2_J049
J8D
AIRBORN-RC4
PMC2_J02
PMC2_J04
PMC2_J06
PMC2_J08
PMC2_J010
PMC2_J012
PMC2_J014
PMC2_J016
PMC2_J018
PMC2_J020
PMC2_J022
PMC2_J024
PMC2_J026
PMC2_J028
PMC2_J030
PMC2_J032
PMC2_J034
PMC2_J036
PMC2_J038
PMC2_J040
PMC2_J042
PMC2_J044
PMC2_J046
PMC2_J048
PMC2_J050
J9A
AIRBORN-RC4
+5 V dc
+3.3 V dc
−12 V dc
+12 V dc
−12 V dc
+12 V dc
+5 V dc
+3.3 V dc
+5 V dc
+3.3 V dc
Temperature PCM input 1
Temperature PCM input 2
GPIO(2)
GPIO(1)
GPIO(0)
+5 V dc
+3.3 V dc
+5 V dc
+3.3 V dc
J10B
AIRBORN-RC4
PMC1_J051
PMC1_J053
PMC1_J055
PMC1_J057
PMC1_J059
PMC1_J061
PMC1_J063
PMC1_J052
PMC1_J054
PMC1_J056
PMC1_J058
PMC1_J060
PMC1_J062
PMC1_J064
PMC2_J060
PMC2_J062
PMC2_J064
PMC2_J057
PMC2_J059
PMC2_J061
PMC2_J063
PMC2_J052
PMC2_J054
PMC2_J056
PMC2_J058
J11C
AIRBORN-RC4
PMC1_J01
PMC1_J03
PMC1_J05
PMC1_J07
PMC1_J09
PMC1_J011
PMC1_J013
PMC1_J015
PMC1_J017
PMC1_J019
PMC1_J021
PMC1_J023
PMC1_J025
PMC1_J027
PMC1_J029
PMC1_J031
PMC1_J033
PMC1_J035
PMC1_J037
PMC1_J039
PMC1_J041
PMC1_J043
PMC1_J045
PMC1_J047
PMC1_J049
J12D
AIRBORN-RC4
PMC1_J02
PMC1_J04
PMC1_J06
PMC1_J08
PMC1_J010
PMC1_J012
PMC1_J014
PMC1_J016
PMC1_J018
PMC1_J020
PMC1_J022
PMC1_J024
PMC1_J026
PMC1_J028
PMC1_J030
PMC1_J032
PMC1_J034
PMC1_J036
PMC1_J038
PMC1_J040
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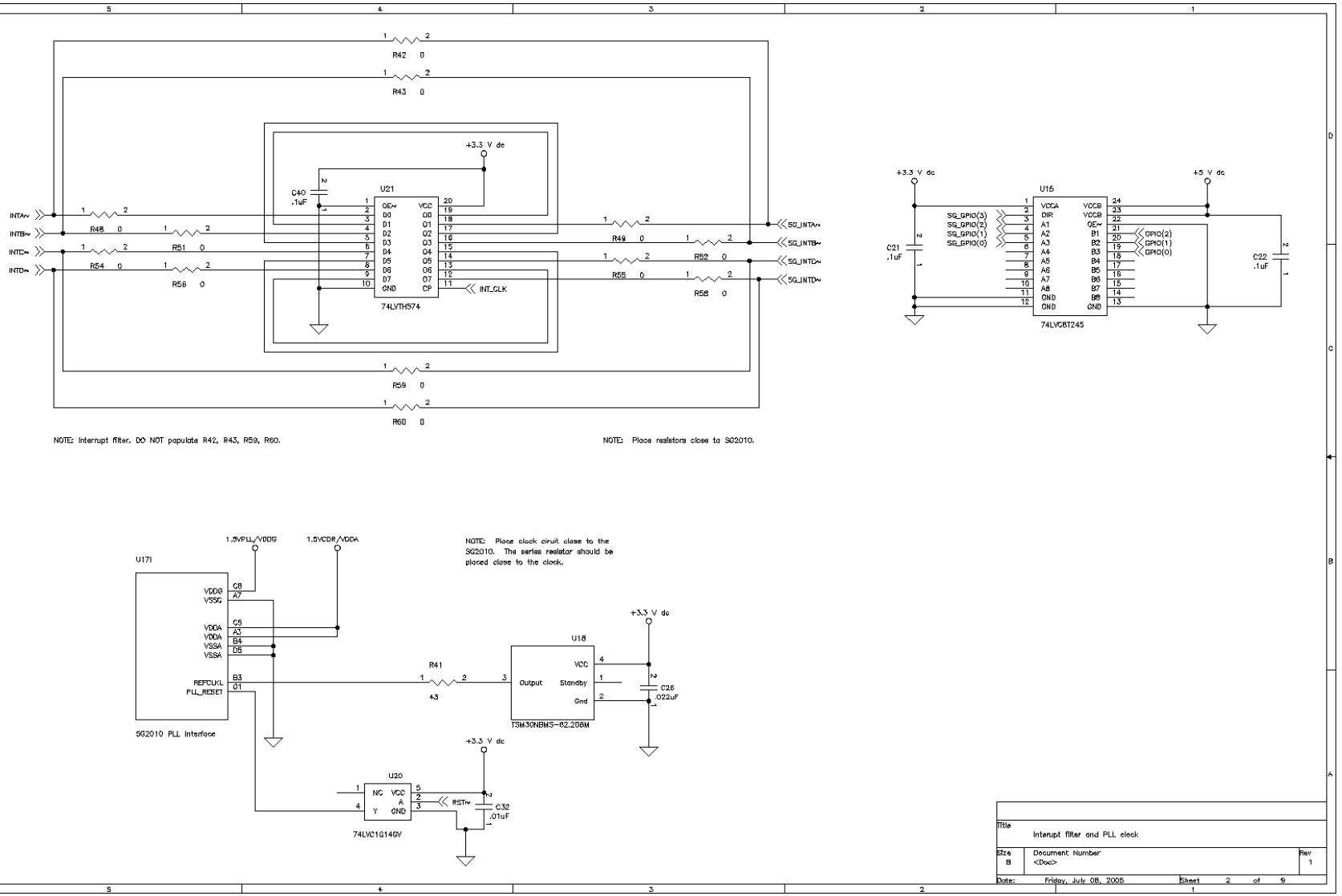
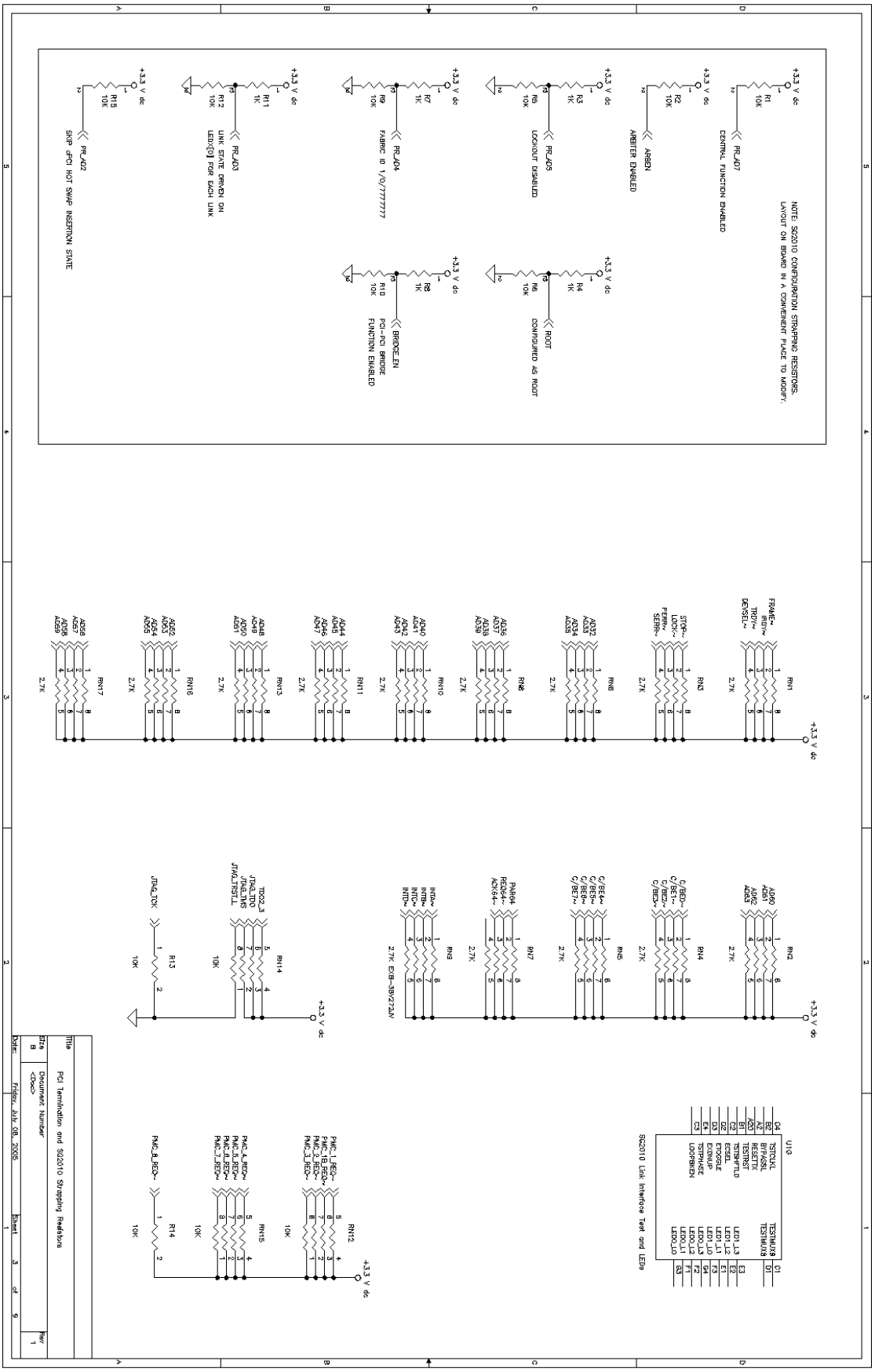
PMC1_J046
PMC1_J048
PMC1_J050
Title
AIRBORN Board Connector
Size
B
Document Number
<Doc>
Rev
1
Date:
Thursday, June 30, 2005
Sheet
1
of
8



Title	Interupt filter and PLL clock	
Size B	Document Number <Doc>	Rev 1
Date: Friday, July 08, 2005	Sheet 2 of 9	


NOTE: SC2010 CONFIGURATION STRAPPING RESISTORS.
LAYOUT ON BOARD IN A CONVENIENT PLACE TO MODIFY.
+3.3 V dc
R1 10K
PRJ_A07
CENTRAL FUNCTION ENABLED
R2 10K
ARBEN
ARBITER ENABLED
R3 1K
PRJ_A05
LOCKOUT DISABLED
R4 1K
ROOT
CONFIGURED AS ROOT
R7 1K
PRJ_A04
FABRIC ID 1/0/7777777
R8 1K
BRIDGE_EN
PCI-PCI BRIDGE FUNCTION ENABLED
R11 1K
PRJ_A03
LINK STATE DRIVEN ON LED'S[0] FOR EACH LINK
R15 10K
PRJ_A02
SKIP dPCI HOT SWAP INSERTION STATE
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
RN13
RN15
RN16
RN17
2.7K
R13
R14
10K
RN14
TDO22_3
JTAG_TDO
JTAG_TMS
JTAG_TRSTLL
JTAG_TCK
U10
SC2010 Link Interface Test and LEDs
Title
PCI Termination and SC2010 Strapping Resistors
Size
B
Document Number
<Doc>
Rev
1
Date:
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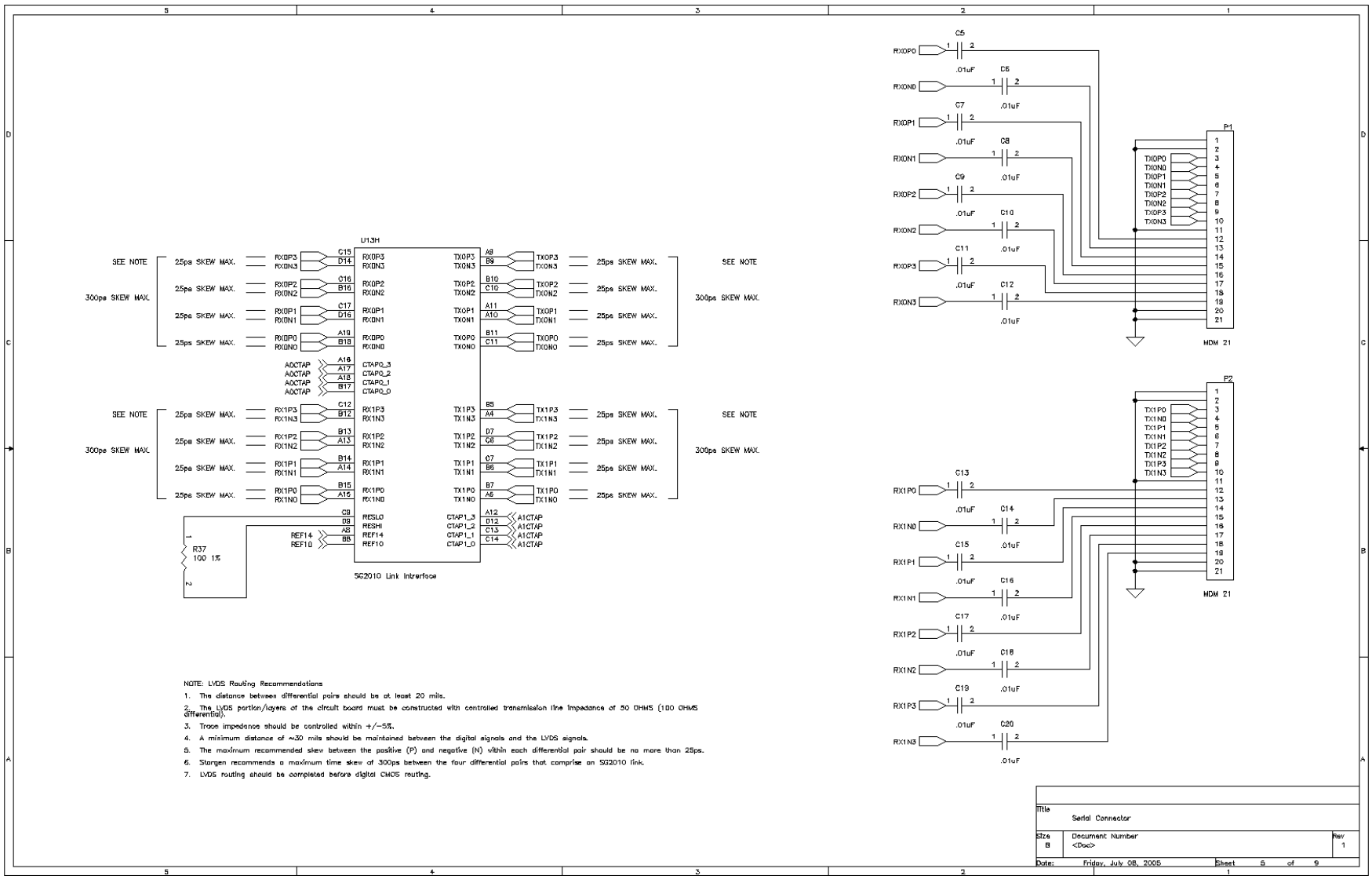
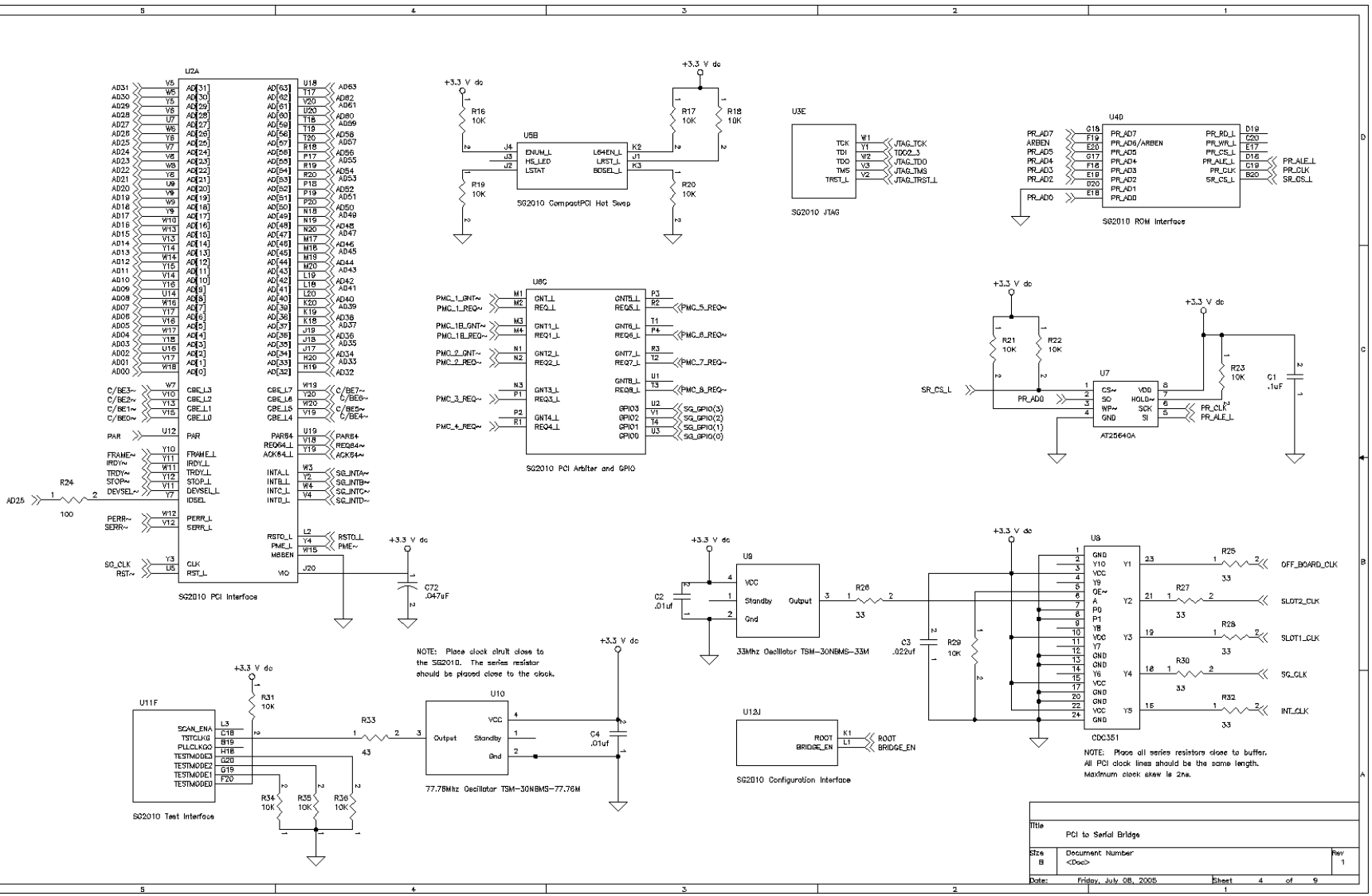
3
of
9

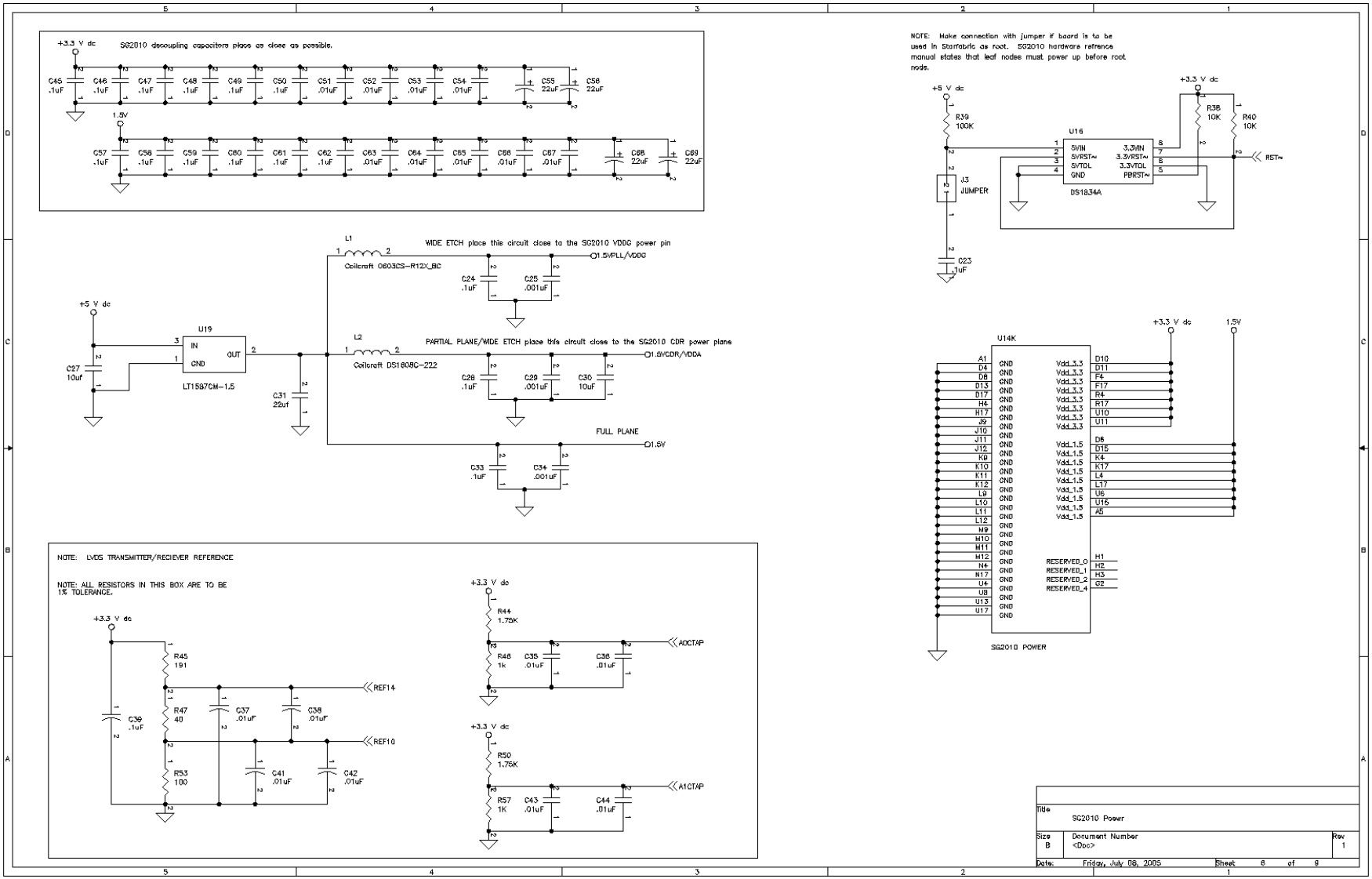


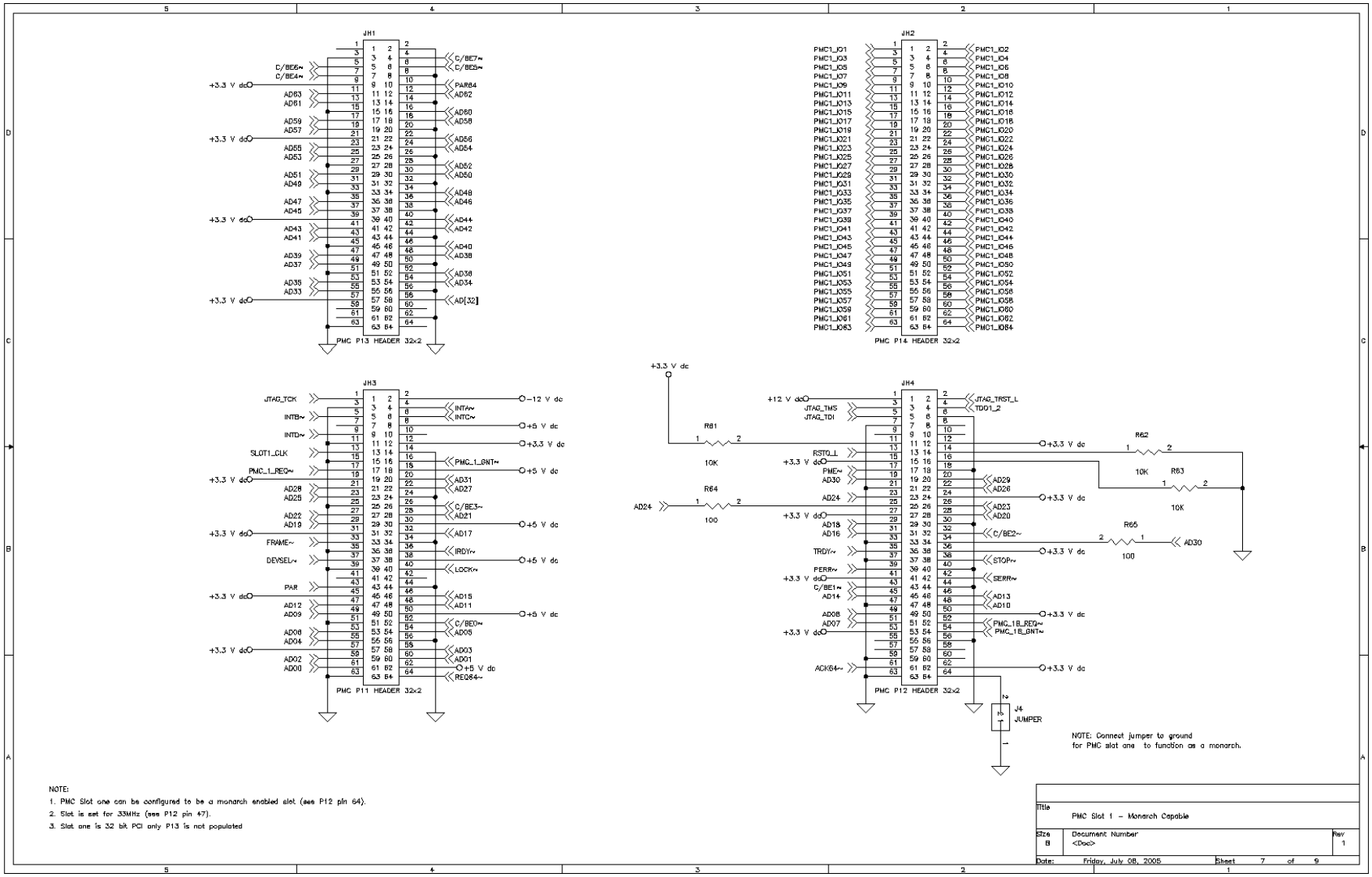
NOTE: LVDS Routing Recommendations

1. The distance between differential pairs should be at least 20 mils.
2. The LVDS portion/layers of the circuit board must be constructed with controlled transmission line impedance of 50 OHMS (100 OHMS differential).
3. Trace impedance should be controlled within +/−5%.
4. A minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.
5. The maximum recommended skew between the positive (P) and negative (N) within each differential pair should be no more than 25ps.
6. Stargen recommends a maximum time skew of 300ps between the four differential pairs that comprise an SG2010 link.
7. LVDS routing should be completed before digital CMOS routing.

Title: Serial Connector		
Size: B	Document Number: <Doc>	Rev: 1
Date: Friday, July 08, 2005	Sheet 5 of 9	


U2A
SG2010 PCI Interface
U5B
SG2010 CompactPCI Hot Swap
U3E
SG2010 JTAG
U4D
SG2010 ROM Interface
U6C
SG2010 PCI Arbiter and GPIO
U7
AT25640A
U11F
SG2010 Test Interface
U10
77.76Mhz Oscillator TSM-30NBMS-77.76M
U9
33Mhz Oscillator TSM-30NBMS-33M
U12J
SG2010 Configuration Interface
U8
CDC351
NOTE: Place clock ckuit close to the SG2010. The series resistor should be placed close to the clock.
NOTE: Place all series resistors close to buffer. All PCI clock lines should be the same length. Maximum clock skew is 2ns.
Title
PCI to Serial Bridge
Size B
Document Number <Doc>
Rev 1
Date: Friday, July 08, 2005
Sheet 4 of 9

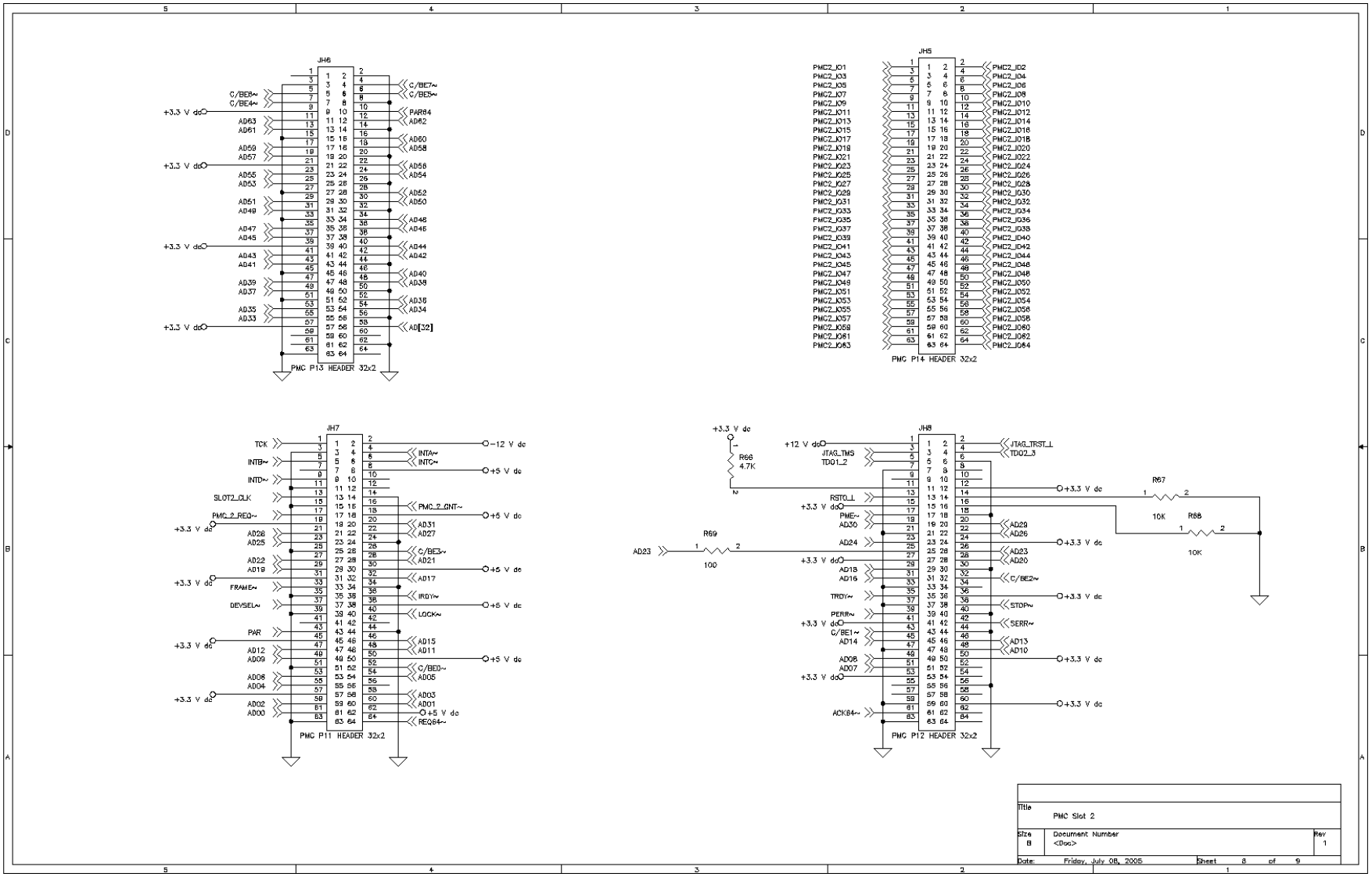

SG2010 decoupling capacitors place as close as possible.
+3.3 V dc
1.5V
C45 .1uF
C46 .1uF
C47 .1uF
C48 .1uF
C49 .1uF
C50 .1uF
C51 .01uF
C52 .01uF
C53 .01uF
C54 .01uF
C55 22uF
C56 22uF
C57 .1uF
C58 .1uF
C59 .1uF
C60 .1uF
C61 .1uF
C62 .1uF
C63 .01uF
C64 .01uF
C65 .01uF
C66 .01uF
C67 .01uF
C68 22uF
C69 22uF
NOTE: Make connection with jumper if board is to be used in Starfabric as root. SG2010 hardware refrence manual states that leaf nodes must power up before root node.
+5 V dc
+3.3 V dc
R39 100K
R38 10K
R40 10K
U16
5VIN
5VRST~
5VTOL
GND
3.3VIN
3.3VRST~
3.3VTOL
PBRST~
DS1834A
RST~
J3 JUMPER
C23 .1uF
L1
WIDE ETCH place this circuit close to the SG2010 VDDG power pin
Coilcraft 0803CS-R12X_BC
1.5VPLL/VDDG
C24 .1uF
C25 .001uF
+5 V dc
U19
IN
GND
OUT
LT1587CM-1.5
C27 10uF
C31 22uF
L2
PARTIAL PLANE/WIDE ETCH place this circuit close to the SG2010 CDR power plane
Coilcraft DS1608C-222
1.5VCDR/VDDA
C28 .1uF
C29 .001uF
C30 10uF
FULL PLANE
1.5V
C33 .1uF
C34 .001uF
+3.3 V dc
1.5V
U14K
SG2010 POWER
GND
Vdd_3.3
Vdd_1.5
RESERVED_0
RESERVED_1
RESERVED_2
RESERVED_4
NOTE: LVDS TRANSMITTER/RECIEVER REFERENCE
NOTE: ALL RESISTORS IN THIS BOX ARE TO BE 1% TOLERANCE.
+3.3 V dc
R45 191
R47 40
R53 100
C39 .1uF
C37 .01uF
C38 .01uF
C41 .01uF
C42 .01uF
REF14
REF10
R44 1.75K
R48 1k
C35 .01uF
C36 .01uF
ADCTAP
R50 1.75K
R57 1K
C43 .01uF
C44 .01uF
A1CTAP
Title
SG2010 Power
Size B
Document Number <Doc>
Rev 1
Date: Friday, July 08, 2005
Sheet 8 of 9

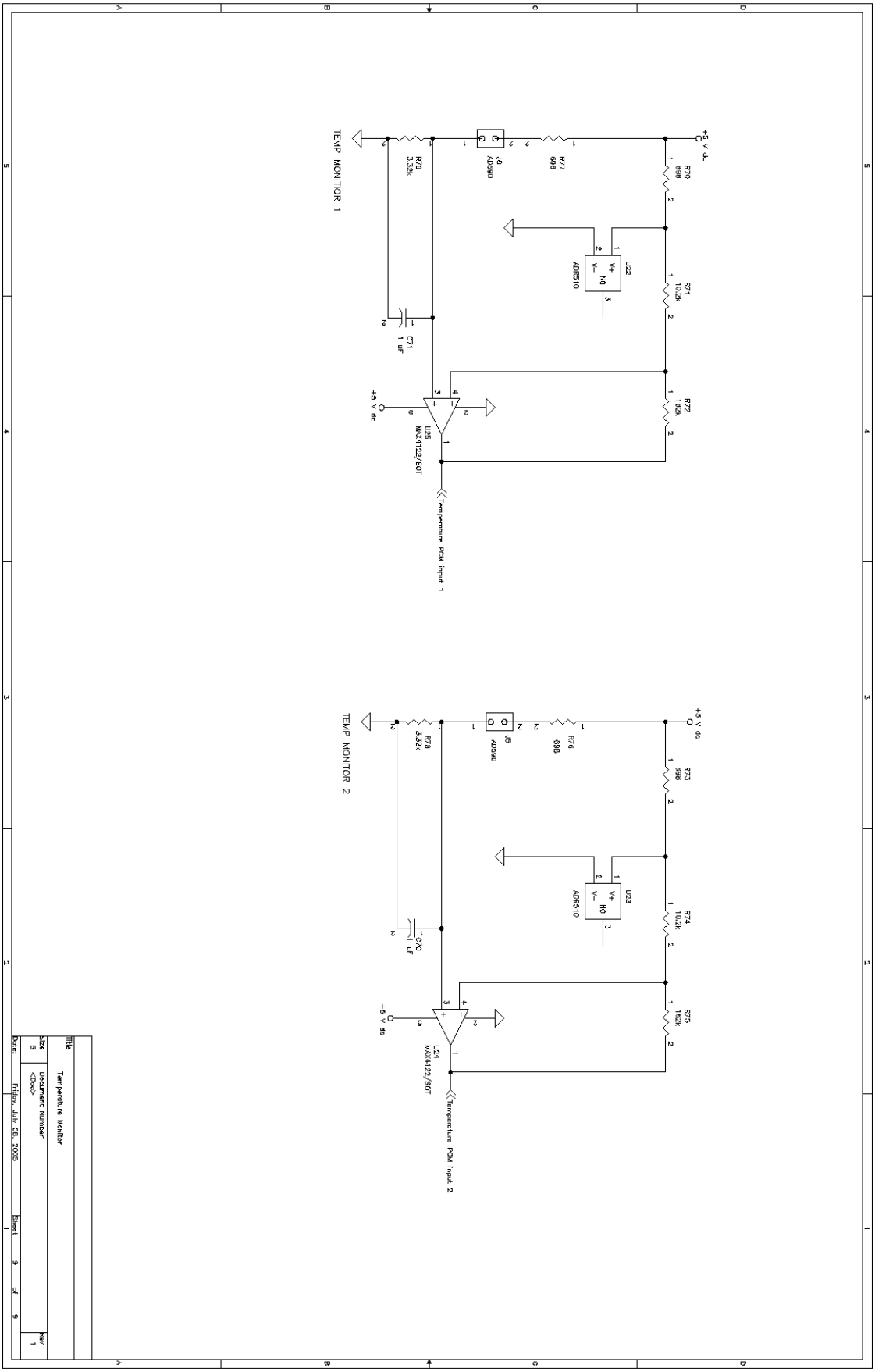


NOTE:

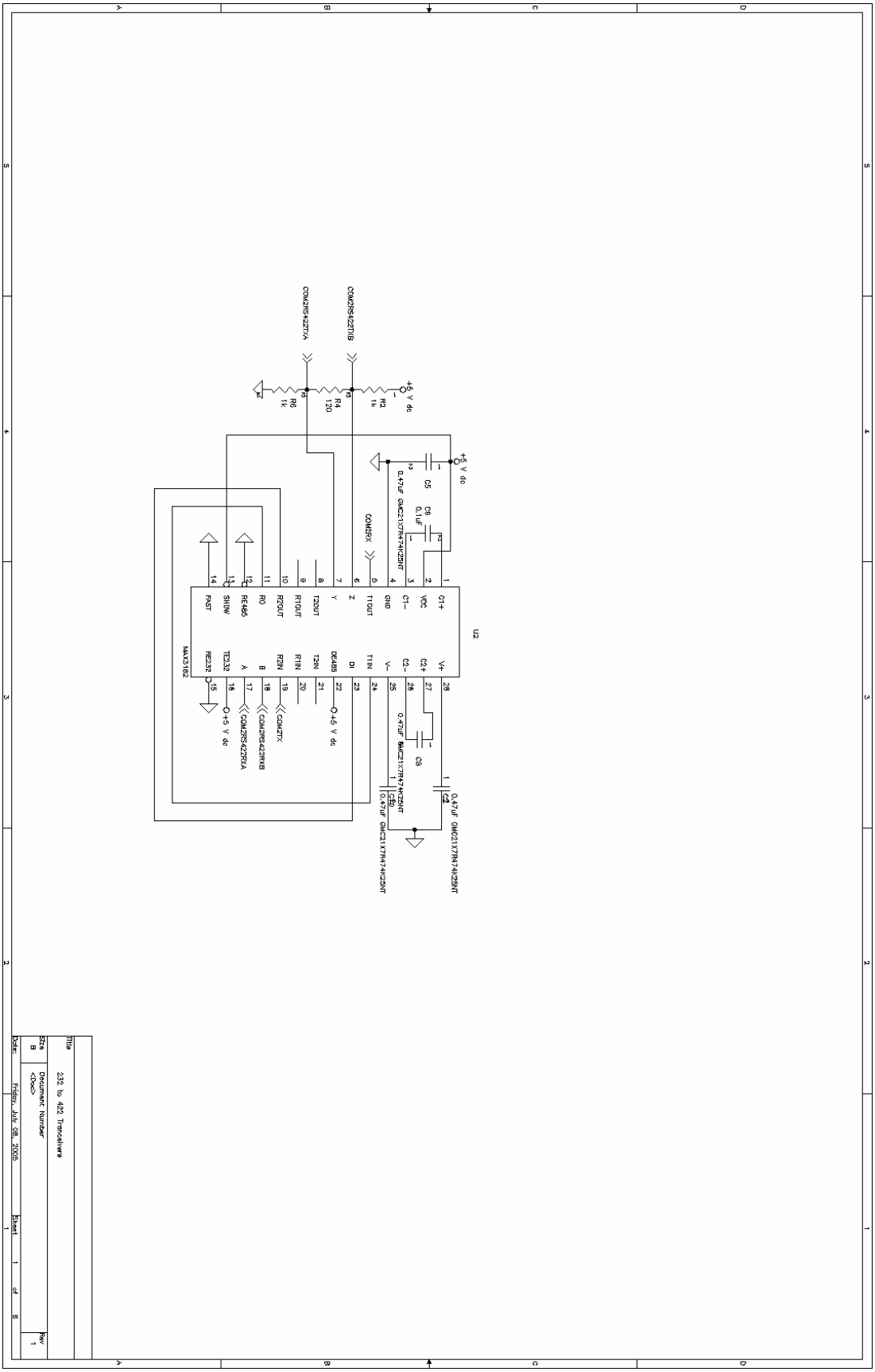
1. PMC Slot one can be configured to be a monarch enabled slot (see P12 pin 64).
2. Slot is set for 33MHz (see P12 pin 47).
3. Slot one is 32 bit PCI only P13 is not populated

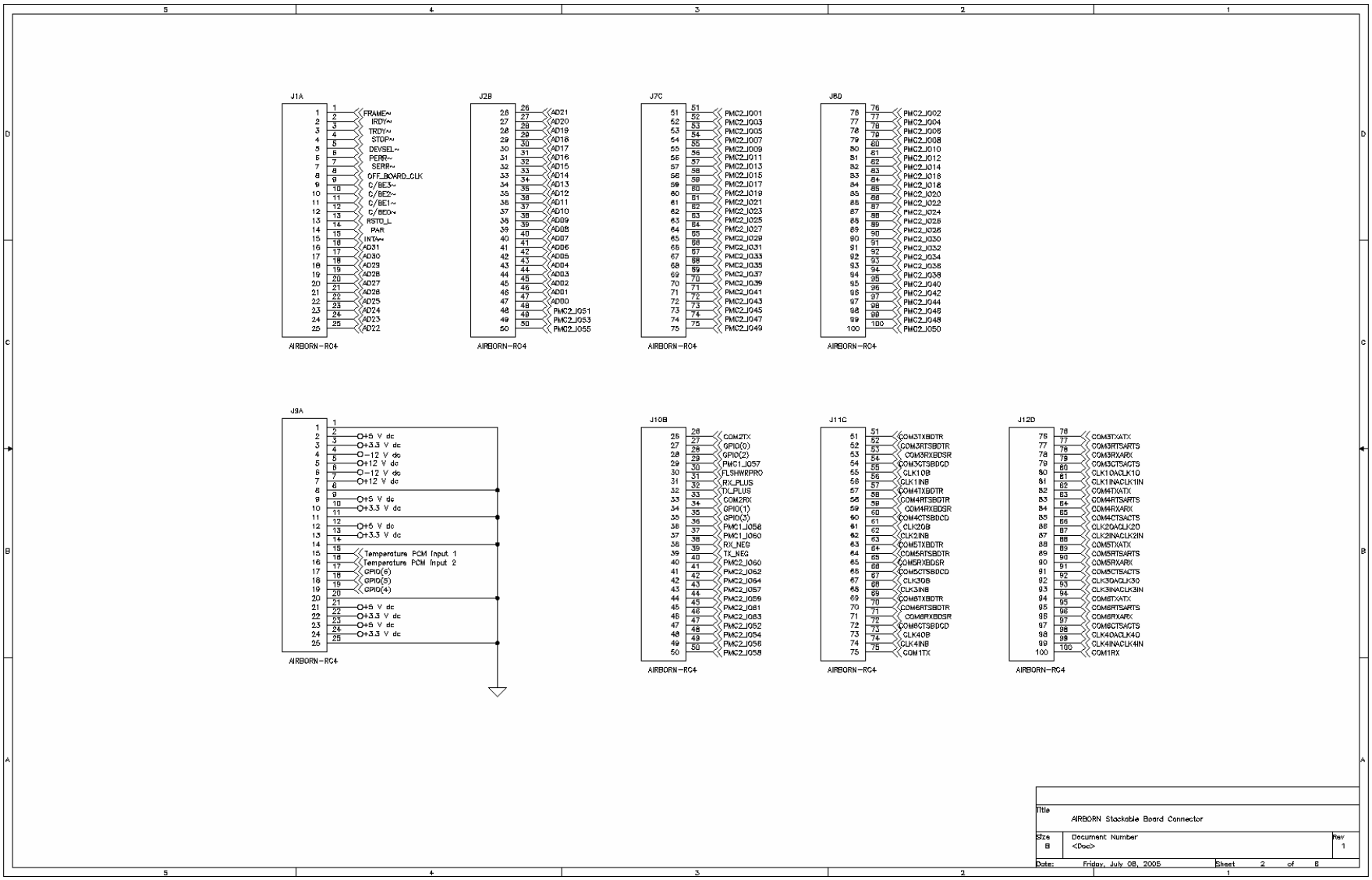
Title	PMC Slot 1 – Monarch Capable	
Size B	Document Number <Doc>	Rev 1
Date: Friday, July 08, 2005	Sheet 7 of 9	

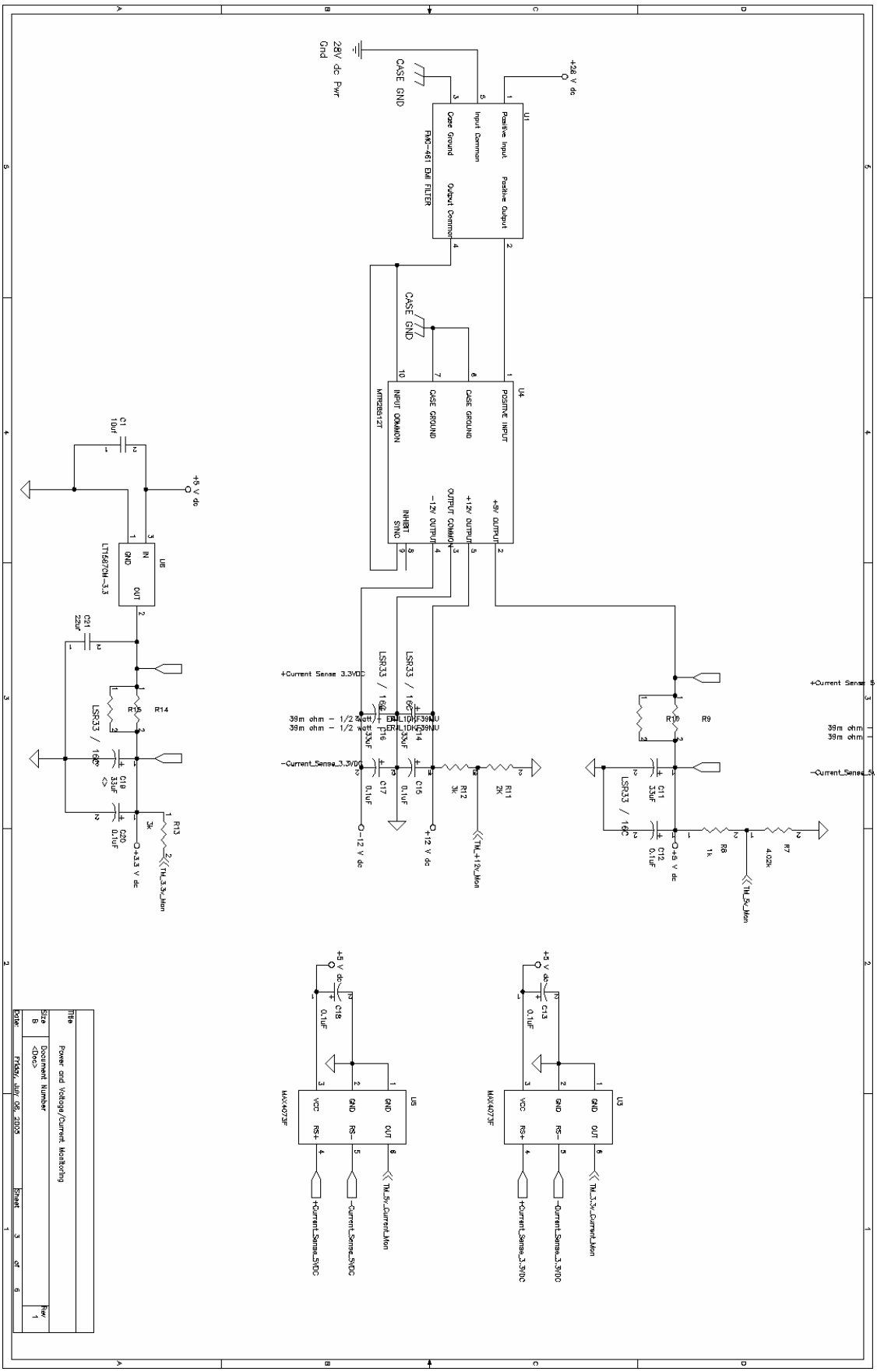

JH6
PMC P13 HEADER 32x2
JH5
PMC P14 HEADER 32x2
JH7
PMC P11 HEADER 32x2
JH8
PMC P12 HEADER 32x2
R66
4.7K
R67
10K
R68
10K
R69
100
Title
PMC Slot 2
Size
B
Document Number
<Doc>
Rev
1
Date:
Friday, July 08, 2005
Sheet
8
of
9


TEMP MONITOR 1
+5 V dc
J6
AD590
R77
698
R70
698
R78
3.32k
C71
1 uF
U22
ADR510
R71
10.2k
R72
162k
U25
MAX4122/SOT
Temperature PCM Input 1
TEMP MONITOR 2
+5 V dc
J5
AD590
R76
698
R73
698
R79
3.32k
C70
1 uF
U23
ADR510
R74
10.2k
R75
162k
U24
MAX4122/SOT
Temperature PCM Input 2
Title
Temperature Monitor
Size
B
Document Number
<Doc>
Rev
1
Date:
Friday, July 28, 2006
Sheet
3
of
6

APPENDIX C: IMPACCT 2 CONNECTOR/POWER BOARD SCHEMATICS


COM2RS422TXA
COM2RS422TXB
+5 V dc
R6 1k
R4 120
R2 1k
C5 0.1uF
C6 0.1uF
C3 0.47uF
C4 0.47uF
C1 0.47uF
C2 0.47uF
GNC21X7R474K25NT
COM2RX
U2
C1+
VCC
C1-
GND
T1OUT
T1IN
C2+
C2-
V+
V-
DE485
DI
T2IN
R1IN
R2IN
B
A
TE232
RE232
T2OUT
R1OUT
R2OUT
RO
RE485
SHDW
FAST
Y
Z
MAX3318
COM4TX
COM2RS422RXB
COM2RS422RXA
+5 V dc
Title
232 to 422 Transceivers
Size B
Document Number
<Doc>
Rev 1
Date: Friday, July 08, 2005
Sheet 1 of 8


J1A
1 FRAME#
2 IRDY#
3 TRDY#
4 STOP#
5 DEVSEL#
6 PERR#
7 SERR#
8 OFF_BOARD_CLK
9 C/BE3#
10 C/BE2#
11 C/BE1#
12 C/BE0#
13 RSTO_L
14 PAR
15 INTA#
16 AD31
17 AD30
18 AD29
19 AD28
20 AD27
21 AD26
22 AD25
23 AD24
24 AD23
25 AD22
AIRBORN-RC4
J2B
26 AD21
27 AD20
28 AD19
29 AD18
30 AD17
31 AD16
32 AD15
33 AD14
34 AD13
35 AD12
36 AD11
37 AD10
38 AD09
39 AD08
40 AD07
41 AD06
42 AD05
43 AD04
44 AD03
45 AD02
46 AD01
47 AD00
48 PMC2_IO51
49 PMC2_IO53
50 PMC2_IO55
AIRBORN-RC4
J7C
51 PMC2_IO01
52 PMC2_IO03
53 PMC2_IO05
54 PMC2_IO07
55 PMC2_IO09
56 PMC2_IO11
57 PMC2_IO13
58 PMC2_IO15
59 PMC2_IO17
60 PMC2_IO19
61 PMC2_IO21
62 PMC2_IO23
63 PMC2_IO25
64 PMC2_IO27
65 PMC2_IO29
66 PMC2_IO31
67 PMC2_IO33
68 PMC2_IO35
69 PMC2_IO37
70 PMC2_IO39
71 PMC2_IO41
72 PMC2_IO43
73 PMC2_IO45
74 PMC2_IO47
75 PMC2_IO49
AIRBORN-RC4
J8D
76 PMC2_IO02
77 PMC2_IO04
78 PMC2_IO06
79 PMC2_IO08
80 PMC2_IO10
81 PMC2_IO12
82 PMC2_IO14
83 PMC2_IO16
84 PMC2_IO18
85 PMC2_IO20
86 PMC2_IO22
87 PMC2_IO24
88 PMC2_IO26
89 PMC2_IO28
90 PMC2_IO30
91 PMC2_IO32
92 PMC2_IO34
93 PMC2_IO36
94 PMC2_IO38
95 PMC2_IO40
96 PMC2_IO42
97 PMC2_IO44
98 PMC2_IO46
99 PMC2_IO48
100 PMC2_IO50
AIRBORN-RC4
J9A
1
2 +5 V dc
3 +3.3 V dc
4 -12 V dc
5 +12 V dc
6 -12 V dc
7 +12 V dc
8
9 +5 V dc
10 +3.3 V dc
11
12 +5 V dc
13 +3.3 V dc
14
15 Temperature PCM Input 1
16 Temperature PCM Input 2
17 GPIO(6)
18 GPIO(5)
19 GPIO(4)
20
21 +5 V dc
22 +3.3 V dc
23 +5 V dc
24 +3.3 V dc
25
AIRBORN-RC4
J10B
26 COM2TX
27 GPIO(0)
28 GPIO(2)
29 PMC1_IO57
30 FLSHWEPRO
31 RX_PLUS
32 TX_PLUS
33 COM2RX
34 GPIO(1)
35 GPIO(3)
36 PMC1_IO58
37 PMC1_IO60
38 RX_NEG
39 TX_NEG
40 PMC2_IO60
41 PMC2_IO62
42 PMC2_IO64
43 PMC2_IO57
44 PMC2_IO59
45 PMC2_IO61
46 PMC2_IO63
47 PMC2_IO52
48 PMC2_IO54
49 PMC2_IO56
50 PMC2_IO58
AIRBORN-RC4
J11C
51 COM3TXBDTR
52 COM3RTSBDTR
53 COM3RXBDSR
54 COM3CTSBDCD
55 CLK10B
56 CLK1INB
57 COM4TXBDTR
58 COM4RTSBDTR
59 COM4RXBDSR
60 COM4CTSBDCD
61 CLK20B
62 CLK2INB
63 COM5TXBDTR
64 COM5RTSBDTR
65 COM5RXBDSR
66 COM5CTSBDCD
67 CLK30B
68 CLK3INB
69 COM6TXBDTR
70 COM6RTSBDTR
71 COM6RXBDSR
72 COM6CTSBDCD
73 CLK40B
74 CLK4INB
75 COM1TX
AIRBORN-RC4
J12D
76 COM3TXATX
77 COM3RTSARTS
78 COM3RXARX
79 COM3CTSACTS
80 CLK10ACLK10
81 CLK1INACLK1IN
82 COM4TXATX
83 COM4RTSARTS
84 COM4RXARX
85 COM4CTSACTS
86 CLK20ACLK20
87 CLK2INACLK2IN
88 COM5TXATX
89 COM5RTSARTS
90 COM5RXARX
91 COM5CTSACTS
92 CLK30ACLK30
93 CLK3INACLK3IN
94 COM6TXATX
95 COM6RTSARTS
96 COM6RXARX
97 COM6CTSACTS
98 CLK40ACLK40
99 CLK4INACLK4IN
100 COM1RX
AIRBORN-RC4
Title
AIRBORN Stackable Board Connector
Size B
Document Number
<Doc>
Rev 1
Date: Friday, July 08, 2005
Sheet 2 of 8


28V dc Pwr Gnd
CASE GND
+28 V dc
U1
Input Common
Positive Input
Case Ground
Positive Output
Output Common
FMC-481 EMI FILTER
U4
INPUT COMMON
CASE GROUND
POSITIVE INPUT
INHIBIT SYNC
OUTPUT COMMON
+12V OUTPUT
+5V OUTPUT
-12V OUTPUT
MYM28S12T
+5 V dc
U6
IN
GND
OUT
LT1587CM-3.3
C1 10ur
C21 22ur
R15
R14
LSR33 / 1dC
C19 33uF
C20 0.1uF
R13 3k
TM_3.3v_Mon
+3.3 V dc
+Current Sense 3.3VDC
39m ohm - 1/2 watt
C16 33uF
C14 33uF
-Current_Sense_3.3VDC
C17 0.1uF
C15 0.1uF
R12 3k
R11 2K
TM_+12v_Mon
+12 V dc
-12 V dc
R10
R9
C11 33uF
C12 0.1uF
R8 1k
R7 4.02k
TM_5v_Mon
+5 V dc
U5
MAX4073F
C18 0.1uF
VCC
RS+
RS-
GND
OUT
TM_5v_Current_Mon
+Current_Sense_5VDC
-Current_Sense_5VDC
U3
C13 0.1uF
TM_3.3v_Current_Mon
+Current_Sense_3.3VDC
-Current_Sense_3.3VDC
Title
Power and Voltage/Current Monitoring
Size
B
Document Number
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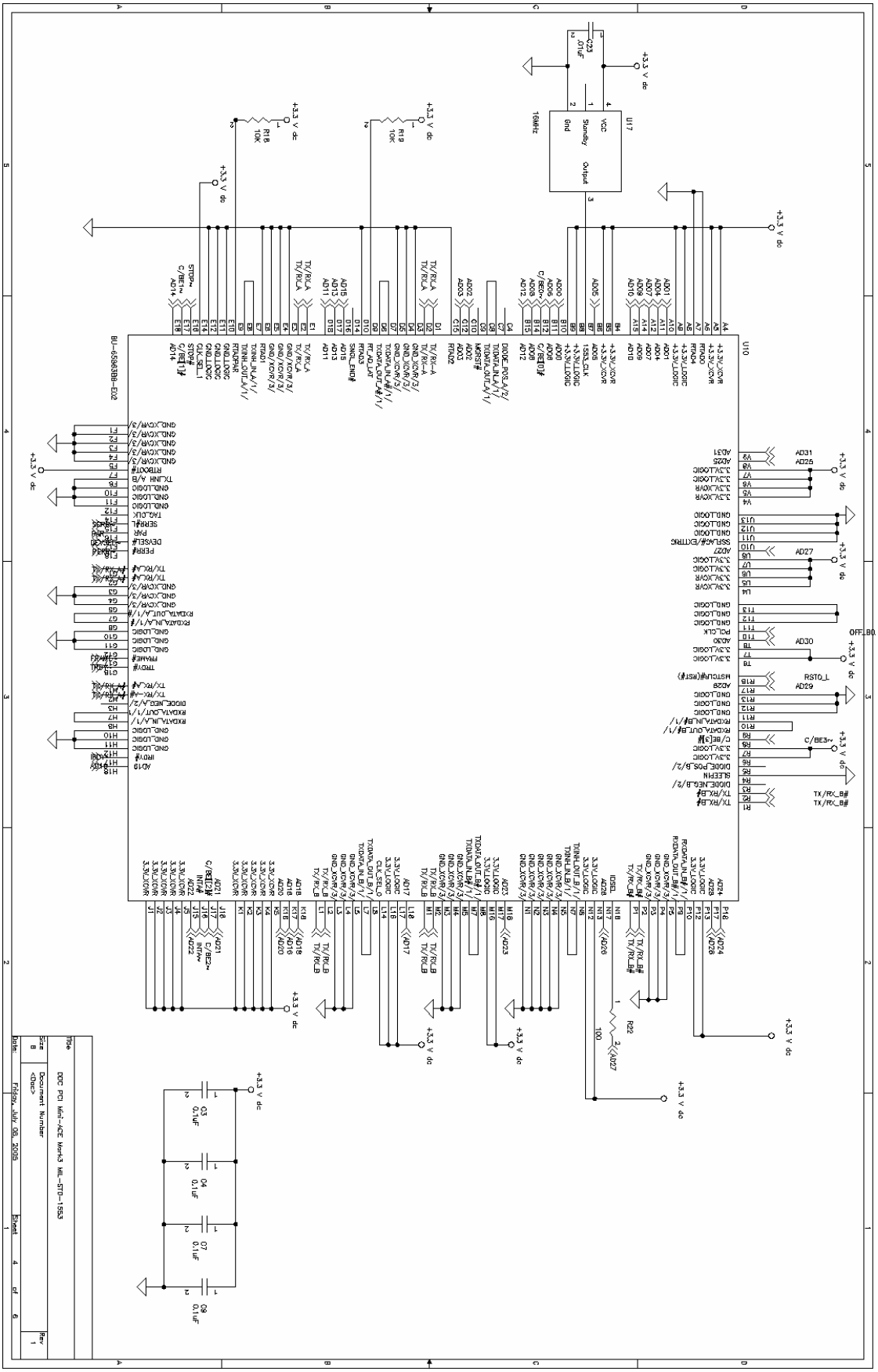

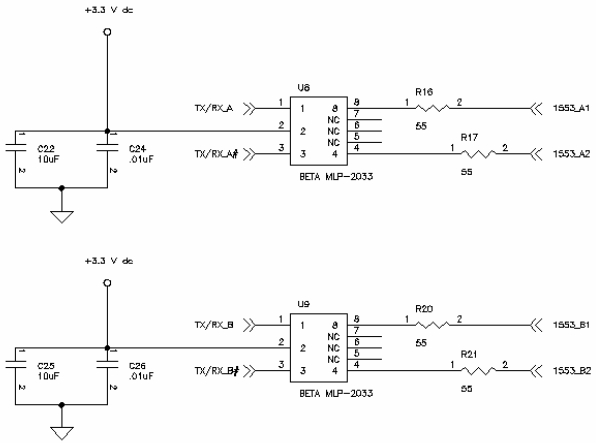

NOTE: Locate transformers close to BU-65863B8-E02. There should be no ground and/or power supply planes underneath the TX/RX_A/B traces, the transformers or 1553_A/ B traces. Avoid, if at all possible, running the 1553 analog signal traces in close proximity to other analog and digital signals on the

board.

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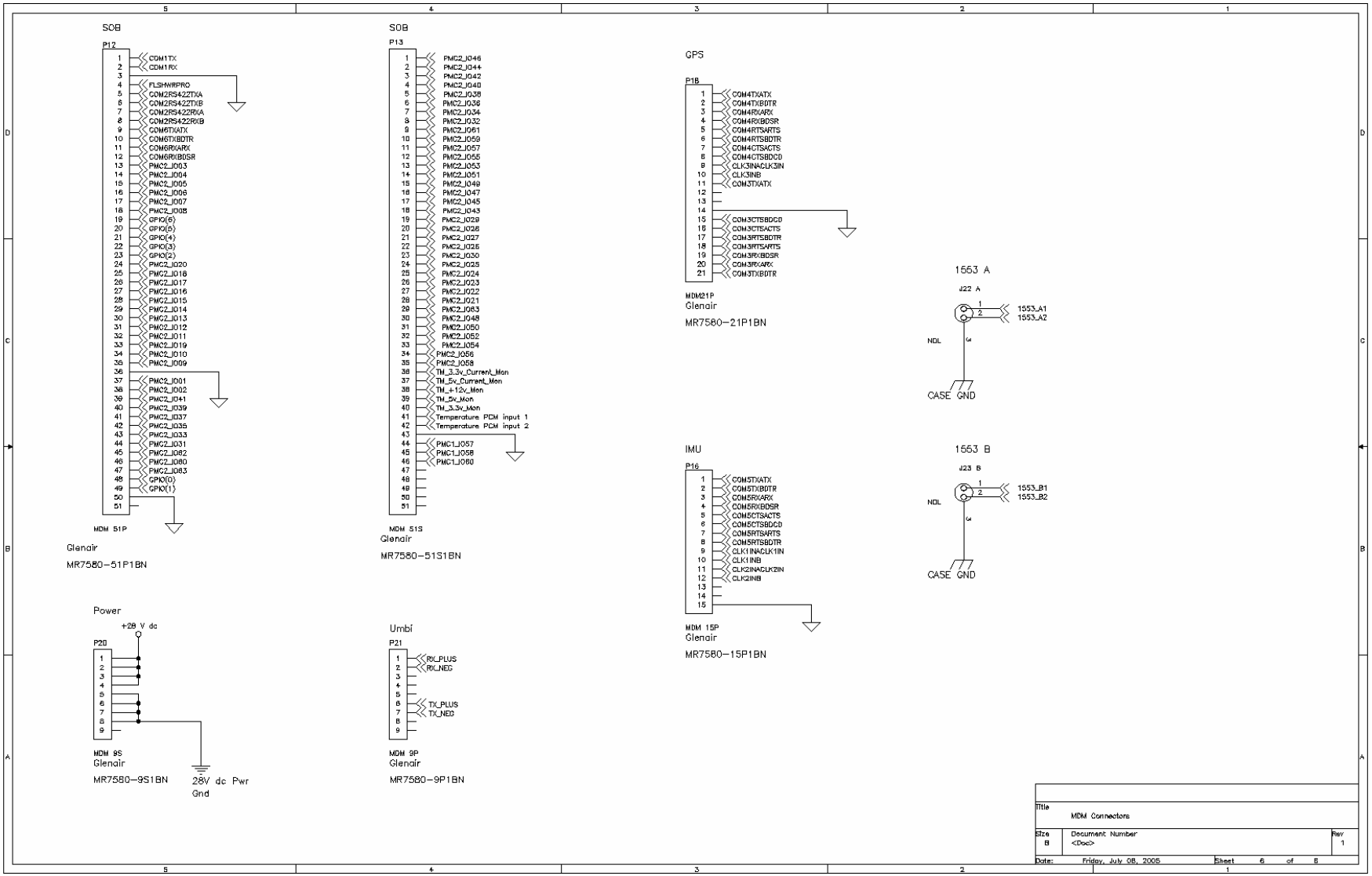
SOB
P12
COM1TX
COM1RX
FLSHWRPRO
COM2RS422TXA
COM2RS422TXB
COM2RS422RXA
COM2RS422RXB
COM6TXATX
COM6TXBDTR
COM6RXARX
COM6RXBDSR
PMC2_IO03
PMC2_IO04
PMC2_IO05
PMC2_IO06
PMC2_IO07
PMC2_IO08
GPIO(6)
GPIO(5)
GPIO(4)
GPIO(3)
GPIO(2)
PMC2_IO20
PMC2_IO18
PMC2_IO17
PMC2_IO16
PMC2_IO15
PMC2_IO14
PMC2_IO13
PMC2_IO12
PMC2_IO11
PMC2_IO19
PMC2_IO10
PMC2_IO09
PMC2_IO01
PMC2_IO02
PMC2_IO41
PMC2_IO39
PMC2_IO37
PMC2_IO35
PMC2_IO33
PMC2_IO31
PMC2_IO62
PMC2_IO60
PMC2_IO63
GPIO(0)
GPIO(1)
MDM 51P
Glenair
MR7580-51P1BN
SOB
P13
PMC2_IO46
PMC2_IO44
PMC2_IO42
PMC2_IO40
PMC2_IO38
PMC2_IO36
PMC2_IO34
PMC2_IO32
PMC2_IO61
PMC2_IO59
PMC2_IO57
PMC2_IO55
PMC2_IO53
PMC2_IO51
PMC2_IO49
PMC2_IO47
PMC2_IO45
PMC2_IO43
PMC2_IO29
PMC2_IO28
PMC2_IO27
PMC2_IO26
PMC2_IO30
PMC2_IO25
PMC2_IO24
PMC2_IO23
PMC2_IO22
PMC2_IO21
PMC2_IO63
PMC2_IO48
PMC2_IO50
PMC2_IO52
PMC2_IO54
PMC2_IO56
PMC2_IO58
TM_3.3v_Current_Mon
TM_5v_Current_Mon
TM_+12v_Mon
TM_5v_Mon
TM_3.3v_Mon
Temperature PCM input 1
Temperature PCM input 2
PMC1_IO57
PMC1_IO58
PMC1_IO60
MDM 51S
Glenair
MR7580-51S1BN
GPS
P18
COM4TXATX
COM4TXBDTR
COM4RXARX
COM4RXBDSR
COM4RTSARTS
COM4RTSBDTR
COM4CTSACTS
COM4CTSBDCD
CLK3INACLK3IN
CLK3INB
COM3TXATX
COM3CTSBDCD
COM3CTSACTS
COM3RTSBDTR
COM3RTSARTS
COM3RXBDSR
COM3RXARX
COM3TXBDTR
MDM21P
Glenair
MR7580-21P1BN
1553 A
J22 A
1553_A1
1553_A2
NDL
CASE GND
IMU
P16
COM5TXATX
COM5TXBDTR
COM5RXARX
COM5RXBDSR
COM5CTSACTS
COM5CTSBDCD
COM5RTSARTS
COM5RTSBDTR
CLK1INACLK1IN
CLK1INB
CLK2INACLK2IN
CLK2INB
MDM 15P
Glenair
MR7580-15P1BN
1553 B
J23 B
1553_B1
1553_B2
NDL
CASE GND
Power
+28 V dc
P20
MDM 9S
Glenair
MR7580-9S1BN
28V dc Pwr
Gnd
Umbi
P21
RX_PLUS
RX_NEG
TX_PLUS
TX_NEG
MDM 9P
Glenair
MR7580-9P1BN
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MDM Connectors
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