SIMPLE LOW COST TECHNIQUES FOR FREQUENCY SYNTHESIS

by

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TABLE OF CONTENTS

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INTRODUCTION

Requirement for the Frequency Synthesizer:

The Electronics Laboratory in the Electrical Engineering Department at the Kansas State University has a variety of Computer Systems such as the North Star Horizon, Hewlett Packard 9845 B, and LSI-11. These systems are used for making electrical measurements. One of the laboratory objectives is to automate the systems in such a way that making measurements is not a tedious and time consuming process. Towards this goal attempts are made to improve upon the existing test systems.

Most of the measurements are made with the aid of a Multiprogrammer. The multiprogrammer has various slots to house cards that have specific functions such as - the V/F card, the relay card, the VCO card, and others.

In the present test system, when a specific frequency has to be measured, it is supplied through the relay card onto the system, where measurements are made with the help of a frequency counter within the system. The frequency is supplied by a composite XR 2206 integrated circuit chip wherein the frequency can be varied with a proper setup of the supporting components. Though this gives a reasonably good output, it is found that there is a drift on the output frequency with time. Hence there has been the need for another system that functions better than the existing one and produces stable frequencies.

Several simple methods for the generation of sine waves are available. Here, attention is paid to three methods and a comparison is

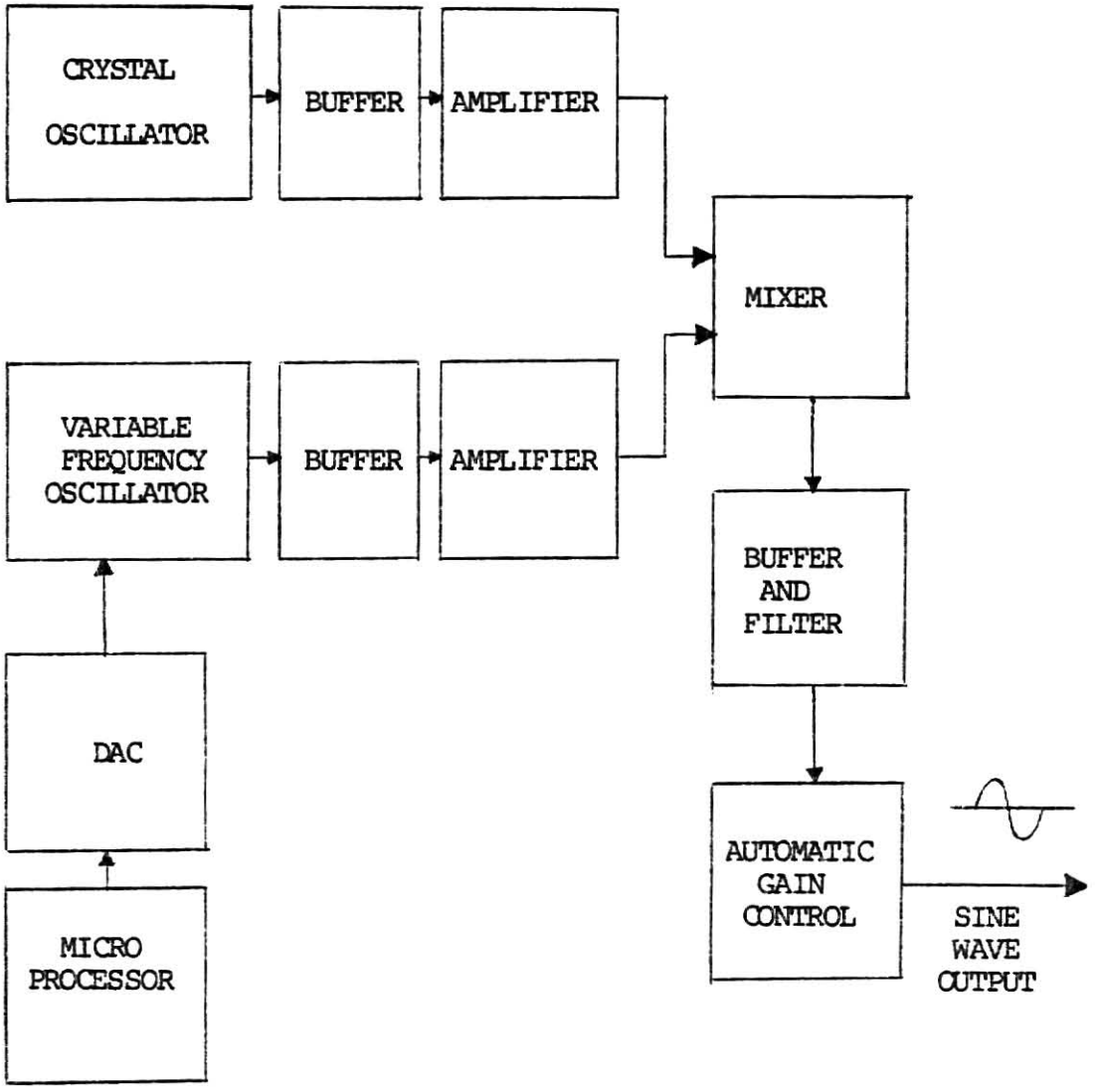


Fig. 1

Block Diagram of Frequency Synthesizer using higher frequencies

made between them.

For the first method, a block diagram of the proposed frequency synthesizer is shown in Fig.1. This consists of discrete components in each block and when put together gives the required output frequency.

In the proposed setup shown in Fig. 1, a higher fixed frequency of 6 M Hz is supplied by a crystal oscillator. The Variable Frequency Oscillator supplies frequencies of 5 to 6 M Hz which can be varied with a capacitor in the picofarad range. The two frequencies are run through a mixer which gives the output frequencies along with a lot of others. The variation in frequency causes amplitude modulation since the range of frequencies is high. The output of the mixer has to be filtered to get the required range of frequencies from 1 Hz to 1 M Hz. The amplitude is controlled by an automatic gain control circuit on the output side. The final output is a stable, drift-free sine wave of the required frequency.

Fig. 2 shows the block diagram of the second method. In this method, lower frequencies generate the sine waves of interest. One fixed frequency of 200 K Hz, and another variable frequency of 100 to 200 K Hz were mixed in an analog multiplier and an active filter used to obtain the clean wave.

The advantages in these two methods are :

1. They can be more easily controlled since the controlling parameter is a varicap - a variable capacitance, that functions in the picofarad range. A voltage variation varies the capacitance and this voltage can be conveniently supplied by the microprocessor via the D/A converter.

2. The output point supplies the required frequency which has

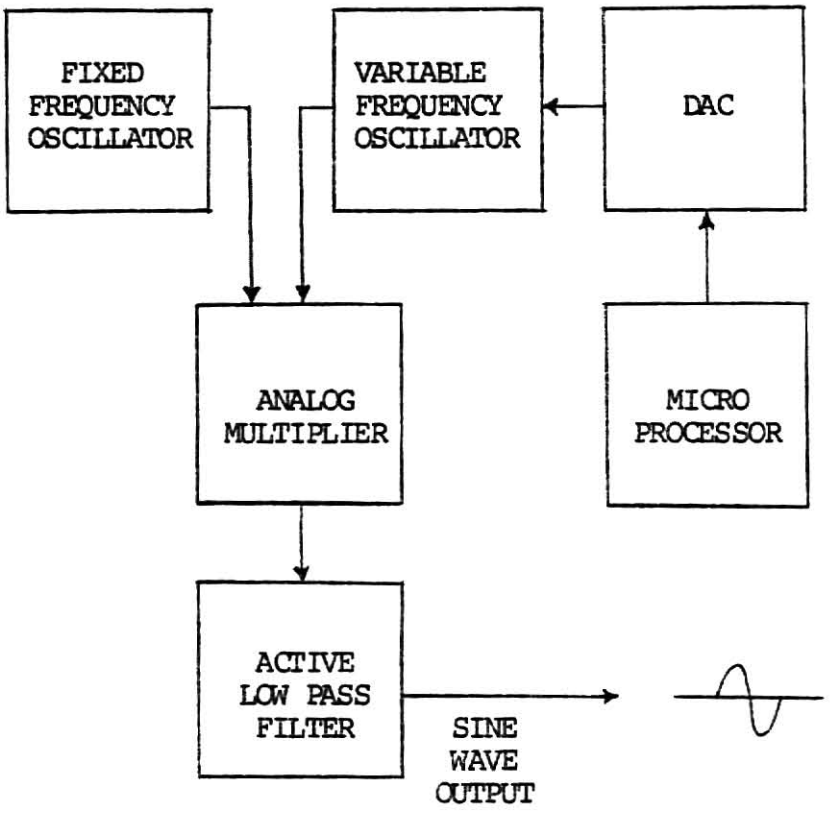


Fig. 2

Block diagram of frequency synthesis using an Analog Multiplier and lower fequencies.

already been measured by the microprocessor since the microprocessor itself calculates the frequency and outputs it. A feedback loop in the system can ensure this.

3. The output is a drift free sinusoid, especially if a feedback loop were to be used.

An ideal sinusoidal signal generator should provide an output signal that has the following characteristics :

a. Stable operating frequency

b. No harmonic content

c. Stable output amplitude

d. No spurious outputs.

The limitations on the components used restrict the precision of the characteristics available, and hence, in the above, the b and d cases get restricted to low harmonic content, and low spurious output - due to hum, noise, jitter, modulation, and other such factors.

A block diagram of the principle on which the third method is based is shown in Fig. 3. This is a digital method for the synthesis of a sine wave. The limitations in this method are the speed and the range of frequencies because of the speed of operation of the circuitry and components involved, and because of the limitations on the digital to analog converter. The idea in this method is to control a counter with the help of an oscillator, which counts out the sine wave amplitude samples stored in a read only memory, which in turn is fed to a digital to analog converter. The output waveform of the digital to analog converter will not be a continuous waveform but will have steps, but the filtered output will be a fairly smooth curve. The experimental analysis of this technique was done by a simulation technique on the

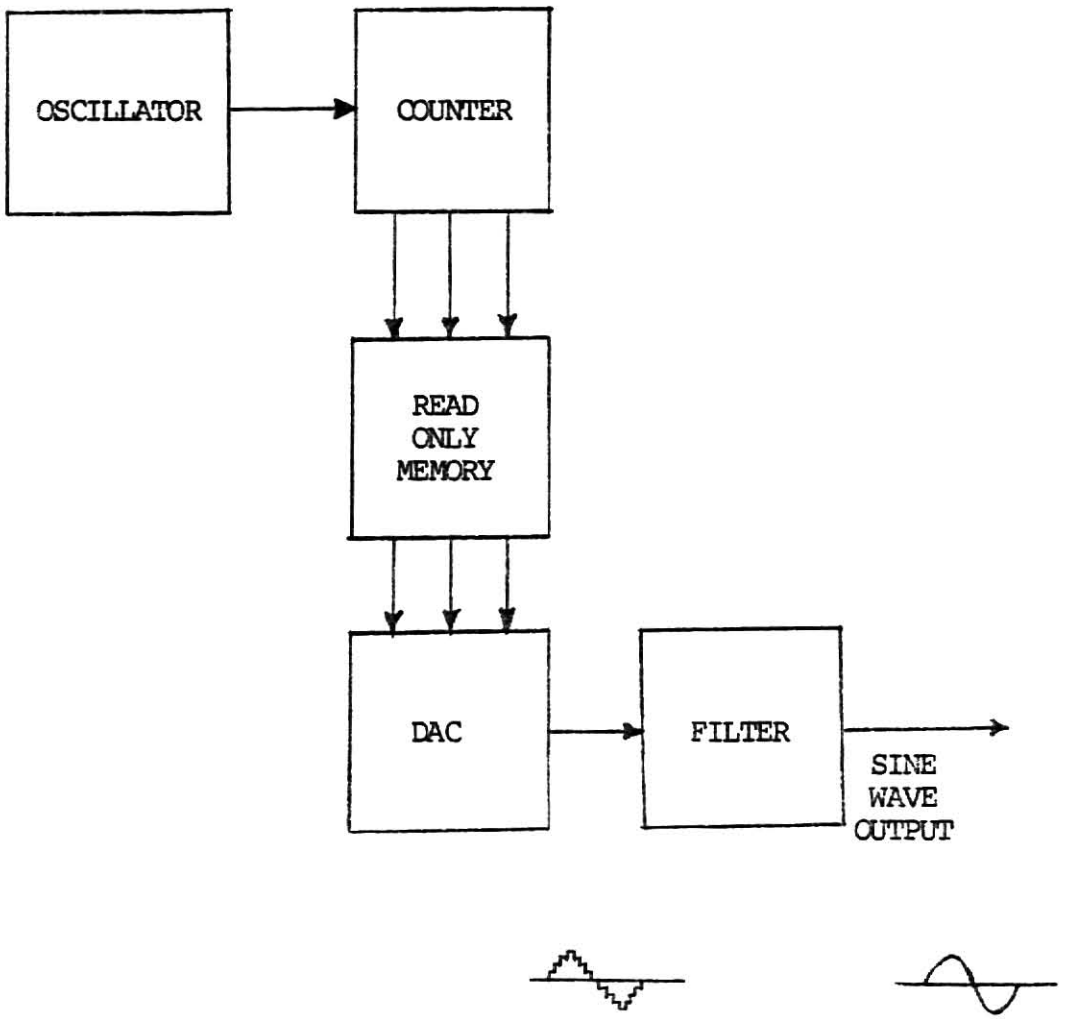


Fig. 3

Digital Technique for frequency synthesis.

PDP-11 Computer system. The system has an attachment which has a digital to analog converter in it . The output of the digital to analog converter is available at a convenient point and can be displayed on an oscilloscope. The read only memory is replaced by the random access memory of the system for this experiment. A machine language program, or a program in Fortran can be written to simulate the conditions to simulate the counter output. On running this program different frequencies of the sine wave can be displayed on the oscilloscope depending on the flexibility of the program.

In this report the three methods as explained above are studied in detail and a comparison is made between them.

GOOD DESIGN PRACTICES FOR BUILDING FREQUENCY SYNTHESIZERS.

A good frequency synthesizer [2] contains oscillators whose outputs are spectrally pure and stable. In spite of all the other parts of the circuit functioning in elegant fashion, oscillators not performing well enough can spoil the performance of the frequency synthesizer. The oscillator should not only have minimum noise in the output, but should also be stable with regard to short and long term drift, and be reasonably free of spurious responses. Quick starting when operating voltage is applied is another important characteristic of an oscillator.

Oscillator instability can result from poor design practices. To improve the stablity characteristics it is useful to observe the following points :

1. to use well filtered regulated operating voltages

2. whenever possible, to avoid the use of magnetic core material in the oscillator tank coil. (Air-wound or ceramic-form coils are found to be the best if they are rigid.)

3. to use fixed value, temperature stable capacitors in the frequency determining part of the circuit. (The recommended capacitor types are of Silver-mica or Polystyrene.)

4. chances of mechanical instability will be reduced if all the electrical and mechanical components are secured rigidly in their part of the circuit.

5. to build the oscillator on a firm, flex-free chasis.

6. when practical, to enclose the oscillator in its own shield

compartment and use RF filtering in the DC supply leads. More constant the ambient temperature surrounding the oscillator, greater will be the frequency stability.

Precautions should be taken to make sure that the oscillator looks into a constant load impedance. Phase shifts can even be caused by minute load changes which can affect the oscillator frequency. The effect is more obvious with variable frequency oscillators than with crystal controlled oscillators. It is good design practice to couple very lightly to the oscillator stage because of the above conditions. By adding one or more buffer or amplifier stages before the oscillator signal is supplied to the mixer, the power level can be increased.

Frequency shifts can be caused by changes in operating voltages. Hence, regulated voltages are recommended for oscillators.

Inductance in magnetic cores, such as slug-tuned coils, vary with ambient temperature variations which can severely affect the oscillator frequency. Slugs, not fixed properly in the coil forms can cause mechanical instability. Therefore, toroidal inductors are unsuitable for use in stable variable frequency oscillators.

High-Q tuned circuits can be used to hold the oscillator noise to an acceptable level. Higher the tank Q, narrower the bandwidth, and lower the noise output voltage. Excessive low noise will have a serious effect on mixer performance.

Unwanted mixer injection can be caused by high amounts of harmonic content in the low chain output. It is worthwhile using suitable filtering at the low-chain output since harmonic energy can degrade the performance of some kinds of mixers.

SINE WAVE SYNTHESIS USING HIGHER FREQUENCIES

Description of the blocks:

In the first method, it has been shown in Fig. 1 that the main blocks of this system can be classified into :

A. Crystal Oscillator

B. Variable Frequency Oscillator

C. Buffers and Amplifiers

D. Mixer

E. Filter

F. Automatic Gain Control

G. Digital to Analog Converter

H. Microprocessor

The blocks are taken below one at a time for analysis.

OSCILLATORS

Crystal Oscillator:

The object of having a crystal oscillator is to obtain a constant frequency output at a convenient value. Here, this value has been chosen as 6 M Hz. Any oscillator configuration with R,L,and C could have been chosen but the pitfall is that the output frequency would not be constant. Hence, the use of a crystal in the oscillator circuit.

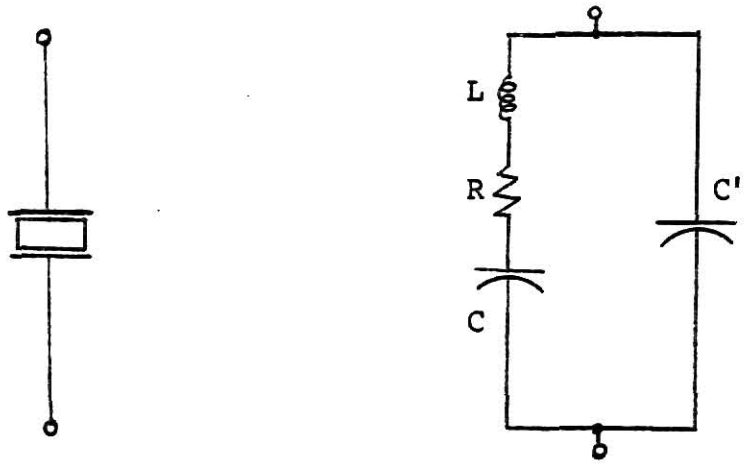
The frequency of oscillation of a vibrating mechanical system is often much sharper than the operating frequency of a resonant electrical combination consisting of a capacitor and a coil [1]. Resonant systems are often described in terms of their quality or Q. Q is the ratio of the energy stored per cycle to the energy dissipated per cycle of oscillation. It can be generally said that a high Q system has a very sharply defined resonant frequency at which response is very good. It also takes approximately Q cycles for a resonant system once excited to have its vibrations die down significantly in amplitude. The Q of a vibrating quartz crystal can be several hundred thousand whereas the Q of a good electrical circuit may be just a few hundred. Thus, if a required frequency is to be accurately controlled and sharply fixed, then it should be controlled in frequency by the vibrations of a quartz crystal.

The most common system used to impart their frequency to an electrical oscillator, is a vibrating quartz crystal, even though various mechanical resonant systems can be used. Such a crystal is

piezoelectric, which means that an electrical signal applied to metal electrodes on the crystal will cause a mechanical deformation of the crystal, and conversely a mechanical deformation of the crystal will result in an electrical signal. To an input AC signal such a crystal appears as an electrical resonant circuit connected in parallel with the actual electrical capacitance of the crystal and its mounting. Quartz is the most commonly used material for a piezoelectric crystal. It has electrodes plated on opposite faces and if a potential is applied between these electrodes, forces will be exerted on the bound charges within the crystal. In a properly mounted device deformations take place within the crystal and an electromechanical system is formed which vibrates when properly excited. The crystal dimensions, the orientation of the surfaces with respect to its axes, and the way in which the device is mounted determine the resonant frequency and the Q of the device. Frequencies ranging from a few kilohertz to a few megahertz, and Qs in the range from several thousand to several hundred thousand are commercially available. The extrordinary high values of Q and the fact that the characteristics of quartz are extremely stable with respect to time and temperature account for the exceptional frequency stability of oscillators incorporating crystals.

The electrical equivalent circuit of a crystal is indicated in Fig. 4. The inductor L, capacitor C, and resistor R are the analogs of the mass, the compliance (reciprocal of the spring constant), and the viscous-damping factor of the mechanical system. The electrostatic capacitance between electrodes with the crystal as the dielectic is represented by C', and its magnitude is very much larger than C.

Neglecting the resistance R, the impedance of the crystal is a



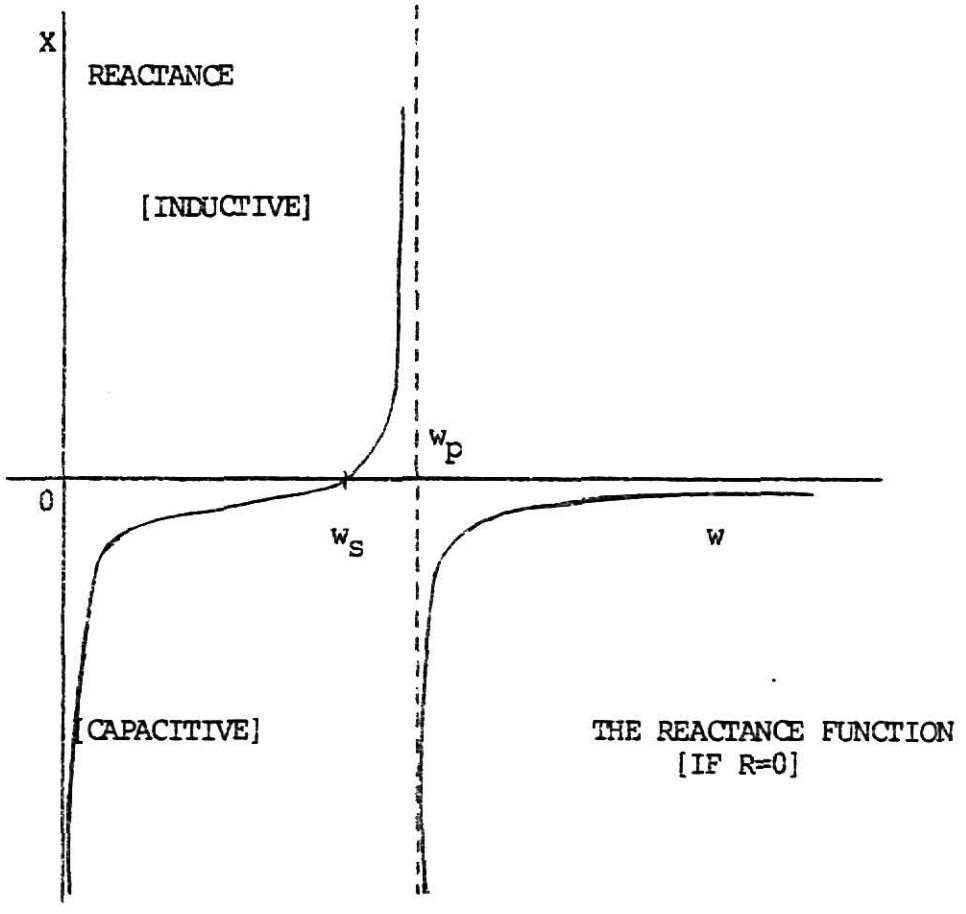


Fig. 4

Crystal Oscillator

reactance jX whose dependence upon frequency is given by

$$jX = \left(\frac{j}{wC'}\right) \frac{w^2 - w_s^2}{w^2 - w_p^2}$$

where $w = \frac{1}{\sqrt{LC}}$ is the series resonant frequency, also known as the zero impedance of frequency, and $w = \left(\frac{1}{L}\right)\left(\frac{1}{C} + \frac{1}{C'}\right)$ is the parallel resonant frequency, also called the infinite impedance frequency. Since $C' >> C$, then $w_p \tilde{-} w_s$. For $w_s < w < w_p$, the reactance is inductive, and outside this range it is capacitive, as indicated in Fig. 4.

Sinusoidal Oscillators

In Fig. 5 an input xi is supplied to the input terminals of the amplifier which gives an output xo = Axi [1]. The output is fed back through a feedback network and its output is xf = βxo = Aβxi. The output of the mixing network is xf' = -xf = -Aβxi.

$$\text{Hence, the loop gain} = \frac{xf'}{xi} = \frac{-xf}{xi} = -A\beta.$$

If xf' is made equal to xi then the amplifier cannot distinguish the source of the input signal applied to it. Hence, if terminal-2 were connected to terminal-1 after removing the external source of supply, the amplifier will continue to provide the same output signal xo. xf' = xi means that the instantaneous value of xf' and xi are exactly equal at all times. The condition xf' = xi is the same as the loop gain being equal to unity, or that -Aβ = 1. Hence, for a sinusoid the amplitude, phase, and frequency of xi and xf' have to be identical. This is known as the Barkhausen Criterion. The book "Integrated Electronics" by Millman and Halkias states :

"The frequency at which a sinusoidal oscillator will operate is the frequency for which the total shift introduced, as a signal proceeds from the input terminals, through the amplifier and feedback network, and back again to the input, is precisely zero, or an integral multiple of 2π. In other words, the frequency of a sinusoidal oscillator is determined by the condition that the loop gain phase shift is zero."

If the magnitude of the product of the transfer gain of the amplifier and the magnitude of the feedback factor of the feedback network (the magnitude of the loop gain) are less than unity at the oscillator frequency, then oscillations will not be sustained.

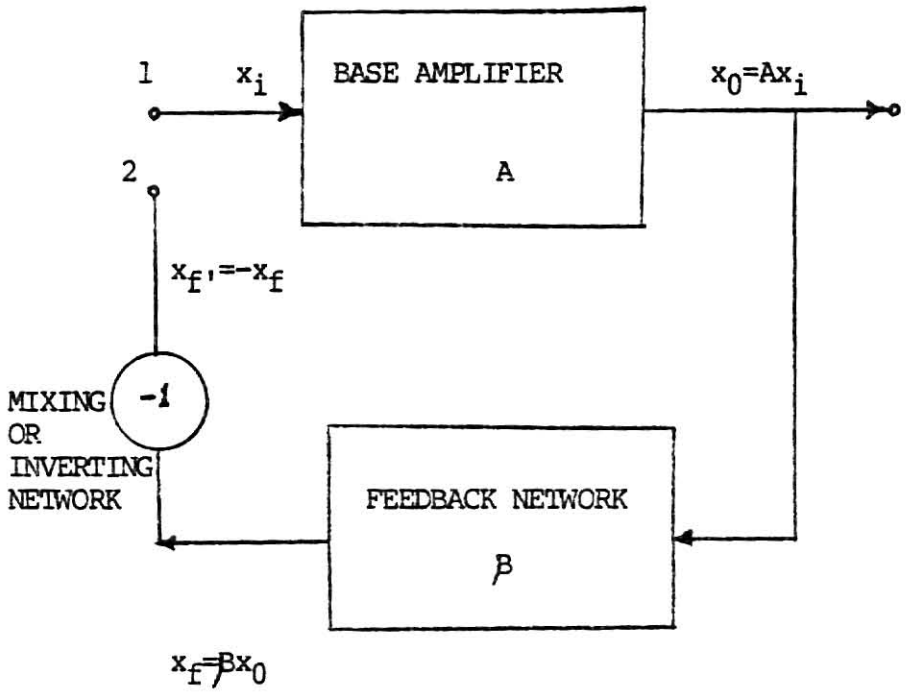


Fig. 5

Feedback Diagram for oscillator analysis.

Due to the restrictions of age, voltage, temperature and operating conditions of the circuit parameters $|A\beta| = 1$ is not practically realisable, and hence $|A\beta|$ will become less or larger than unity. In the former case, the oscillations simply stop, and in the latter case, the amplitude of the oscillations will continue to increase without limit as long as it is not limited by the onset of non linearity of operation in the active devices associated with the amplifier.

Hence, in every practical oscillator the loop gain is slightly greater than unity, and the amplitude of the oscillations is limited by the onset of nonlinearity.

A General form of Oscillator Circuit

Fig. 6 shows the general form that many oscillator circuits fall into [1]. The active device maybe a bipolar transistor, a differential operational amplifier, or an FET. In the analysis below an active device with infinite input resistance is assumed. Fig. 7 shows the linear equivalent circuit of Fig. 6, using an amplifier with negative gain -Av and output resistance Ro. The topology of Fig. 7 is that of a voltage-series feedback.

By considering the circuit of Fig. 6 to be a feedback amplifier with the output taken from terminals 2 and 3 and with the input terminals 1 and 3, the value of the loop gain $-A\beta$ can be obtained. The load impedence ZL consists of Z2 in parallel with the series combination of Z1 and Z3. The gain without feedback is

$$A = -Av\ ZL/(ZL+Ro).$$

The feedback factor is

$$\beta = -Z1/(Z1+Z3).$$

The loop gain is found to be $-A\beta = \dfrac{-Av\ Z1\ Z2}{Ro(Z1+Z2+Z3)+Z2(Z1+Z3)}$.

If the impedances are pure reactances (either inductive or capacitive), then Z1 = jX1, Z2 = jX2, Z3 = jX3. For an inductor, X = wL, and for a capacitor, X = -1/wC. Then

$$-A\beta = \frac{-Av\ X1\ X2}{j\ Ro(X1+X2+X3)-X2(X1+X3)}.$$

For the loop gain to be real (zero phase shift)

$$X1+X2+X3 = 0 \qquad \text{and}$$

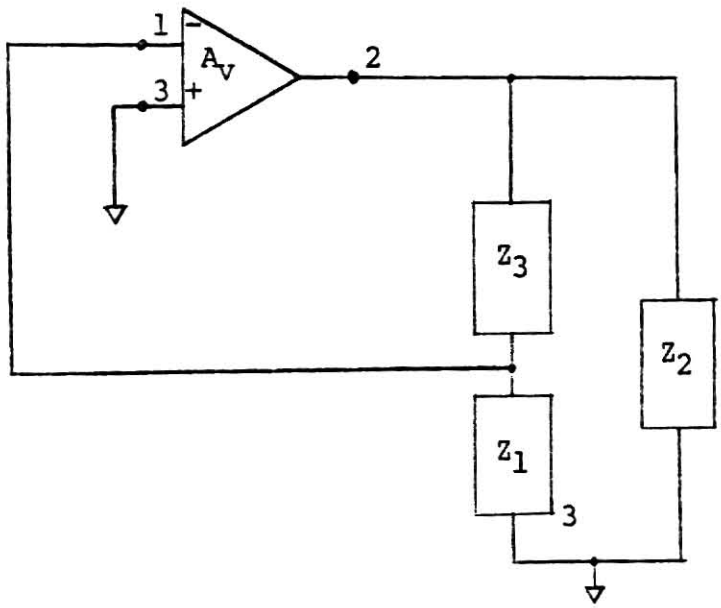


Fig. 6

General form of Oscillator Circuit.

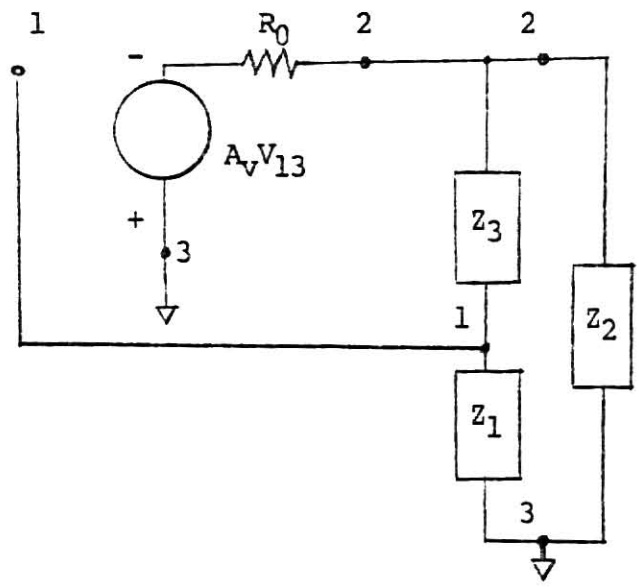


Fig. 7

Equivalent circuit of the general form.

$$-A\beta = \frac{-Av\ X1\ X2}{-X2(X1+X3)} = \frac{-Av\ X1}{X1 + X3}$$

The circuit will oscillate at the resonant frequency of the series combination of X1, X2, and X3.

From the above two equations

$$-A\beta = \frac{+\ Av\ X1}{X2}$$

As Av is positive, X1 and X2 must have the same sign since $-A\beta$ must be positive, and at least unity in magnitude. In other words, they must be the same kind of reactance, either both inductive or both capacitive. From the above equations therefore, X3 = -(X1+X2) must be inductive if X1 and X2 are capacitive and vice versa.

If X1 and X2 are capacitors and X3 is an inductor, the circuit is called a "Colpitts oscillator". If X1 and X2 are inductors and X3 is a capacitor, the circuit is called a "Hartley oscillator".

Normally many oscillator configurations can be obtained with just resistors and capacitors which give a reasonably good output. If a variation in the output frequency is being considered at higher frequencies it has been found that the use of inductances provides for better flexibility.

In spite of all the design precautions and care taken for building oscillators, it has been found that out of a few different circuits tried out only one particular circuit functions very well for the present requirement, and that too under specific conditions. After a few trials with different circuits the circuit finally chosen, tested and used here is as shown in Fig. 11. Particular precaution has had to be taken to see that the oscillator was built in a compact fashion.

Precaution has also been taken to setup the ground points of the circuit together.

The Colpitts oscillator configuration was found to be the best suited for the present application. Fig. 8 shows the general setup of the Colpitts oscillator. Here the resistors R1 and R2 are not entirely negligible for low frequencies and may have several degrading effects, but can be conveniently neglected at higher frequencies. At low frequencies they may increase the effective resistance of the crystal branch of the circuit, thus reducing its Q in addition to decreasing the loop gain. They may also cause relaxation-type oscillations under certain conditions. Both of these problems maybe reduced by using field effect transistors, but an FET does not give temperature stability and hence is not used here.

The Colpitts oscillator can be thought of as an emitter-follower and a capacitive tapped tank circuit, as shown in Fig. 9. If capacitors C1 and C2 are large enough so that the input and output impedance of the transistors are effectively swamped, and if the crystal resistance Re is small, then the ratio of the tank circuit is

$$\frac{e2}{e1} \simeq \frac{X1 + X2}{X2}$$

with voltages e1 and e2 in phase.

The input impedance can be written from Fig. 10 as

$$Z1 = \frac{j\,X2(Re+jX1+jXe)}{jX2+jX1+jXe+R2.}$$

Assuming $X1+X2+Xe = 0$, the input impedance is

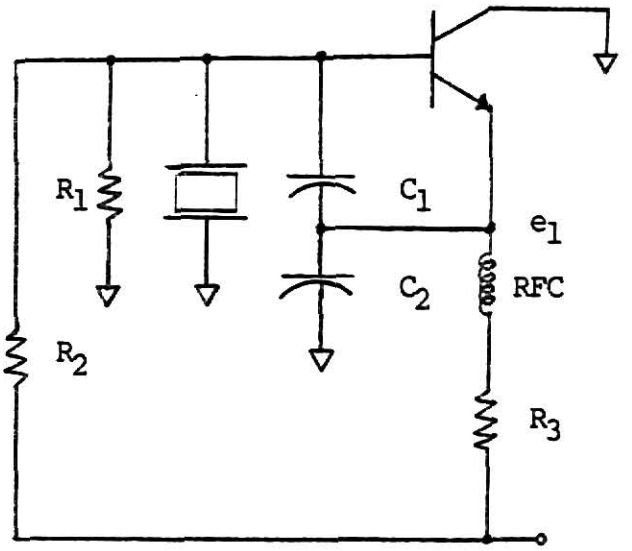


Fig. 8

Schematic diagram of the Colpitts Crystal Oscillator.

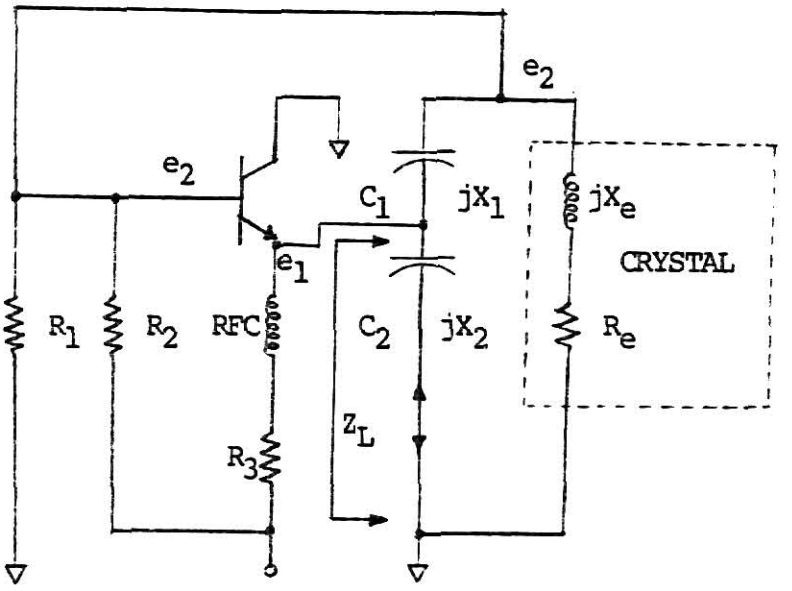


Fig. 9

Signal flow diagram of the Colpitts Oscillator.

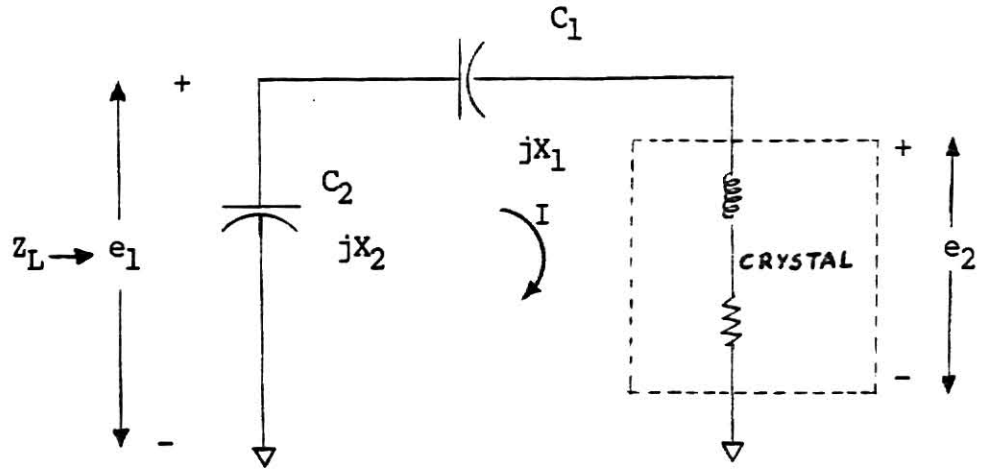


Fig. 10

Simplified diagram of the Colpitts oscillator phase shift circuit.

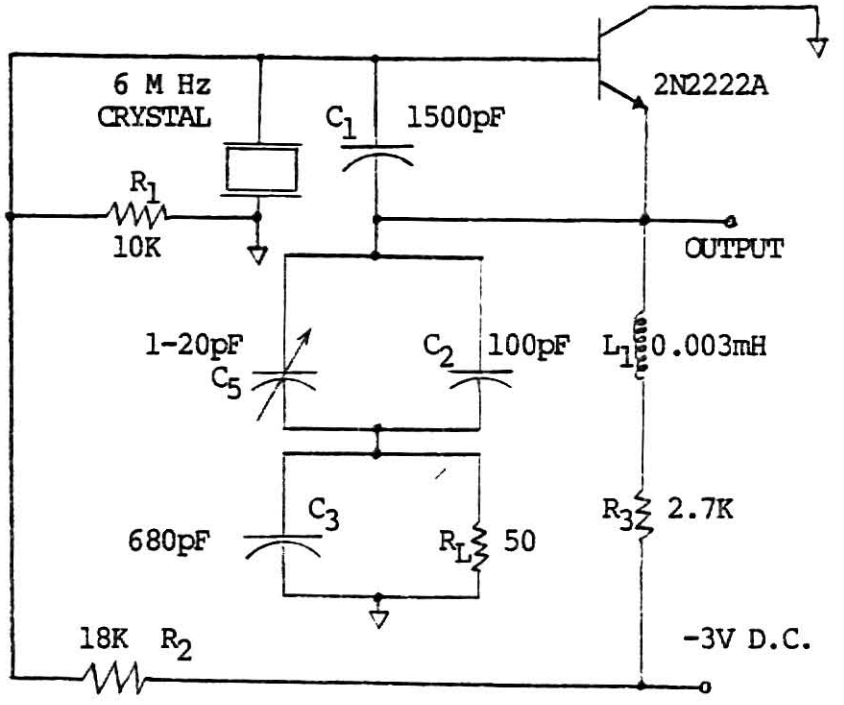


Fig. 11

Schematic diagram of 6 M Hz Colpitts oscillator.

$$Z1 = \frac{-X2(X1+Xe)+jRe\ X2}{Re}$$

Again applying the same assumption

$$Z1 = \frac{X2(X2+jRe)}{Re}$$

If it is assumed that X2 >> Re, then

$$Z1 = \frac{X2^2}{Re.}$$

The voltage e2 maybe written as

$$e2 = I(Re+jXe)$$

where

$$I = \frac{e1}{jX1+Re+jXe.}$$

Combining the above

$$\frac{e2}{e1} = \frac{Re + jXe}{Re + jX1 + jXe.}$$

If it is again assumed that X1 + X2 + Xe = 0, then Xe = -(X1+X2) and X2 = -(X1+Xe). Substituting these gives

$$\frac{e2}{e1} = \frac{Re - j(X1+X2)}{Re - jX2.}$$

Assuming now that Re << X2 and Re << X1, then

$$\frac{e2}{e1} = \frac{X1 + X2}{X2.}$$

For this to be true, the crystal has to be resonant with the series combination of C1 and C2. Therefore, it is seen that the load

seen by the emitter-follower is

$$Z1 = \frac{X2^2}{Re}$$

and is purely resistive. The gain of the emitter-follower is

$$A = \left\{\frac{e1}{e2}\right\} = \frac{gm\ Z1}{1 + gm\ Z1.}$$

Since Z1 is resistive, the phase shift through the emitter-follower is zero, and the phase shift of the entire loop is zero. If the loop gain exceeds unity then the circuit will oscillate. This is true if

$$\frac{e2}{e1} A >= 1.$$

Substituting for A and e2/e1

$$\left\{\frac{gm\ Z1}{1 + gm\ Z1}\right\} \left\{\frac{X1 + X2}{X2}\right\} >= 1.$$

Substituting for Z1

$$\left[\frac{gm\ X2^2/Re}{1 + gm\ X2^2/Re}\right] \left[\frac{X1 + X2}{X2}\right] >= 1.$$

But simplifying this gives

$$gm\ X1\ X2 >= Re.$$

Since the crystal must be resonant with the series combination of C1 and C2, the crystal reactance can be calculated using the equation X1 + X2 + Xe = 0, where Xe is the crystal reactance.

This analysis is limited by the assumption made. When an

experimental approach was used for designing the Colpitts oscillator the following guidelines were used [4] :

a. C1 and C2 should be as large as possible but still allow the circuit to oscillate with two to three times the maximum permissible crystal resistance. If this results in the crystsl reactance, Xe being smaller than that of the specific load capacity, a trimmer capacitor maybe placed in series with the crystal to trim the crystal onto frequency.

b. It is desirable to let |XL| << 1/goe and |X1| << 1/gie. This minimises the effect of transistor input and output conductances on the circuit. Best stability also occurs if C1 and C2 are as large as possible because they swamp out any change in the transistor capacitances. From Fig. 8 it can be seen that the resulting reactance of the crystal and a series trimmer will be smaller if C1 and C2 are large, thus minimising the shunt effect of R1 and R2.

The circuit used based on the above design is shown in Fig. 11. It is to be noted that the crystal is used as an inductor in this oscillator circuit, and should be operated in the region of its characteristic where it behaves as an inductor. When building a circuit for higher frequency values with a higher frequency crystal, the capacitance values will have to be reduced. A longer wire behaves as an inductor and may introduce quite a bit of inductance error when not required (as for a capacitance). This point should be particularly noted while building an oscillator since the circuit may not oscillate, or may oscillate at a totally different frequency than what is required.

It is found that the circuit of Fig. 11 functions satisfactorily

as per the present requirement giving a stable sine wave output at 5.998 M Hz. with an amplitude of 1.1 V peak to peak without distortion. Any variation to try to increase the amplitude tends to distort the waveform. The values of the components here have been chosen on an experimental basis and function very well for this requirement.

Fig. 12 shows a variable frequency oscillator, wherein the variation is obtained by varying the variable capacitance in the LC section of the circuit. This type of oscillator can be made very stable by using polystyrene capacitors in the frequency determining part of the circuit. These variable frequency oscillator circuits can be scaled to other operating frequencies by using the values shown to determine the reactance of the capacitors.

In spite of winding the coil as per calculations it is sometimes found that the experimental determination of the number of turns on the coil yields the best results as required. By variation of the capacitance in the frequency determining part of the circuit it has been found that a variation over almost one full M Hz, from 5 M Hz to 6 M Hz is possible with very good resolution. This is hence very useful in the application for measurements in the instrumentation laboratory.

Moreover, the reason for selecting this configuration with variable capacitors in the picofarad range is because of the further application of this circuit. The capacitors can be replaced by varicaps which can conveniently be varied by a variation in the analog voltage, which would be the output of the digital to analog converter as shown in Fig. 1. Hence, the varicaps in the variable frequency oscillator circuit will be the variable parameters in the automated system for

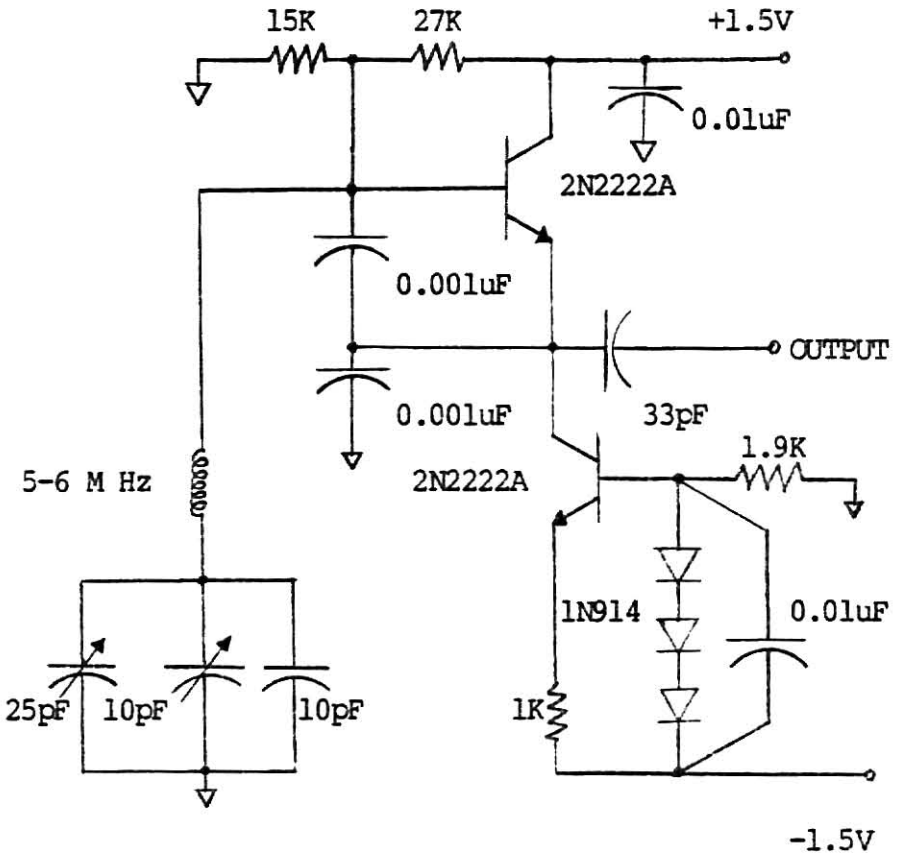


Fig. 12

Colpitts Variable Frequency Oscillator.

frequency control.

At present, the variable capacitors are controlled manually for variations in frequency.

BUFFERS AND AMPLIFIERS

The objective of having buffer stages in the oscillator circuit is to connect the signal from the output of the oscillator to the amplifier input without loading the oscillator output. The strength of the output waveform of the oscillator not being sufficient to drive the mixer, amplifier stages have to be used.

In a buffer circuit the output follows the input. It has a high input impedance, very low input current, and very low output impedance. These are the qualities required here for the stage between the oscillator and the amplifier.

For designing a buffer, a suitable operating collector current for the transistor is assumed in order to provide the output swing. The emitter resistance is then so chosen that the emitter voltage is approximately half the supply voltage to the transistor. The biasing network resistances are then chosen so that they provide the necessary base current for linear operation of the transistor. Next, the coupling capacitors are so chosen that they provide a negligible reactance at the frequency of operation.

When much higher input impedances are required than those that can be got by an emitter follower network, a bootstrap network is used as is the case with the crystal oscillator network shown in Fig. 13.

The buffer network shown in Fig. 15 is used between the mixer and the filter stage to avoid loading the mixer output.

For designing the amplifier, the required operating collector current is again chosen. The collector resistance is chosen so that the

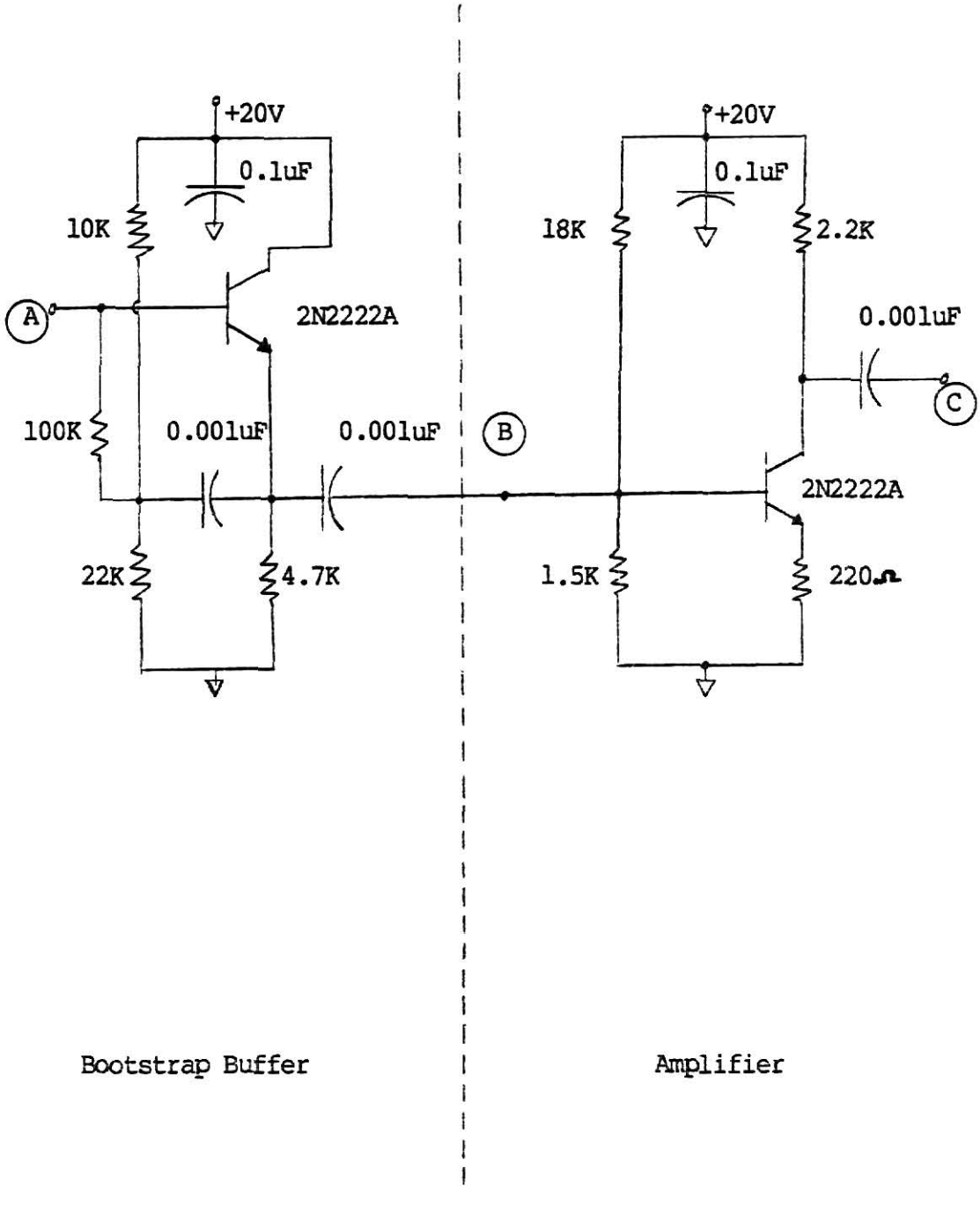


Fig. 13

Buffer and Amplifier circuits for the Colpitts Oscillator.

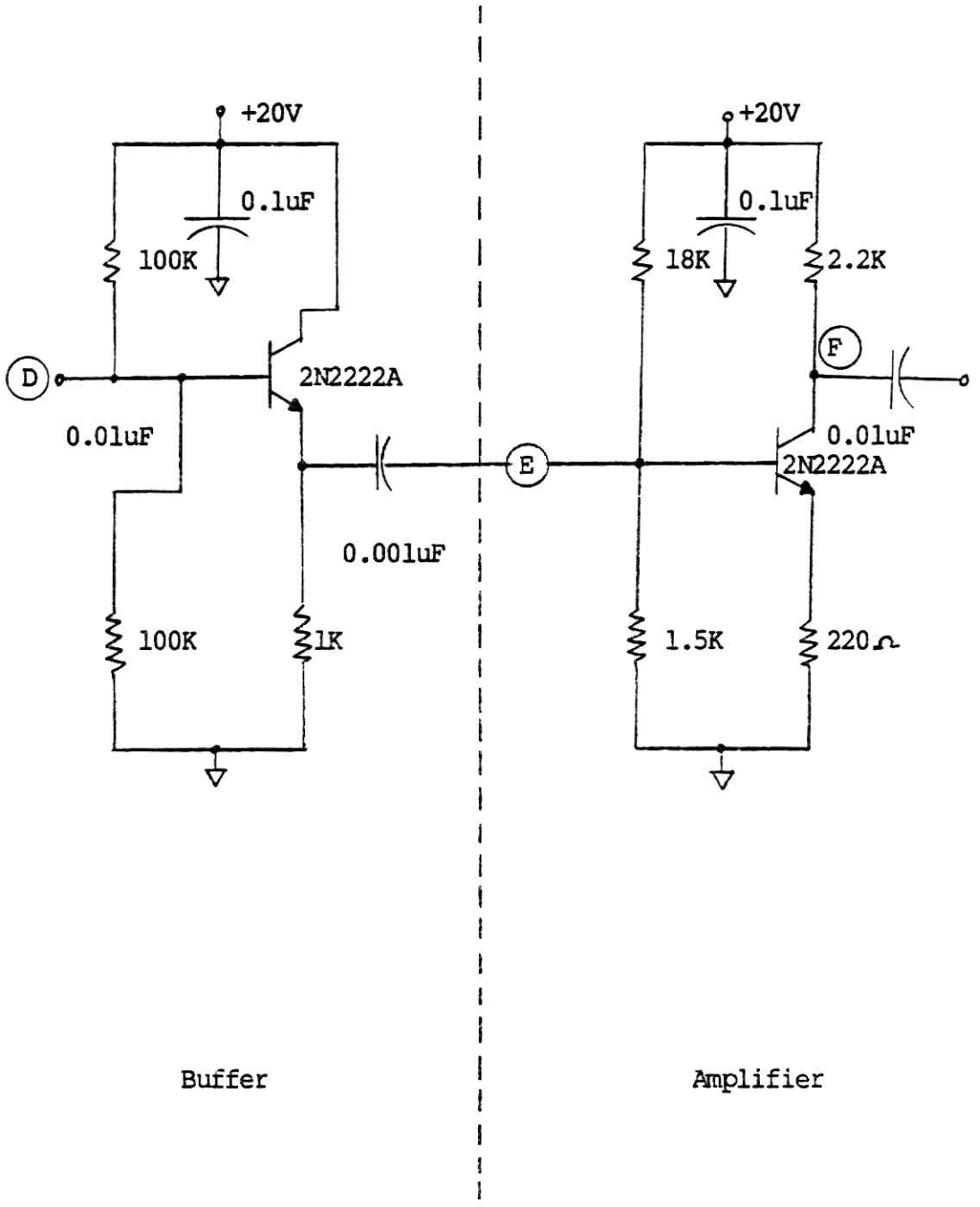


Fig. 14

Buffer and Amplifier circuits for the Variable Frequency Oscillator.

collector is biased at approximately half the value of the supply voltage to the amplifier. If negative feedback has to be used, then the emitter resistance is chosen so that the stage gives the required gain. The biasing network is designed so that the required base current is got for linear operation. The coupling capacitors are again chosen so that they have negligible reactance at the frequency of operation.

Mica or ceramic capcitors have to be used between the ground points and the points where the supply is connected to the amplifiers and the buffers to avoid any noise pickup or distortion due to interference during the passage of the signal through the stage. Ceramic capacitors of 0.1 uF value were found to be good enough in the circuits used.

Fig. 13 shows the crystal oscillator buffer followed by the amplifier, and Fig. 14 shows the variable frequency oscillator buffer followed by its amplifier. The amplifier and buffer configurations have been so chosen as to amplify the waveforms without distortion of the signal in the required range of operation. The design and implementation of the variable frequency oscillator amplifier had to go through sufficient number of changes to accommodate the frequency variation from the variable frequency oscillator which also causes a variation in the amplitude of the output waveform.

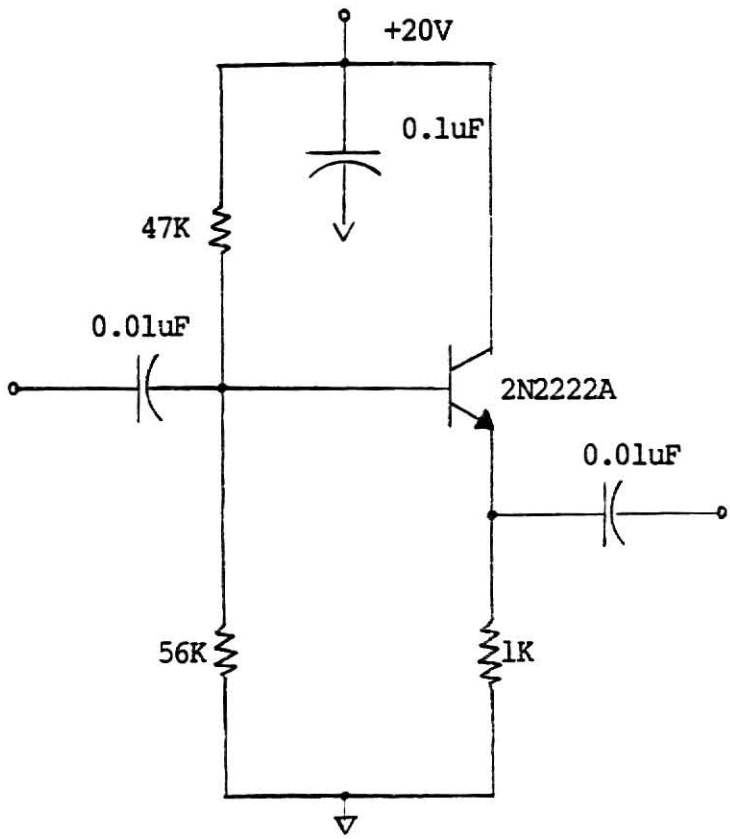


Fig. 15

Buffer between the mixer and filter stages.

MIXER

One of the most important parts of this synthesizer is the mixer [2]. It is at this point where the greater consideration for dynamic range exists. For best overall performance, the mixer should receive only enough preamplifier signal to overcome the mixer noise. There will be desensitization and other effects when excessive amounts of signal energy are permitted to reach the mixer which can render the mixer useless. Hence a 'strong mixer' can be utilised which can handle high signal levels without being adversely affected. Field effect transistors are preferred over bipolar transistors in this design.

A suitable filter is used after the mixer stage to reject the unwanted mixer products that fall outside the passband of the filter. Care should be taken to keep the noise level at a minimum. Excessive noise will appear as noise sidebands in the output.

The symbolic representation of a mixer [5] is shown in Fig. 16 with two inputs and one output. One is usually a larger input as compared to the other. The output frequency f_0 is also called the intermediate frequency. In many applications of the mixer, as this one, the mixer intermediate frequency port is very wide in frequency response, sometimes covering several octaves.

If the two input frequencies f_1 and f_2 are assumed to be constant single tone inputs at any instant of time, there will be two possible intermediate frequency outputs. One is the sum of the input frequencies and is termed the upper sideband, while the other is the difference frequency, called the lower sideband.

The only outputs of interest are the sum and difference frequencies in normal mixer applications. The other outputs that may occur are then termed spurious outputs. These will include the frequencies f_1 and f_2 as well as their harmonics. The harmonics may be present in the input signals or they may be created by high order curvature in the transfer function of the mixer. Other spurious outputs will be at frequencies that are the sum or difference of harmonics of the input frequencies. If the inputs are f_1 and f_2, possible outputs are $f_0 = nf_1 \pm mf_2$ where m and n are both integers from 0 upward. The magnitude of the spurious responses will be different for various mixer types. The responses always decrease as m and n become large. However, the rate of decrease maybe small for some mixers.

Considering the relationship between voltage and current in a linear resistance the equation can be written as

$$i = bv$$

where i is the current, v the voltage, and b a constant of proportionality which, in this case, is conductance [10]. Considering a bipolar transistor if i be the collector current, and v the base voltage for a class A amplifier, a DC component of collector current 'a' is also present, where a is independent of the signal voltage at the base. Hence the equation now becomes

$$i = a + bv$$

Fig. 17 shows a nonlinear characteristic say, of a nonlinear resistance. The linear relationship holds only upto point x on the graph after which the current either saturates when c becomes negative or there is some kind of avalanche multiplication where c becomes more positive. Hence, the current now becomes proportional to the voltage,

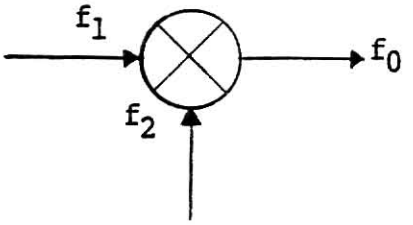


Fig. 16

Symbolic representation of a Mixer.

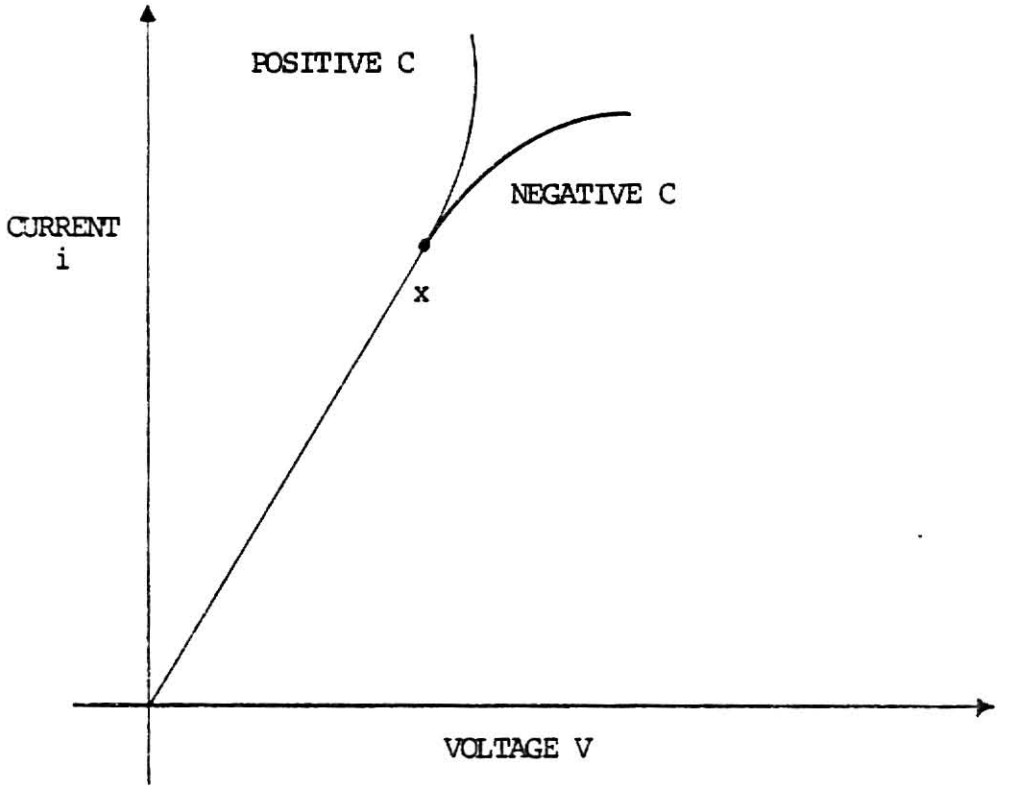


Fig. 17

Nonlinear Resistance Characteristics.

its square, cube, and also the higher powers. The nonlinear relationship can hence be written as

$$i = a + bv + cv^2 + dv^3 + \text{higher powers.}$$

As c is much smaller than b in practice, at lower values of v, the graph is linear. Actually, only the square term is large enough to have any effect in most applications. So, the equation can now be written as

$$i = a + bv + cv^2$$

where c is the constant of nonlinearity.

This equation can effectively be used for the gate voltage–drain current characteristic of a field effect transistor. Considering the simultaneous application of two sinusoidal input voltages $u = U \sin pt$ and $v = V \sin qt$ to the gates of the field effect transistor,

$$\begin{aligned} i &= a + b(u+v) + c(u+v)^2 \\ &= a + b(u+v) + c(u^2+2uv+v^2) \\ &= a + b(U \sin pt + V \sin qt) \\ &\quad + c(U^2 \sin^2 pt + 2UV \sin pt \sin qt + V^2 \sin^2 qt) \end{aligned}$$

Since $\sin x \sin y = 1/2[\cos(x-y) - \cos(x+y)]$ and

$\sin^2 x = 1/2\ (1 - \cos 2x)$

by simplification,

$$\begin{aligned} i &= a + bU \sin pt + bV \sin qt + 1/2\ cU^2\ (1-\cos 2pt) \\ &\quad + 1/2\ cV^2(1-\cos 2qt) + cUV\ [\cos(p-q)t - \cos(p+q)t] \\ &= (a+1/2\ cU^2+1/2\ cV^2) + (bU \sin pt) + (bV \sin qt) \\ &\quad - (1/2\ cU^2 \cos 2pt + 1/2\ cV^2 \cos 2qt) \\ &\quad + [cUV \cos (p-q)t] - [cUV \cos (p+q)t] \end{aligned}$$

The above equation clearly shows that the output of a field effect transistor mixer mixing two sine waves has the following for its output :

a. DC component term,

b. the first input waveform term,

c. the second input waveform term,

d. harmonics of the two waveforms,

e. the lower sideband voltage, and

f. the upper sideband voltage.

The frequencies of interest in the output are only the lower sideband voltage terms and these will have to be seperated from the rest with the help of a suitable filter.

Fig. 18 shows the circuit diagram of the mixer used for the frequency synthesizer. As mentioned earlier, a MOSFET has been chosen as the active element of the mixer. The two input signals are fed in through the two gates G1 and G2, and the output is seen at the drain, D. The larger input from the crystal oscillator amplifier is fed to G2, and the smaller input of lower amplitude fed to G1 from the variable frequency oscillator amplifier. For the mixer to function properly and give well modulated outputs over the entire range of interest the amplitudes of these two inputs had to be specific values. Experimentally it was found that the supply voltage for the crystal oscillator had to be -3.0 V DC , and the supply voltage for the variable frequency oscillator had to be ± 0.15 V DC. Variations in these values would cause the input at G1 to get modulated, which is not a desirable condition as it would distort the mixer output. Keeping the above values fixed the mixer output would give a well modulated waveform as shown in Fig. 19. Fig. 20 shows the spectrum analyser display for such a mixed output.

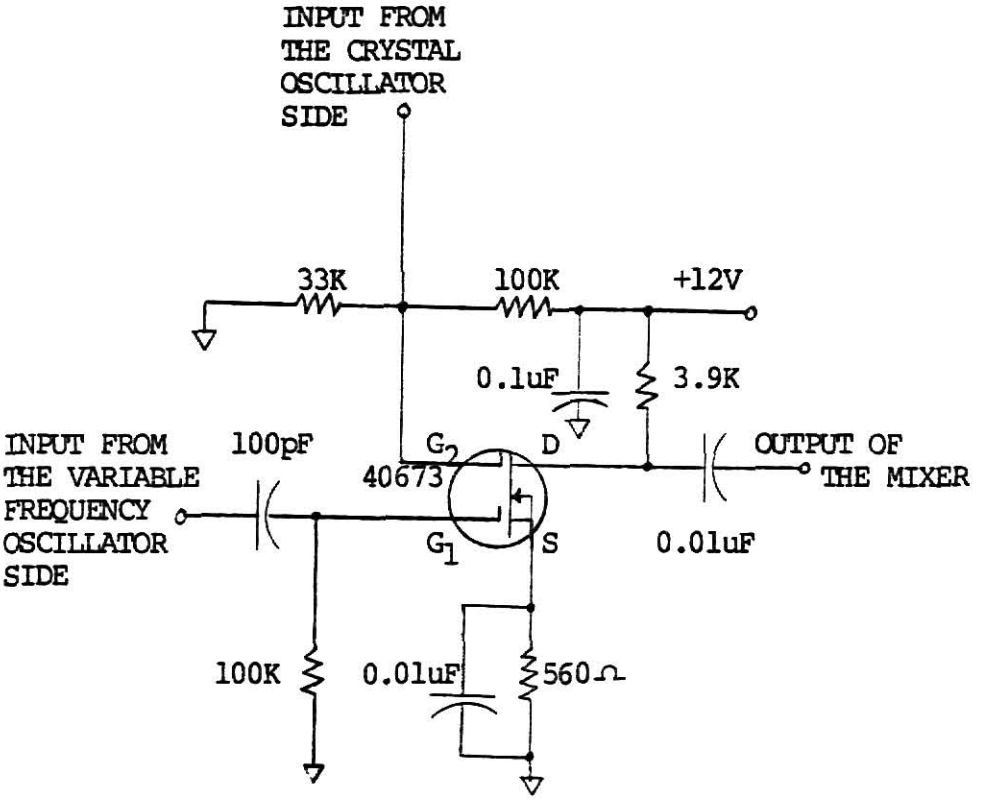


Fig. 18

Schematic diagram of the practical Mixer circuit.

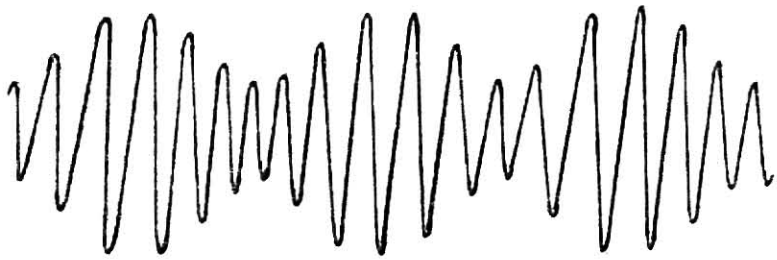


Fig. 19

Modulated output waveform of the mixer.

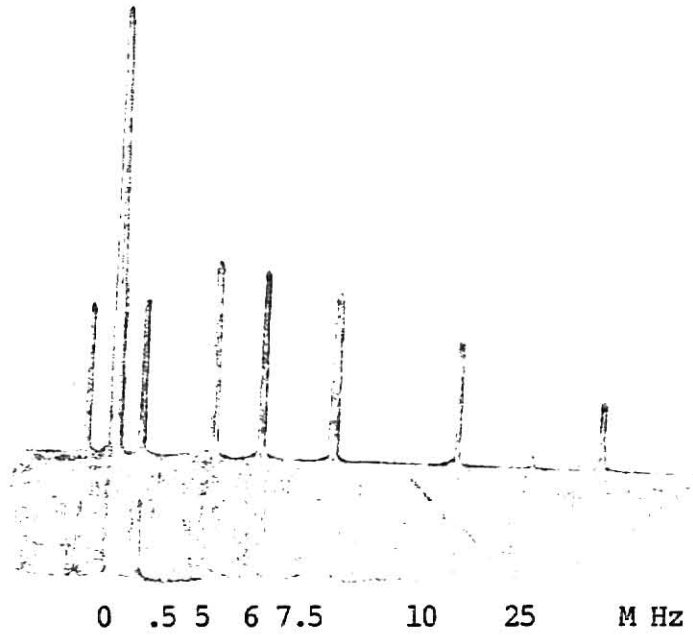


Fig. 20

Spectrum Analyzer display for the mixer output.

NOISE REDUCTION

While working with circuits involving higher frequencies the importance of noise reduction and reduction in interference from other parts of the circuit is very clearly seen. Fig. 21a shows the waveform as seen on the oscilloscope at the output of the variable frequency oscillator amplifier before using the grounding and shielding techniques. Fig. 21b shows the same point after the power supply ground was connected to the power supply chassis ground. Fig. 21c shows the waveform after all the shielding techniques were used. It was found during the work on the synthesizer that the 6 M Hz frequency from the crystal oscillator was interfering with the variable frequency oscillator output, distorting it, which in turn was distorting the output of the mixer circuit. Once the system was properly shielded and grounded, the mixer output was found to be well modulated, as was to be expected from two properly mixed signals.

In quite a few electronic systems, the DC power supply and distribution systems are common to many other circuits [11]. Hence, care must be taken to see that the DC power system does not become a channel for noise coupling between the circuits connected to it. The best solution to such a problem is to have individual power supply units supplying different sections of the circuit with separate ground points. Also, any AC signal generated by the load should not generate an AC voltage across the DC power bus. Even though a power supply is ideally a zero impedance source of voltage, in practice the power supplies do have some impedance and represent a source of coupling

Fig. 21a

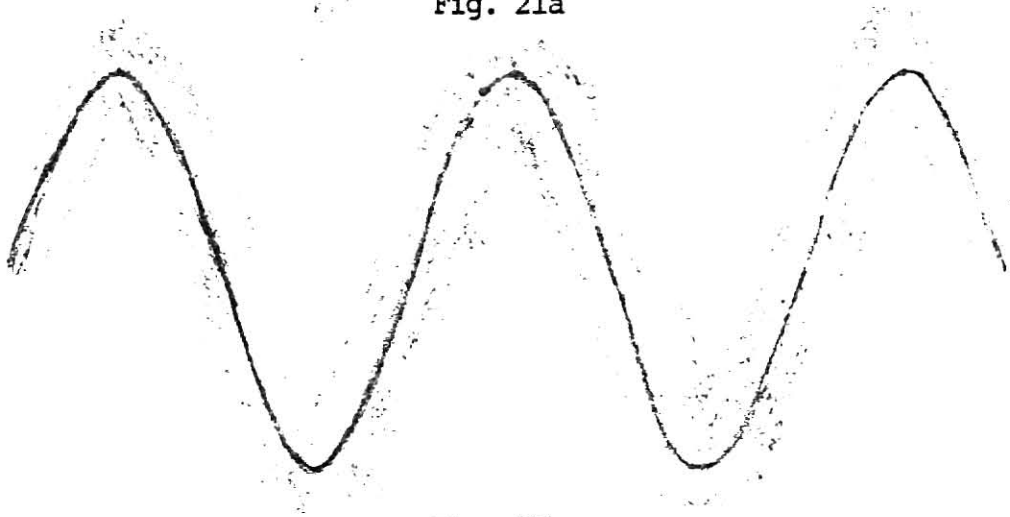


Fig. 21b

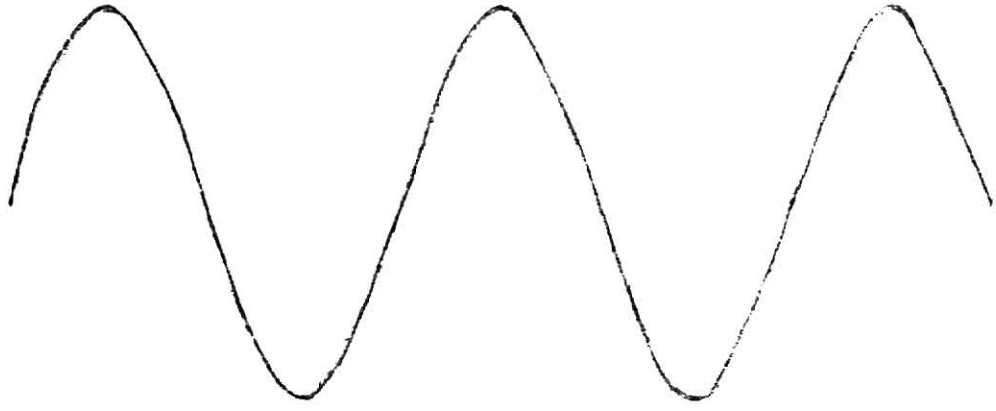


Fig. 21c

Noisy and clear waveforms before and after shielding.

between the circuits using them. Not only do the power supplies have finite impedances, the conductors used to connect them to the circuit add to these impedances. Filtering techniques have to be used to reduce the noise pickup and the coupling. For best noise performance, the power transmission line should have as low a characteristic impedance as possible, which in turn means that it should have a high capacitance and low inductance. When the same power supply is used to supply more than one section of the circuit, supply to the sections can be decoupled by using decoupling filters.

To prevent high frequency or noisy circuits from radiating noise or from interfering with other sections of the circuit, metallic enclosures are used as shields. All the leads entering or leaving the shielded enclosure should be filtered for the shield to be effective, so that they do not conduct noise out of the shield. At high frequencies special care has to be taken to ensure the effectiveness of the filter. Shielding has been found to be very effective. The power supply leads wound on a toroidal core with sufficient number of turns at the circuit end are placed in the shield. Mica or ceramic capacitors, with short leads, should be connected between the power supply connection and the ground at the circuit end. For the other leads leading out of the shielded enclosure, shielded conductors with their shields grounded at one end, can be used. This prevents the noise pick-up by the conductors.

Ground loops are sometimes the most difficult to analyse or trouble-shoot among the electrical connection problems involving more than one power supply. One of the most important factors to be kept in mind is that the ideal concept of a single, quiet ground potential is

incorrect and misleading. No two ground points have exactly the same potential. Even though the potential differences in most cases is small, they maybe sufficient to cause a few amperes of current flow in the ground loop. Normally, at low frequencies, a good method is to have only one ground return point in a power supply system which includes the power supply, all its loads, and all the other power supplies connected to the same loads. In the case of circuits like the present one involving high frequencies, each power supply should be individually grounded, and sections of a circuit with one ground have to be isolated from the other sections which have a different ground connection. Sections of the circuit that are shielded to avoid interference should be properly connected to the ground. An electrostatic shield enclosure, to be effective, should be connected to the zero signal reference potential of its circuitry.

For the frequency synthesizer, the variable frequency oscillator circuits and the crystal oscillator circuits have been separately shielded. The layout of the circuit is of high importance in high frequency circuits. The ground points have to be brought together and connected to a single point in what is known as the star connection. The leads of all the capacitors have to be short to avoid noise pickup. The circuit itself has to be compactly packed in as small a space as possible. All these points have been taken care of while building the synthesizer. The shields of the circuits have been connected to the zero signal reference potential points individually. Fig. 22 shows the layout of the shielding procedure used.

Some of the salient points that should be looked into to reduce

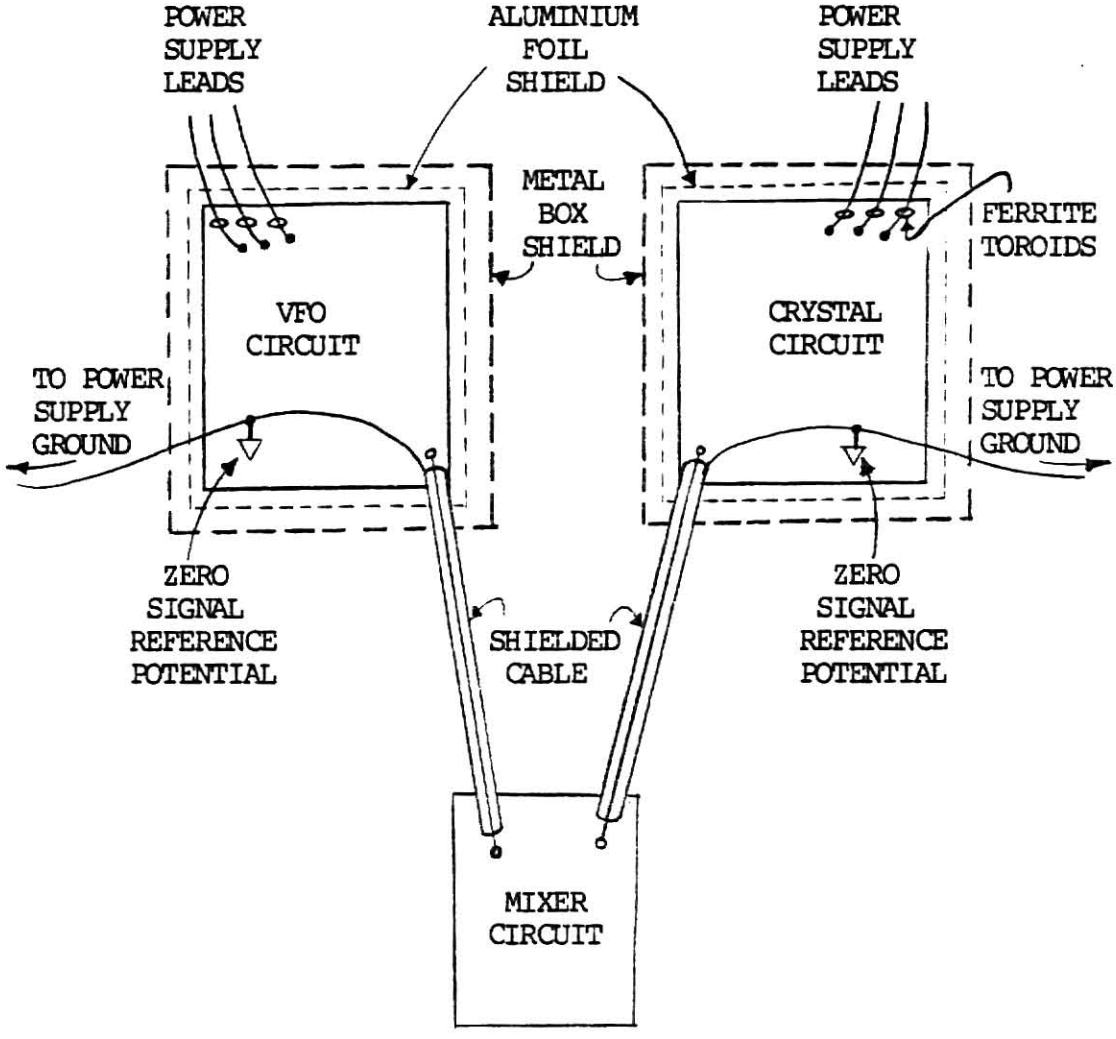


Fig. 22

Layout of the Shielding and Grounding procedures used.

noise and spurious output signals for high frequencies are listed below.

a. A multipoint ground system should be used. In high frequency circuits even a single ground loop can cause some current to flow in it which would interfere with the signal of interest. Hence, each section of the circuit should be separately grounded.

b. The basic objectives of a good ground system are: to minimise noise voltages from more than one ground current flowing through a common impedance, and to avoid generating ground loops.

c. Noise sources should be enclosed in a shielded enclosure.

d. All leads leaving a noisy environment should be filtered.

e. Noisy leads shold be twisted and shielded.

f. The shields should be connected to the zero signal reference potential in that section of the circuit.

g. Shields on signal leads should be insulated.

h. Ground leads should be kept as short as possible.

i. Capacitor leads should be kept short to a minimum.

j. Sensitive portions of the circuit should be shielded.

k. Any leads entering shielded enclosures containing sensitive circuits should be filtered or decoupled.

l. The lengths of sensitive leads should be kept as short as possible.

m. Toroidal inductors maybe used on the power supply lines on entering the shielded enclosure.

Appendix A shows the layout of the final circuit of the

synthesizer. Various relevant points on the circuit have been marked as A,B,C,D,E, and so on. The waveforms following the layout on successive pages in Appendix A show the effect of shielding and grounding at each stage of the circuit. Initially, the circuit was built on a protoboard but after putting all the components together and testing it, the circuit was rebuilt on perforated boards and the components soldered together for compactness and to reduce noise pickup. The circuit was again tested after this and the improvement in the output waveform can be clearly seen in the diagrams in Appendix A.

FILTER

The characteristics of an ideal low pass filter is shown in Fig. 23. Frequencies below the cutoff frequency, f_c, are passed through the filter without attenuation. This region is called the passband. Frequencies above the cutoff frequency are completely attenuated. This region is known as the stopband.

A resistor and capacitor are connected to form a simple low pass filter in Fig. 24. Using the voltage divider property, the frequency domain transfer function using the s plane impedances can be written as

$$H(s) = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + sCR}$$

As $s = -1/RC$, this filter has a pole, but has no zeros. Substituting for $s = jw$ gives the frequency response of this filter which shows that the response decreases as the frequency increases, and also that there is no attenuation at DC. Hence, this is the response of a low pass function.

Fig. 25 shows another network comprising of a series inductor, and a resistor in parallel. Analysing again as above,

$$H(s) = \frac{R}{sL + R} = \frac{1}{1 + sL/R}$$

A single pole at $s = -R/L$ and no finite zeros are the result. Again, there is no impedance at DC, and there is no attenuation. The inductive reactance increases with increase in frequency, increasing the attenuation. The response is again a low pass function.

Fig. 26 shows the sample of a practical low pass response. The

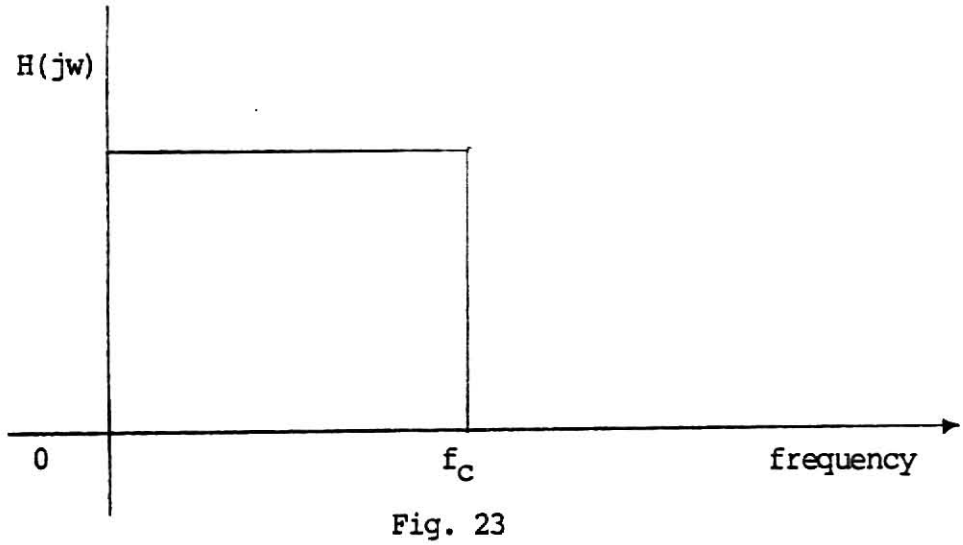


Fig. 23

Ideal Low Pass Filter Characteristics.

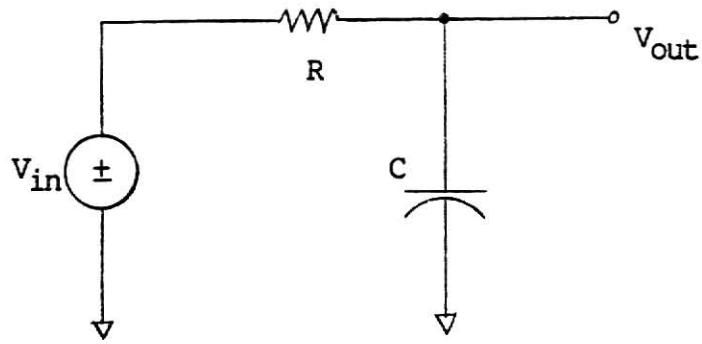


Fig. 24

Simple Low Pass Filter with resistor and capacitor.

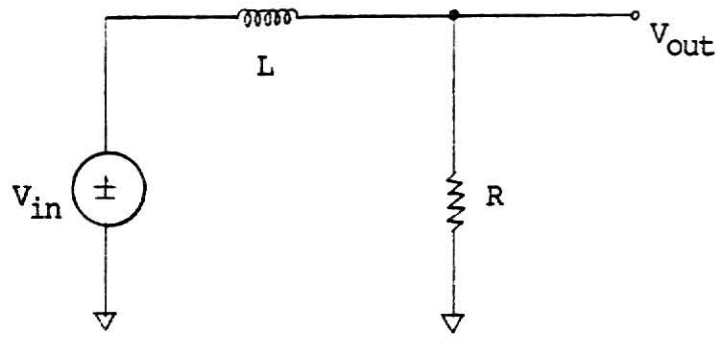


Fig. 25

Simple Low Pass Filter with a Series Inductor.

half power point, or the 3dB point defines the cutoff frequency, f_c. The filter does not have a well defined stop band, which is true of any practical filter.

If the reactive elements in Fig. 24 and Fig. 25 were interchanged with the resistors in their circuits, it would result in high pass filters. Combination of high pass and low pass filters can be used to form band pass, and band stop or band reject filters.

Here, the interest is primarily with building a low pass filter. It has been found that low pass characteristics are obtained from series inductors or shunt capacitors. A composite filter can be built by mixing component types which result in more than one pole in the transfer function analysis, representing the number of reactive components used. An important requirement while building filters is the way in which they are terminated. Impedances and admittances are the points of interest at the terminals of the filter. The filters should function properly with the impedances presented at frequencies in the passband, and should also tolerate the impedances seen in the stopband. For this, filters can be built with ladder configurations which consist of combinations of series and shunt elements.

For building filters an ideal filter is taken as the reference, and based on that suitable approximation methods are used. Attempts are made at choosing filter polynomials which approximate one or the other characteristics of an ideal filter. Normally, the Butterworth and Chebyshev are the popular practical polynomials and filter types used. Both the types have their own advantages and disadvantages. The choice depends on the application. The Butterworth low pass filters have the poles on a circle in the s plane whereas the Chebyshev low pass filters

have them on ellipses. The Butterworth filters are described by circular functions, while the Chebyshev filters are described by hyperbolic functions and are more difficult to analyse. Tables are available with the help of which the above two types of filters can be built. For building a practical low pass filter, it may begin with the first component either being an inductor or a capacitor. The next component in the ladder must be of the other type, and each additional reactive component must be opposite to the previous one. Terminating resistors have to be used for a filter to function as designed. The values of the terminating resistors are quite critical. For the synthesizer, since the operating frequencies are high, active filters are difficult to use and hence filters with passive elements are better suited. Table 1 in Appendix B shows the values of gk, k=1,2,3,4,5 for fifth order filters [5]. For calculating the values of the capacitances and inductances, the formulas to be used from design considerations are:

$$Ck = gk/Rw$$

and

$$Lk = gkR/w$$

where $w = 2\pi f$, f being the 3dB cutoff frequency.

Fig. 27 shows a third order Butterworth LPF (low pass filter) with f = 1 M Hz.

From Table 1 and the above equations the values of the capacitors and inductors are calculated. Fig.28 shows a fifth order Butterworth filter with R = 25 , which was found to be the approximate value of the impedance when looking back into the mixer circuit from the filter. The capacitance and inductance values were again calculated as explained above.

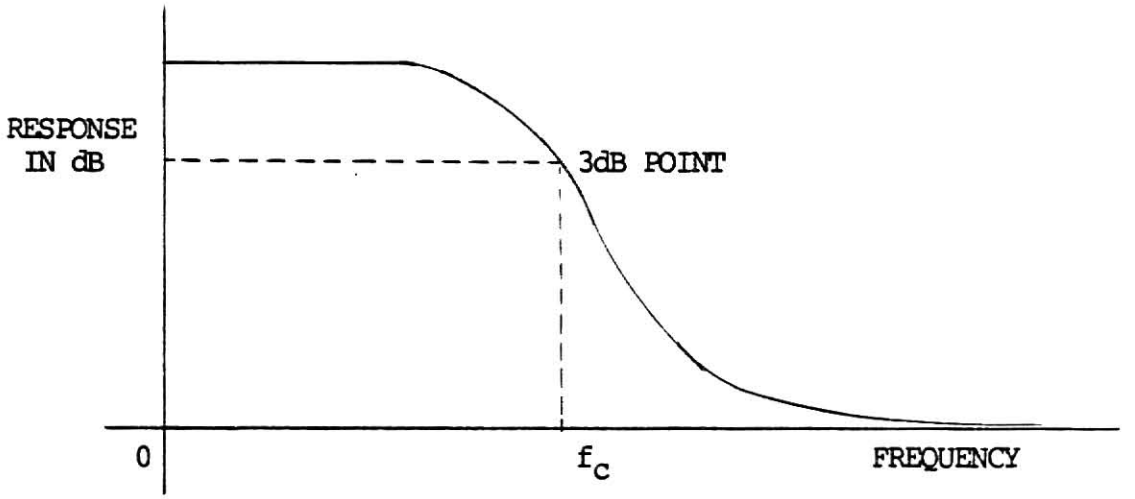


Fig. 26

Practical low pass filter response.

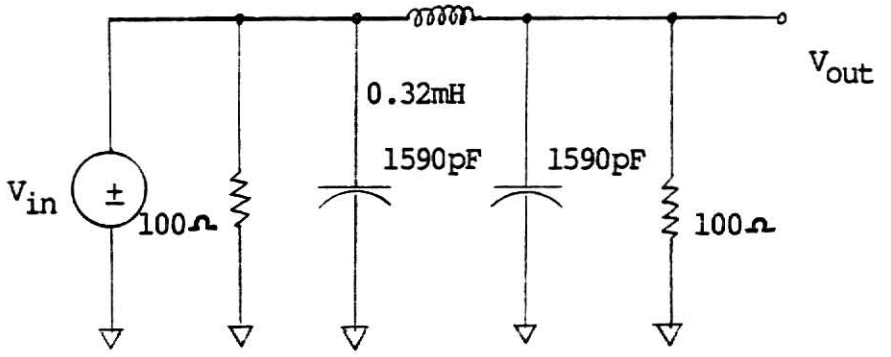


Fig. 27

Third order Butterworth low pass filter.

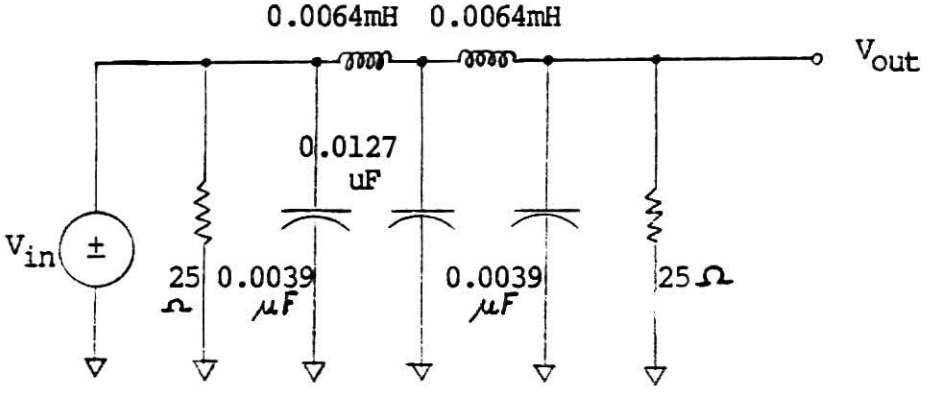


Fig. 28

Fifth order Butterworth low pass filter.

Appendix B shows a computer program in Basic used for calculating the values of the filter parameters on the North Star Horizon computer.

It was found that the output of the filter was not quite satisfactory and this was due to the interference of a high frequency signal on the filter output causing spurious output signals.

After elaborate experimental work a clean sine wave was obtained as the output of the filter in Fig.28 but the drawback was that this output would not vary with a variation in the variable frequency oscillator output. This was due to some ground loops in the circuit which was hard to analyse.

After obtaining a good filter output it would have been found that the amplitude of the output waveform would vary with the variation in frequency. This would need an automatic gain control circuit as the next and final stage of the circuits for the frequency synthesizer.

AUTOMATIC GAIN CONTROL

A simple automatic gain control system is a system by means of which the overall gain of an amplifier circuit is varied automatically with the changing strength of the waveform at the input of this stage. This stage is being used as the last stage in the frequency synthesizer circuit. The input to this stage is the output of the filter stage. It is found that the amplitude of the output waveform of the variable frequency oscillator varies inversely with the variation in frequency. This gets carried on to the filter stage, and hence the need for the automatic gain control to keep the final output waveform to be of a fairly constant amplitude.

The basic principle used for automatic gain control is that a DC control voltage proportional to the strength of the input waveform is used to bias the amplifier into a region of higher AC gain or lower AC gain with the help of feedback. The polarity of the bias voltage is such that the gain decreases as its magnitude increases so that the gain will decrease if the input signal strength increases. This keeps the output waveform substantially constant. With proper design and experimentation, an automatic gain control circuit can be chosen to give a clean sine wave of 1 Hz to 1 M Hz at its output.

FREQUENCY CONTROL USING AN ANALOG MULTIPLIER

The second method involves the use of an analog multiplier, the ICL 8013, to mix two low frequency waveforms and obtain an output which is a clean and pure sine wave in the lower frequency range as from 1 Hz to 100 K Hz.

The data sheets for the ICL 8013 are available in Apendix C. The Intersil ICL 8013 is a four quadrant analog multiplier. The integrated circuit chip is setup for multiplication as shown on page 106. The trimming potentiometers are connected as shown in the figure on page 108. The trimming procedure as detailed on page 106 are followed after giving the Xin and Yin inputs from two function generators. The experimental setup consists of two function generators feeding the analog multiplier. The modulated output of the multiplier was fed to an active filter. The block diagram of the configuration is as shown in Fig. 2. The sine wave from one of the function generators is kept constant at, say 200 K Hz. The sine wave from the second function generator is varied from 0 to 200 K Hz. The modulated output of the multiplier contains the basic frequency, the sum of the two frequencies, and the difference of the two frequencies. The difference frequency is the one of interest and this is low pass filtered to give the required frequency.

The variable frequency from the function generator that is varied in the experiment, and the output frequency from the filter output can again be added together to give a larger variation in the frequency range at the final output.

ANALOG MULTIPLIER

Intersil ICL 8013 is a Four Quadrant Analog Multiplier that can be configured to work out some simple mathematical functions such as multiplication, division, squaring, taking the square root, and can also be configured as a variable gain amplifier. The details and the data sheets are shown in Appendix C. The basic function of ICL 8013 is such that the output is proportional to the algebraic product of the two inputs. The advantage here is that the inputs can be AC waveform signals. The large bandwidth of 1 M Hz is a very good advantage for the present application in instrumentation.

Amplitude modulation is the basic process used for multiplication of the signals. The process by which a function is made to vary in accordance with some information is called modulation [12]. When the amplitude, or the maximum value of a signal is varied in accordance with some information, it is known as amplitude modulation. This is the principle being used here for analysis while mixing two signals. For analysis, considering a voltage $v(t) = W \cos w't$ called the carrier, and some information such as $u(t) = U \cos wt$, then W maybe made to vary so that

$$v(t) = [V + k\, u(t)] \cos w't$$

where k is a constant.

Hence,
$$v(t) = V \left[1 + \frac{kU}{V} \cos wt\right] \cos w't$$

Let $m = \frac{kU}{V}$.

Then $v(t) = V[1 + m \cos wt] \cos w't.$

Since $2 \cos A \cos B = \cos (A+B) + \cos (A-B),$

$$v(t) = V \cos w't + \frac{mV}{2} \cos (w'+w)t + \frac{mV}{2} \cos (w'-w)t.$$

Since the signals lie in the range from w'-w to w'+w the bandwidth will be

$$B = \frac{2w}{2} = 2\pi f.$$

Fig. 29 shows the frequency spectrum of the amplitude modulated waveform, and Fig. 30 shows the output of the same waveform on an oscilloscope.

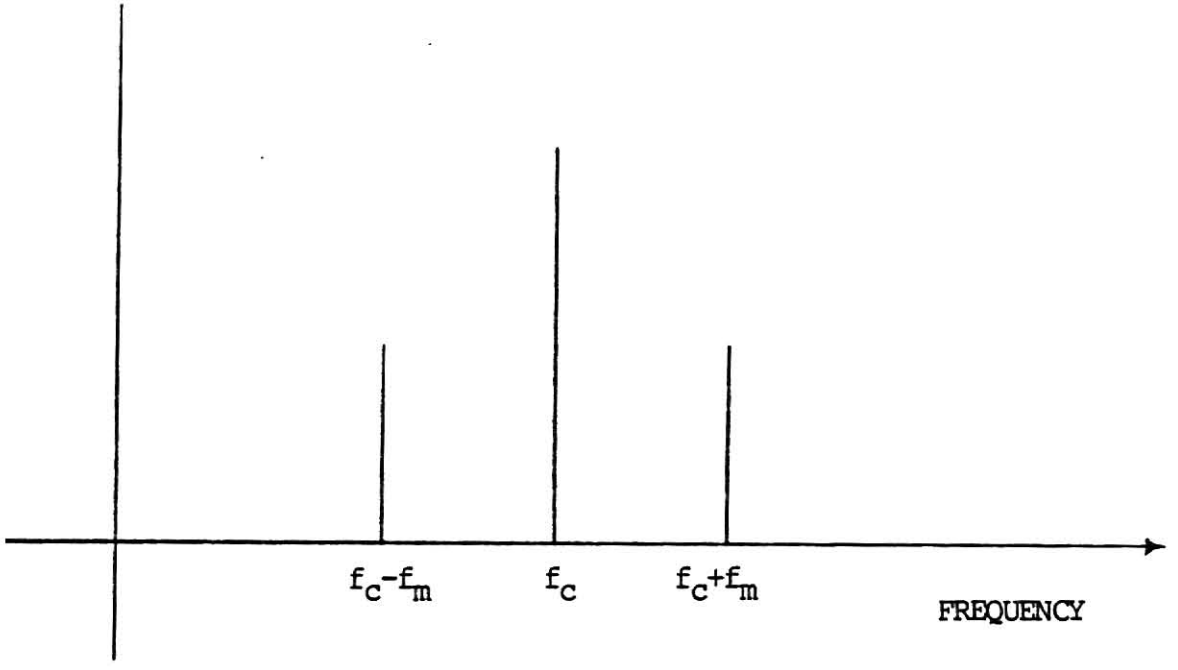


Fig. 29

Frequency Spectrum of an Amplitude Modulated waveform.

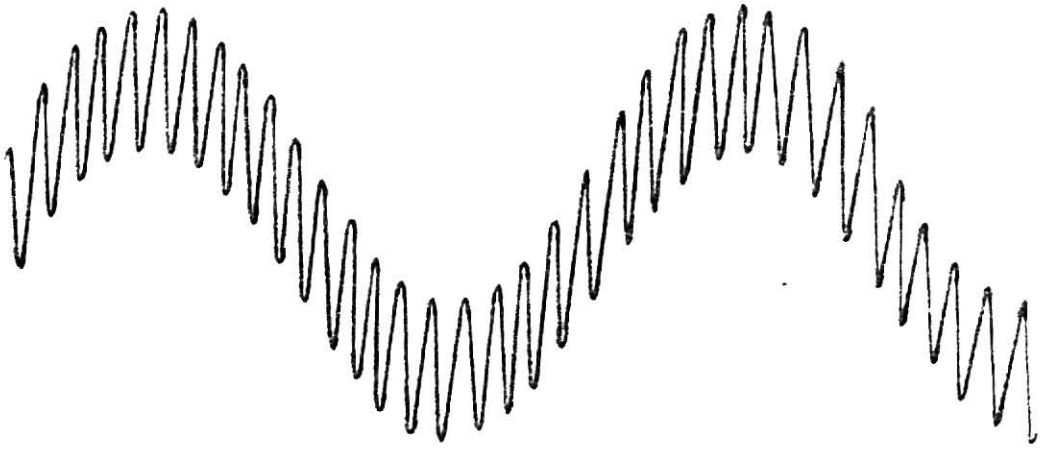


Fig. 30

Oscilloscope display of an Amplitude Modulated waveform.

ACTIVE LOW PASS FILTER

An ideal low pass filter is again reproduced for convenience in Fig.31. All signals in the $0 <= f_c <= f'$ band are transmitted without loss, but for all frequencies where $f_c > f'$ there is no output. In practice such characteristics cannot be obtained, but reasonably good approximations can be got because of the presence of non-ideal physical elements involved in making a filter. If P(s) is the polynomial in the variable s with zeros in the left hand plane, the low pass filter approximation is given as

$$A(s) = \frac{1}{P(s)}$$

Operational amplifiers can be used as the active elements in the filter design which help in realising the arbitrary left hand poles for A(s), along with resistors and capacitors as the passive elements.

The Butterworth polynomial B(s) is found to give a low ripple on the filter characteristics as compared to the others. Thus

$$A(s) = \frac{A'}{B(s)}$$

where $s = jw$.

$$|A(s)|^2 = |A(s)|\ |A(-s)| = \frac{A'^2}{1 + (w/w')^{2n}}$$

From the above two equations

$$|B(w)| = \sqrt{1 + (w/w')^{2n}}$$

Higher the values of n, better the response approximates the characteristics of an ideal low pass filter. It is found that when n is even, the polynomials are the products of the quadratic forms, and when n is odd an additional factor of (s+1) is present. This can be seen from Table 2 [1]. The damping factor k is defined as one half the coefficient of s in each quadratic factor in Table 2.

Table of the factors of polynomials for different values of n.

n	Factors of Polynomials
1	$(s + 1)$
2	$(s^2 + 1.414s + 1)$
3	$(s + 1)\ (s^2 + s + 1)$
4	$(s^2 + 0.765s + 1)\ (s^2 + 1.848s + 1)$
5	$(s + 1)\ (s^2 + 0.618s + 1)\ (s^2 + 1.618s + 1)$

TABLE-2

For a first order filter, the transfer function is

$$\frac{A(s)}{A'} = \frac{1}{s/w' + 1}$$

where $w' = 2\pi f'$ is the high frequency 3dB point.

For a second order Butterworth filter

$$\frac{A(s)}{A'} = \frac{1}{(s/w')^2 + 2k(s/w') + 1}$$

From the point of view of a practical realisation of such a filter, it is found that w' can be chosen so that

$$w' = 1/RC \quad \text{and} \quad A = 3 - 2k \quad \text{or} \quad 2k = 3 - A.$$

A fourth order Butterworth filter can be designed from the above information. Considering a 3dB cutoff frequency of 100 K Hz,

$$A1 = 3 - 2\,k1 \quad \text{and} \quad A2 = 3 - 2\,k2$$

From Table 2

$$A1 = 3 - 0.765 = 2.235 \quad \text{and} \quad A2 = 3 - 1.848 = 1.152.$$

$$A1 = \frac{Ra + Rb}{Ra}.$$

Let $Ra = 10$ K , then $Rb = 12.35$ K .

$$A2 = \frac{Rc + Rd}{Rc}$$

Let $Rc = 10$ K , then $Rd = 1.52$ K .

Let $R = 1$ K . Since $f' = 1/2 \quad RC$,

$$C = \frac{1}{2\,\pi\,f'R} = \frac{1}{2\,\pi\,100\;\;10^3\;\;10^3}$$

$$= 0.001591 \text{ uF} = 1591 \text{ pF}.$$

Fig.32 shows the design of this fourth order Butterworth low pass filter with a 3dB cutoff frequency of 100 K Hz.

The operational amplifiers used in the design of the active filters were uA 741 integrated circuit chips, but it was found that the waveform at lower frequencies was not very clear. A higher frequency waveform was found to be overlapping the lower frequency waveform of interest. It was determined that this was due to the bandwidth of the operational amplifier being not very large, which in turn, was not

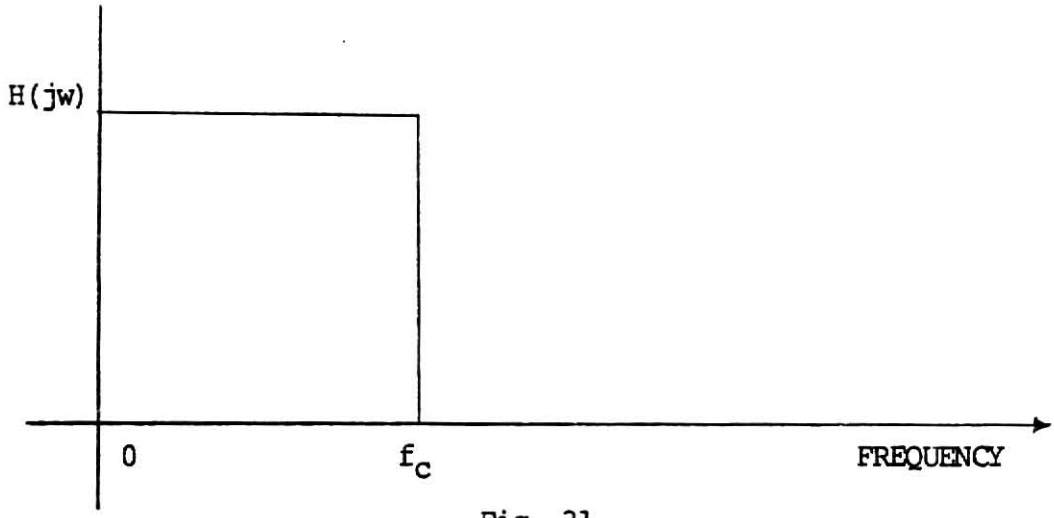


Fig. 31

Ideal Low Pass Filter characteristics.

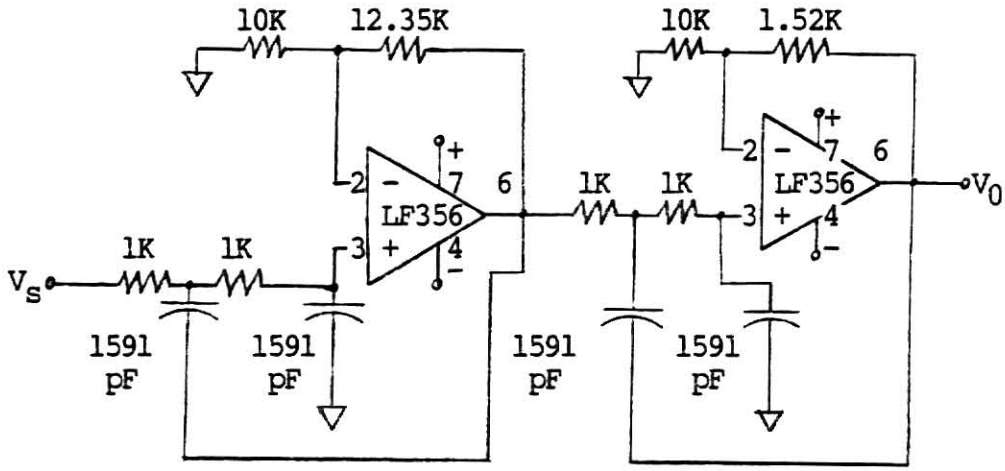


Fig. 32

Fourth order Butterworth Low Pass Filter.

filtering the waveform effectively. The LF 356 operational amplifier was found to have a larger bandwidth, and when the uA 741 was replaced with the LF 356 operational amplifiers the waveform at low frequencies became fairly clear and clean. Appendix C contains the data sheets of both uA 741 and the LF 356 operational amplifiers.

The characteristics of the filter was individually determined and is shown in Fig. 33.

For the present application with the uA 741 operational amplifiers the output of the filter was found to vary over a range of 250 to 400 K Hz when the upper fixed frequency of the fixed oscillator at the mixer input was 400 K Hz. With an LF 356 the range was from 200 to 400 K Hz. Fig. 34 shows the output of the multiplier and the filtered output waveform. It is also to be noted that there is a 180 degrees phase shift between the output of the multiplier and the output of the filter.

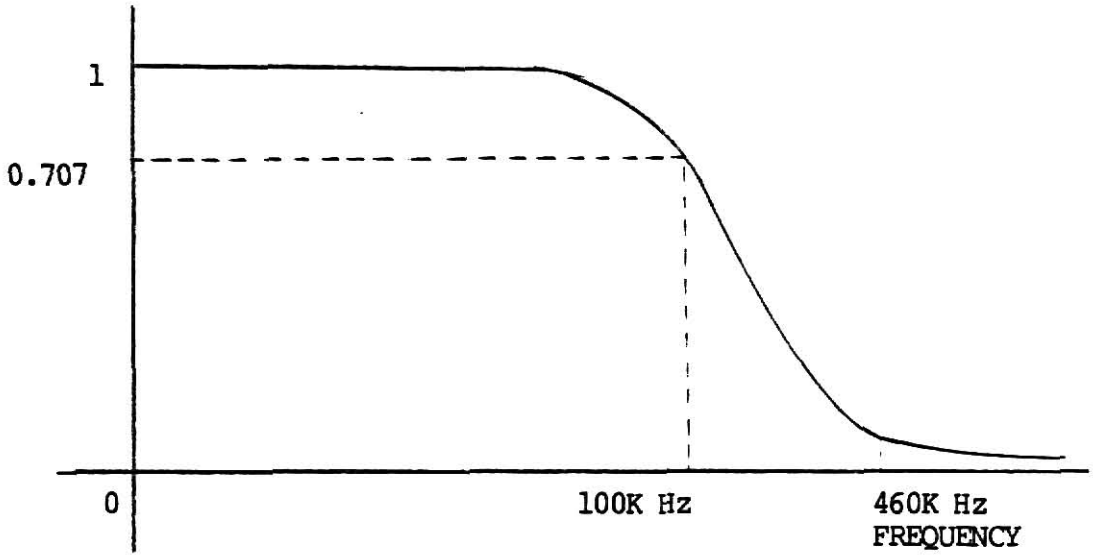


Fig. 33

Practical Active Low Pass Filter characteristics

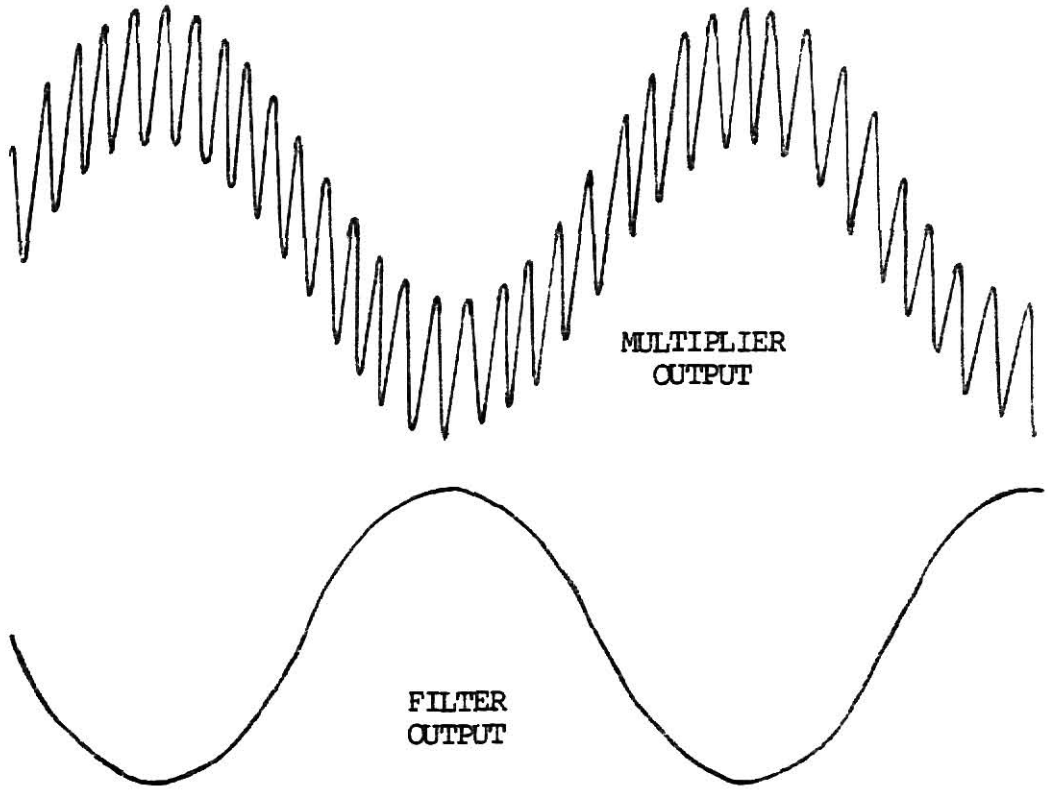


Fig. 34

Multiplier and Filter output waveforms.

DIGITAL TO ANALOG CONVERTERS

Digital to analog converters are the devices by which computers communicate with the outside world. They are employed in a variety of applications including automatic test systems.

D/A converters [8] reconstitute the original data after processing, storage, or even simple transmission from one location to another in digital form. A basic D/A converter contains an arrangement of weighted values of resistances, each of the resistance divider ratios being controlled by a particular level of digital input data, which develops varying output voltages or currents as per the input digital code.

Fig. 35 shows the transfer function of an ideal three bit D/A converter [7]. A single, discrete analog output value, generally a voltage, is produced by each input code word. Over the output range of the converter 2^n different values are produced including zero. It should be noted that the output has a one-to-one correspondence with the input.

Many different circuit techniques can be used to implement D/A converters, but only a few of the popular ones are used today. In the parallel type all the bits change simultaneously on the application of an input code, but in the serial type an analog output is produced only after receiving all the digital input data in serial form. Virtually all the D/A converters used today are of the parallel type.

The different types of D/A converters used commonly are :

a. Weighted current source D/A converter

b. R/2R ladder D/A converter

c. Multiplying and deglitched D/A converters.

D/A converters [8] have fixed references, but for most applications, a special class of them having capabilities of handling various sources, and also AC reference sources exist. These are called the multiplying DAC's since the product of the number represented by the digital input code, and the analog reference voltage (which may vary from zero to full scale, and sometimes goes into the negative values as well) is their output value. Because the turns ratio of the tapped transformers have very good long-term stability and immunity to temperature effects, as compared to the divider circuitry of precision resistors, the D/A converters use tapped transformers in the case of AC measurements and resolver/synchro conversions.

In the present applications the point to be kept in mind is that the input of the D/A is from the microprocessor system whose peripheral output ports will be connected to the D/A. In the first method, the output of the D/A will be connected to the varicap which requires a voltage output for its control. The D/A that will have to be selected here will have to be chosen so that it meets the input-output requirements. Moreover, speed is of importance here, and hence, the speed of conversion will also be an important factor in the selection of the D/A converter. In the second method, the speed, though of importance, is not as critical as for the first method. The controlling element to be connected to the output of the D/A converter in the second method will depend upon the varying element of the oscillator in the circuit. This could again be an semiconductor varicap.

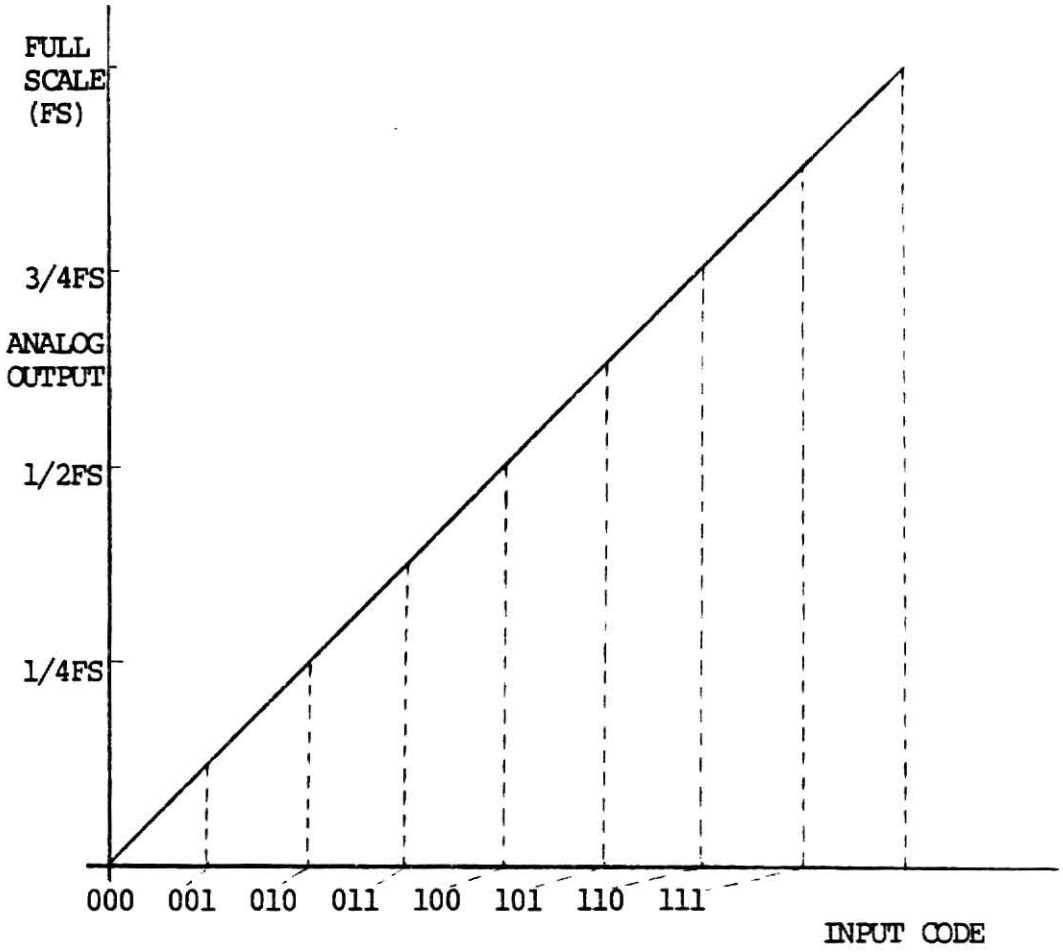


Fig. 35

Transfer function of an ideal three-bit D/A converter.

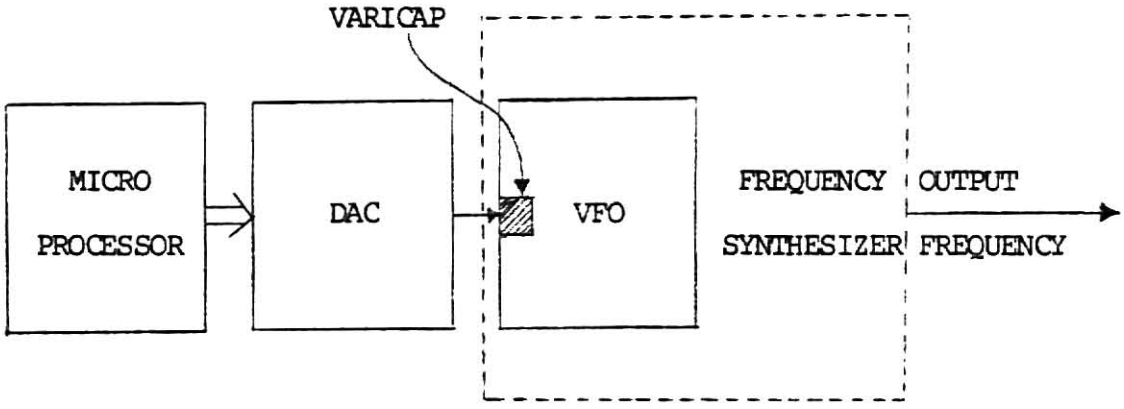


Fig. 36

Block diagram of microprocessor control.

MICROPROCESSOR

In the present day, computers are being used everywhere for all kinds of applications. A microprocessor is a very powerful tool and since it is available in such small sizes it can be conveniently placed almost anywhere and its utility value has gone up greatly. Here, a microprocessor is being used as the controlling element for frequency synthesis. When a user needs a particular frequency output at a point for measurement, or for any application in the laboratory, all that is required is for him to key-in his required frequency value on the keyboard connected to the microprocessor. The microprocessor sends out a signal to the D/A converter which outputs the required voltage value to vary the varicap in the voltage controlled oscillator circuit, which in turn controls the output frequency of the synthesizer. Fig. 36 shows the block diagram of the control.

There is a proposal to use the NSC 800 microprocessors in the instrumentation laboratory and studies are being conducted for their implementation in various instrumentation projects, the frequency synthesizer being one of them.

National Semiconductor company claims that the NSC 800 family of microcomputer and other supporting integrated circuit chips are of the "High Performance/Low-Power concept" [9]. This family is said to have the functionality of one of the most advanced 8-bit, commercially available, mid-range microprocessors. They are of particular interest due to the expanded capabilities brought about by the CMOS nature of this family of integrated circuit chips. The NSC 800 system

incorporating the P^2CMOS technology has its biggest advantage as low power consumption. On an average the P^2CMOS implementation is said to utilise 90 to 95% less power than a comparable NMOS device. Hence, the NSC 800 is a natural choice for applications that utilise battery operation. This is thus particularly useful in instrumentation applications. This system provides for the same high speed of operation as NMOS devices but with only about 5% of the power consumption. This automatically helps in isolating noise problems and hence is a big step forward where work is done with low signal values, especially as in instrumentation applications.

The NSC 800 has a multiplexed address/data bus, on-chip clock generation, on-chip interrupt capability, dynamic memory refresh control, direct memory access, multiprocessing, and operation in power-save mode. These are the hardware advantages. A large instruction set, a sophisticated set of addressing modes, and a multiplicity of programmable registers are the other software advantages.

A similar microprocessor system may be undoubtedly found in the vast market today, but the biggest advantage that the NSC 800 system has over the others is low power consumption, because of which the system can be run, as described earlier, on batteries. This system is suggested here for use in developing the frequency synthesizer.

DIGITAL TECHNIQUE FOR SINE WAVE SYNTHESIS

In this third method, an attempt is made to simulate the condition of Digital Frequency Synthesis with the help of a software technique on the PDP-11/03 computer system in the Instrumentation Laboratory.

Fig. 3 shows the basic principle on which this method functions. One period of a sinusoidal waveform is sampled at equal intervals of time and these sampled values are stored in successive memory locations of the Read Only Memory (ROM). This waveform can be made to have any frequency by simply outputting the samples at different rates. The advantage of this method is that the shape of the output waveform need not necessarily be sinusoidal, but can be of any desired shape. By this technique any stored waveform of any shape can be output at different frequencies for different applications. The control of frequency is obtained simply by controlling the time interval between two successive output samples. By taking a sufficiently large number of samples over one period of time, the continuous reproduction of the waveshape can be made to approximate the original waveform very well with very little error. The oscillator in Fig. 3 is used purely to control the rate at which the counter is made to output the ROM values to the Digital to Analog Converter (DAC). The output of the DAC is essentially a stepped waveform as shown in Fig. 37. When a large number of samples are taken for one period of the waveform, the steps are so small that they almost approximate a line. To get a true, fine and continuous waveform, the output of the DAC is fed to a suitable filter network which smoothes out the waveform as shown in Fig. 38.

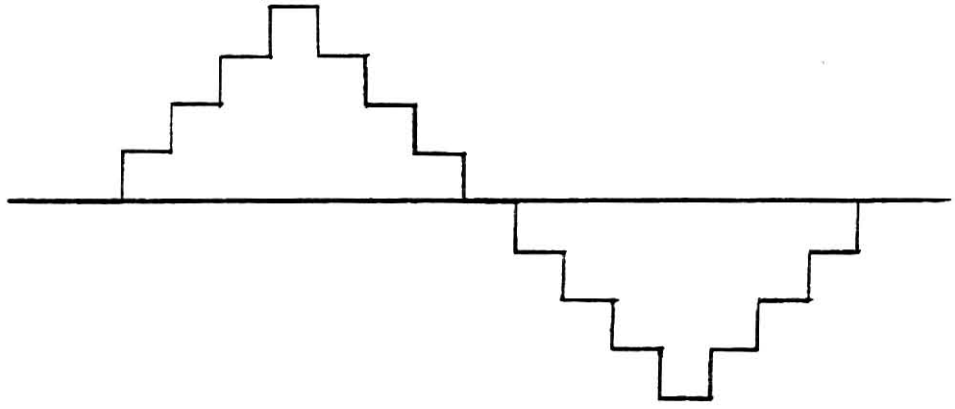


Fig. 37

Output of the DAC with 16 samples.

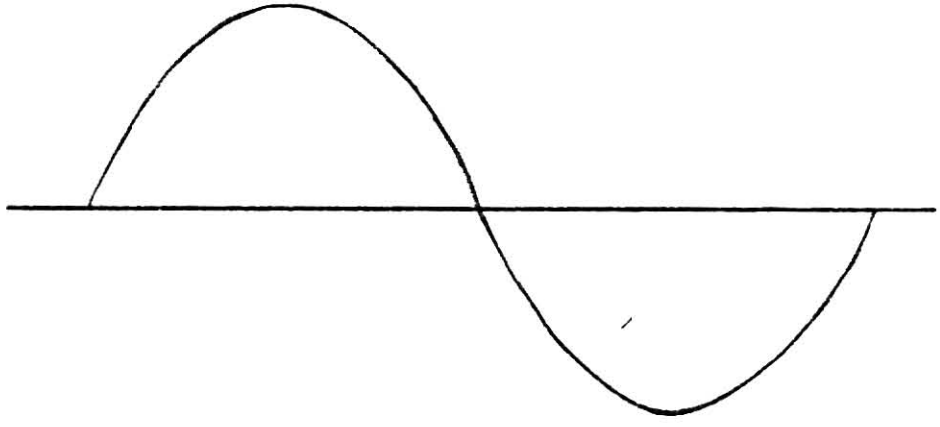


Fig. 38

Filtered output for the waveform in Fig. 37.

PDP-11/03 COMPUTER SYSTEM AND THE EXPERIMENTAL SETUP

The PDP-11/03 computer system in the Instrumentation Laboratory has an LSI-11 microprocessor in it. A patch-panel provision is available which has outlets such as A/D, DAC, Function Generator, DVM, VCO, and other functions on the panel. The patch panel outlets are configured from the connector boards in the patch panel box, which in turn, are connected to the system. These are also software controlled. For the Instrumentation Laboratory some software packages are available to provide for experimentation, such as the LABLIB subroutines. These are available on diskettes and can conveniently be used. The present system configuration uses only a portion of the PDP-11/03 system capabilities so as to make the laboratory system easier to use. The editor used with the system is TECO (Text Editor and COrrector), which is distributed with DIGITAL operating systems. This is a powerful editor which can be used more than just for instrumentation experiment purposes.

In the present experiment, a simulation technique is being used to verify the feasibility of this method of frequency synthesis. The system memory space is used in place of the ROM. A software counter is used to give the time intervals between the samples of the DAC. The patchpanel DAC is made use of to obtain the output waveform at the patchpanel outlet. An oscilloscope is connected to the outlet and the analog output of the DAC is displayed on the oscilloscope. The 'DAC subroutine' is a subroutine of the LABLIB instrumentation laboratory software programs [14]. With this subroutine the user can select any

one of the four 12-bit DAC channels on the patchpanel. He can also convert an offset binary number lying between 0 and 4095 to a corresponding equivalent output voltage value of -5.12 to +5.12 Volts. The DAC conversion time is approximately 170 u sec.

SOFTWARE DESCRIPTION

The software flowchart for the simulation program is as shown on Page-77. Appendix D shows the listing of the program used. The program is written in Fortran and is made as a user-friendly, menu-driven program. The variables of interest are

1. the number of samples per cycle
2. the frequency of the output waveform, and
3. the amplitude of the sine wave.

The frequency of the output waveform is dependent upon the time gap between two samples in a cycle of the sine wave. By varying the time, the output frequency can be varied. The number of divisions per cycle also control the frequency as can be seen in Table 3.

The speed of conversion by the DAC limits the upper frequency that the sine wave can achieve. This is the limitation that this method has. One has also got to take into consideration the speed at which the LSI-11 system works. Under the present circumstances, for the program written in Fortran it is found that the upper limit of frequency is 1.428 K Hz. This is a restriction due to the Fortran language program being run on this system. Of course, on a better system, higher frequencies can easily be obtained. Even on this system, with a different DAC subroutine program of LABLIB, frequencies upto almost 1/170 M Hz, or 5.8824 K Hz can be obtained.

In this program the values of a sine function over one period of time are calculated for a specific number of points in the cycle. These sine function values are the values of the amplitude for the sine wave.

These values cannot directly be fed into the DAC since the DAC is functional only with a digital binary set of integer values. These offset binary numbers have to lie between 0 and 4095, and these will be converted to voltage values of between -5.12 to +5.12 Volts respectively. The program is written to do this conversion and feed the values to the DAC. A small timing loop is written to provide the necessary timing gap between two successive samples being outputted. This time is conveniently provided as a variable, and by varying this time, the frequency of the output waveform can be varied over a wide range of values, which can only be limited by the speed of conversion of the DAC being used. The frequency can also be varied by varying the number of samples per cycle.

A table of sampling time and the corresponding output frequency is shown in Table 3. It is seen that with this experimental setup lower values of frequency are available with higher accuracy, and also the upper limit of frequency is 1.428 K Hz. This demonstrates the feasibility of the application of such a configuration. The restriction on the upper frequency in this case is because of the speed of the LSI-11 system and also because of the DAC subroutine program. The DAC subroutine program could possibly be revamped in PDP-11/03 Macro language to take less time for execution since the DAC itself allows upto approximately 5.88 K Hz frequency of the waveform because of its 170 u sec time of conversion.

With proper components used, with the configuration in Fig. 3, a good sine wave synthesizer can be built with pretty good accuracy and a fairly smooth variation in frequency values.

SOFTWARE FLOWCHART

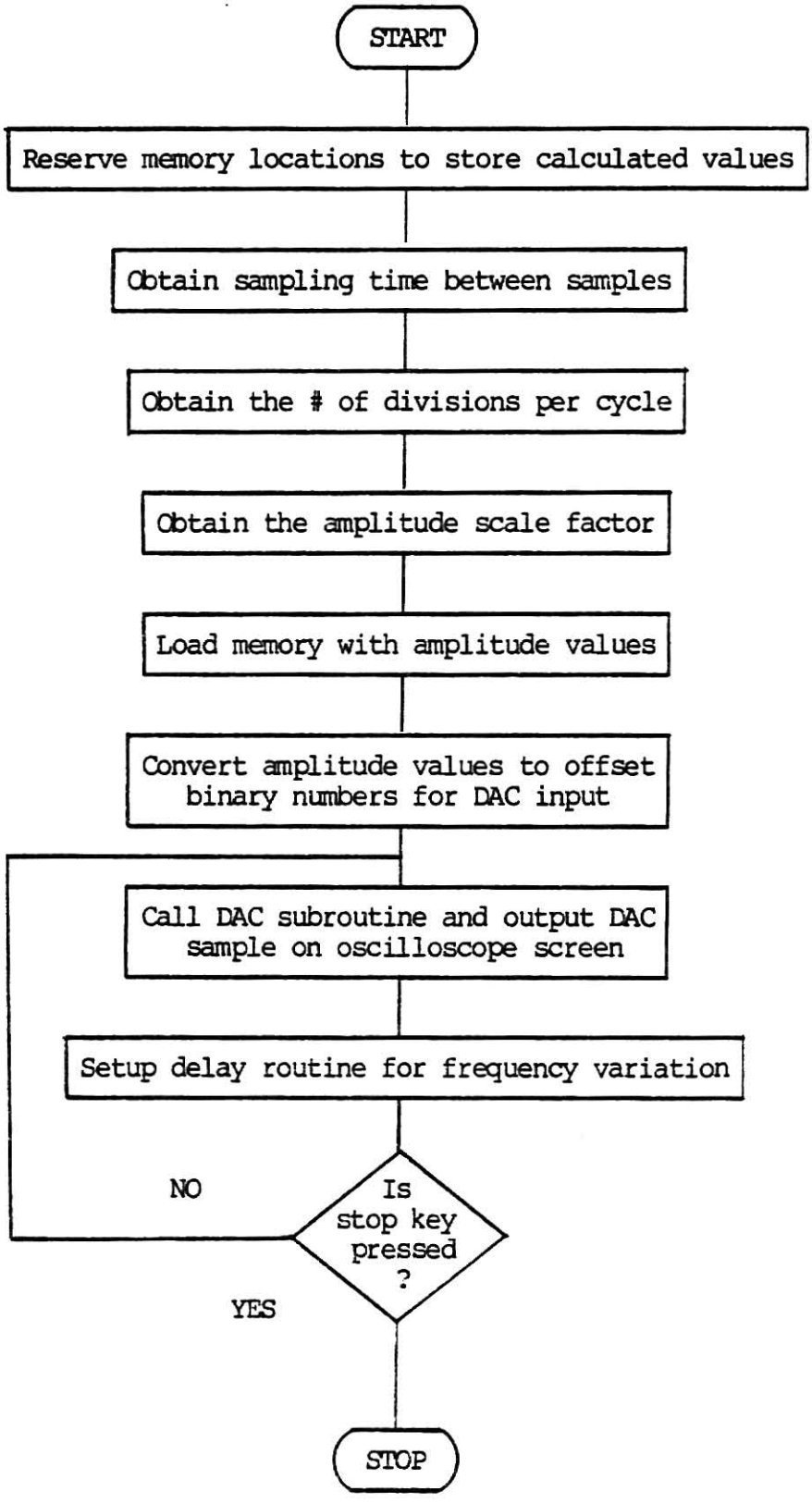


TABLE 3

Table of sampling time and output frequencies.

Sampling time between samples	Number of divisions/cycle	Time for half a cycle (m. sec)	Frequency (Hz)
500	100	1640	0.3048
400	100	1360	0.3676
300	100	1000	0.5
200	100	680	0.735
100	100	340	1.4706
75	100	260	1.9231
50	100	180	2.7778
25	100	98	5.102
20	100	80	6.25
15	100	54	9.2593
10	100	48	10.4167
5	100	31.5	15.873
4	100	27.5	18.18
3	100	24.5	20.408
2	100	21	23.80
1	100	17.5	28.57
10	500	235	8.51
10	400	185	10.81
10	300	145	13.79
10	200	94	21.27
10	100	46	43.47
10	50	23.5	85.10
10	20	10	200
10	10	5.8	344.82
10	4	1.9	526.31
5	4	1.3	769.23
1	4	0.7	1428

(The scale in the above table has been chosen as 1.0, the maximum.)

COMPARISON BETWEEN THE THREE METHODS, AND CONCLUSION

Three totally diverse low cost methods of frequency synthesis have been chosen here for experimentation and analysis.

The first method being a high frequency technique involves the consideration of noise reduction and reduction in signal interference. It has been experimentally found out that this is a feasible technique utilising low cost discrete components. The total cost of components is not more than about $50.00. The drawback in this technique is that there is a persistent fight with noise which the person working has to overcome. The cost of the work and the time involved is quite high in comparison to the other two methods. A simple variable frequency oscillator can be built to vary over a range of frequencies as large as 1 M Hz and mixed with another high frequency from a fixed oscillator and the required value of frequency filtered out. At each stage of the circuit the interference between the two frequencies being mixed has to be avoided by grounding and shielding techniques. This grounding and shielding problem can become quite complex as was found during experimentation. A compact design configuration of the layout of the components is an absolute must, and the layout should be such that the two oscillators built on different panel boards and shielded are made to meet only at the mixer stage. In spite of these hurdles that one has to cross, it should not be forgotten that this method is a good one when a continuous variable frequency is required over a full range of 1 M Hz. No doubt this involves work and time, but with proper design and assembly a good sine wave generator can be built.

The second method is a very simple technique and works very well for a lower range of frequencies. The analog multiplier technique is very similar to the first method, but does not involve the problem of noise because of working at lower frequencies. When a continuous variation in frequency is required from zero to a few K Hz range this technique is very much recommended. The disadvantage here is the limitation in the range of frequencies. The components used are all low cost ones, and the technique is a very simple one. The cost involved in the work and the time taken for experimentation is very low. The total cost of components here is less than about $50.00.

The third method is also a very simple digital technique. The cost of components again, would run into less than about $50.00. The amount of time and work involved is quite low and the results are very good. By taking a sufficiently large number of samples a sine wave can be generated which would be pretty smooth and can give a clean output waveform. The variation in frequency, though not continuous, would be in small steps. With proper care in design these steps can be made small enough to suit the requirement of frequency variation in the laboratory. Better components with marginally a little higher cost can be used to build this sine wave synthesizer with very good accuracy and much better performance.

The first two methods involve the use of a microprocessor, a DAC, and the keyboard associated with the microprocessor for purposes of control of the output frequency. This restricts their use to places where microprocessors are necessarily available in the laboratory. If microprocessors are not used with these methods they can be manually controlled by a variable capacitor or with the help of any other

suitable variable component in the circuit, but then, this would not be an automated method.

On the other hand, the third method does not involve a microprocessor and hence can be used as an individual unit. Keeping in mind the future application of a frequency synthesizer as being the part of a module of an automatic test system in the instrumentation laboratory, the third method is best suited for this application. Of course, it is also useful for other applications too.

Moreover, considering the overall cost involved for frequency synthesis, since the digital method does not use a microprocessor, it is the cheapest of the three techniques used. It is also of interest to remember that the digital technique need not be restricted only to sine wave generation but can also output different frequencies of any shape of the waveform that is stored in memory.

The digital technique for frequency synthesis is definitely recommended for use in the instrumentation laboratory.

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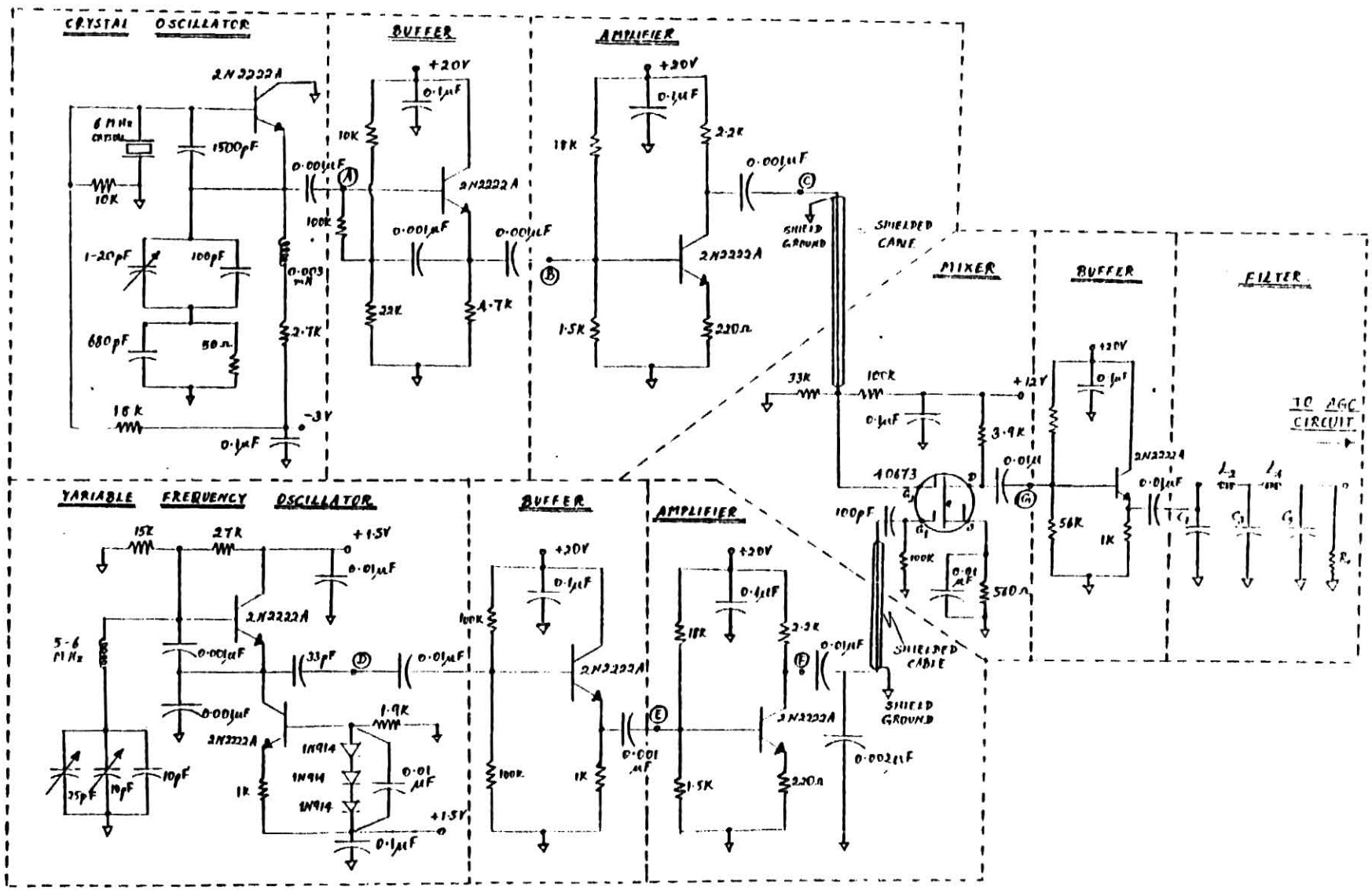
Finally, I would like to express my gratitude to my family and friends for all their support and inspiration.

APPENDIX A

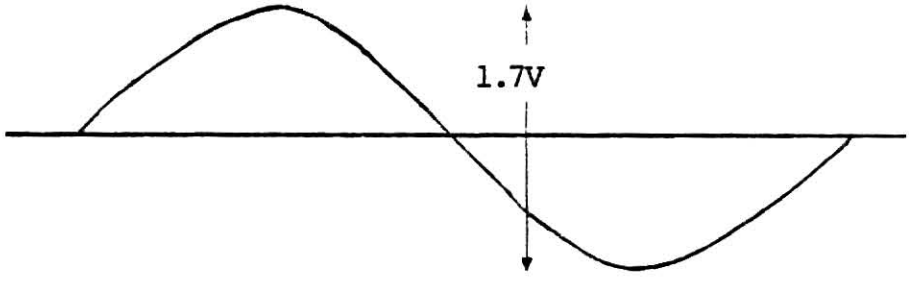
Overall circuit diagram of the RF synthesizer.

Waveforms and Spectrum Analyser diagrams.

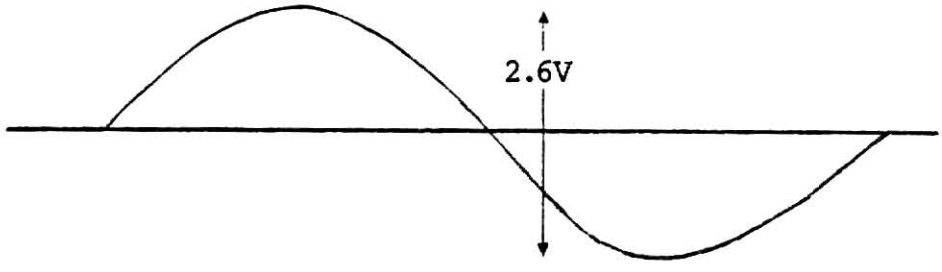


Overall circuit diagram of the RF synthesizer.

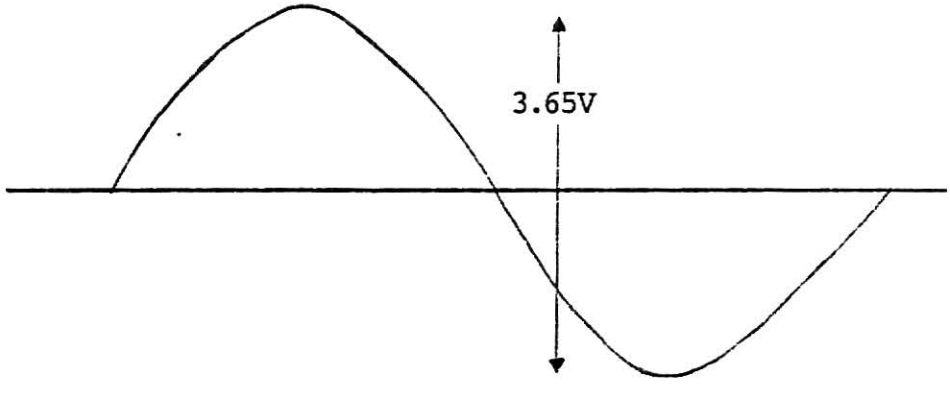
Waveforms and spectrum analyser diagrams.



Waveform at point A

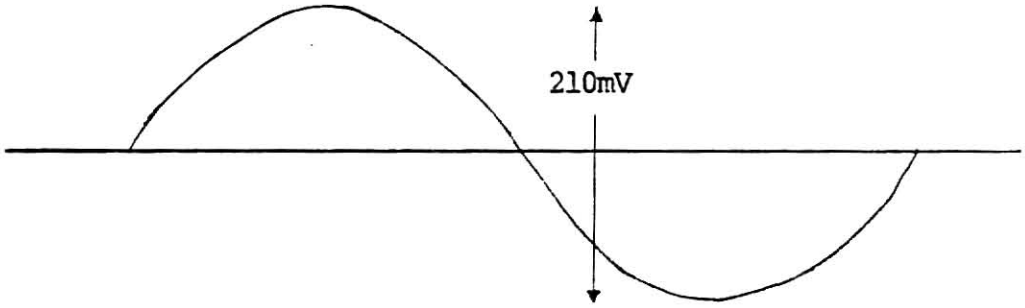


Waveform at point B

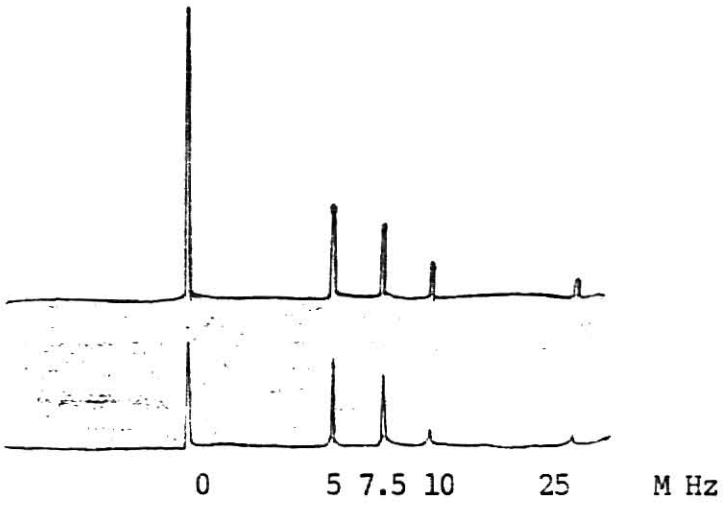


Waveform at point C

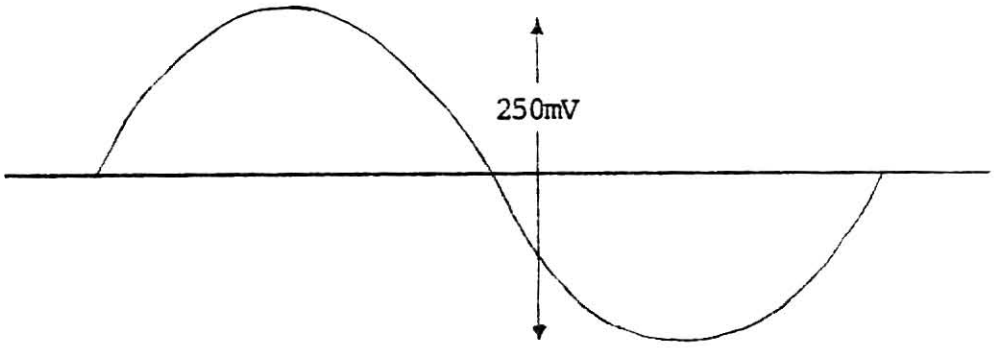
Circuit assembled on the Proto Board.



Waveform at point D

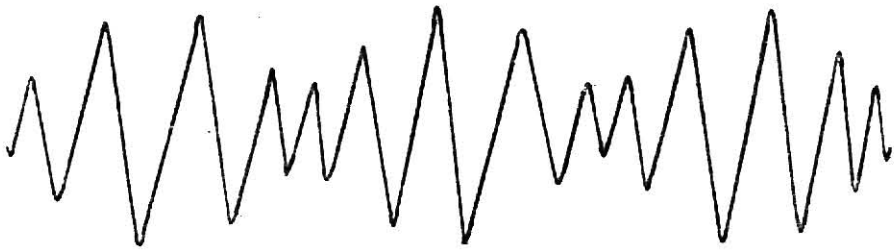


Spectrum analyser display at points D and E.

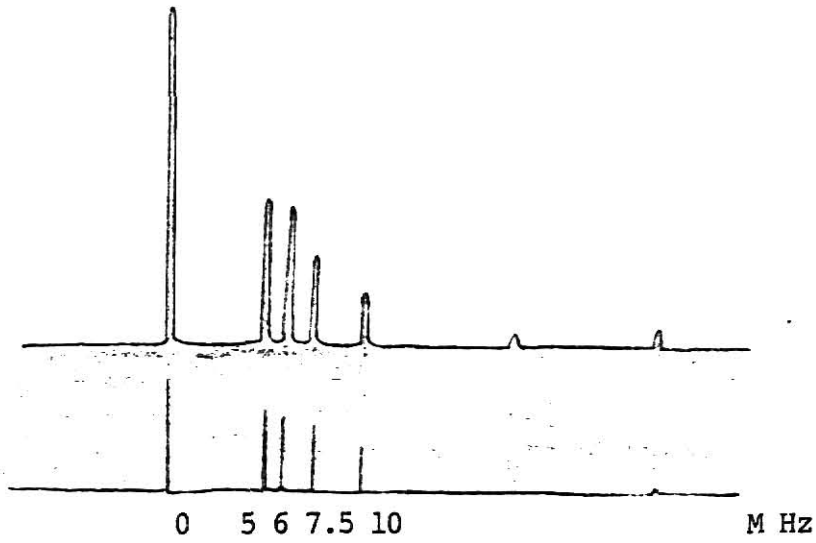


Waveform at point E.

Circuit assembled on the Proto Board.

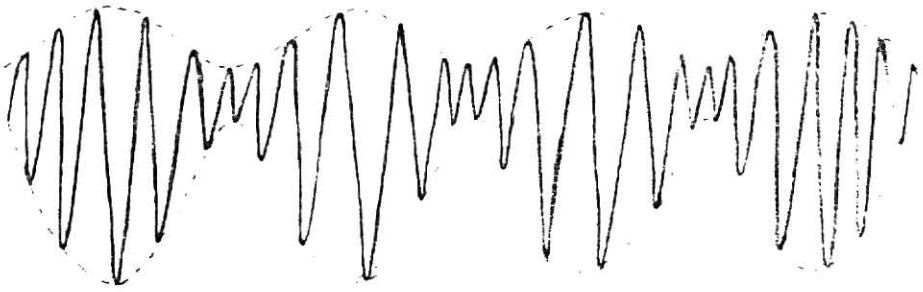


Waveform at point F.

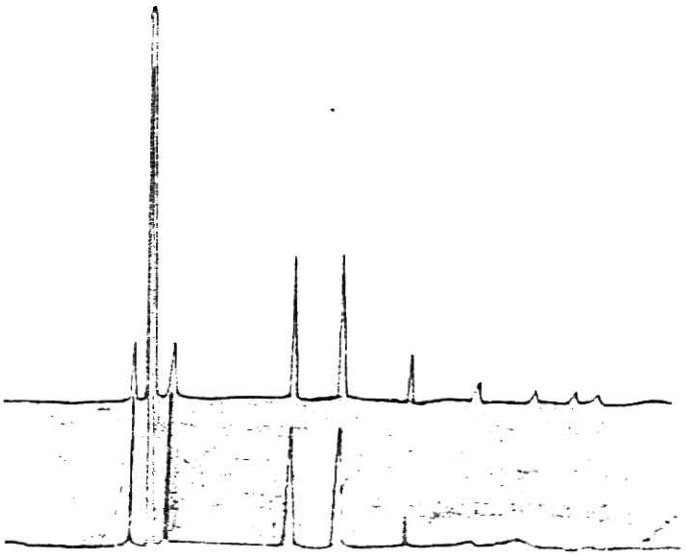


Spectrum analyser display at point F.

Circuit assembled on the Proto Board.

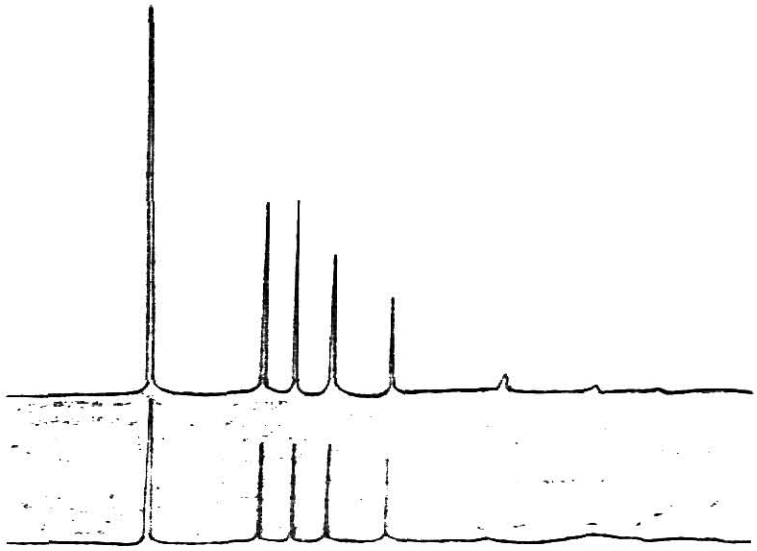


Waveform at point G.

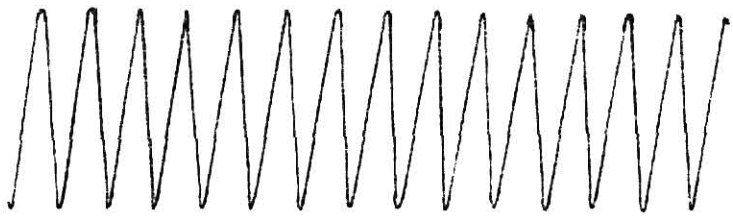


Spectrum analyser display at point G.

Circuit assembled on the Proto Board.

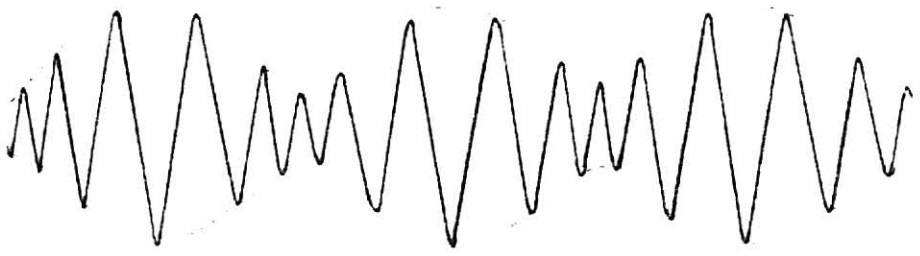


Spectrum analyser output of the mixer at point F.

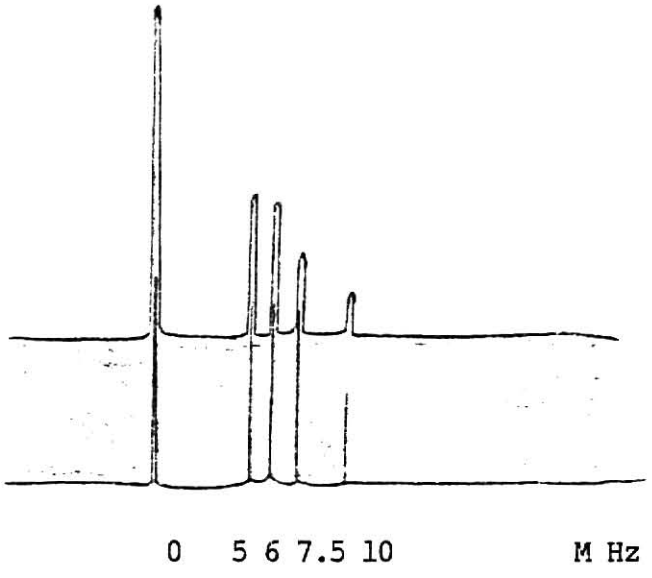


Waveform at point F.

Circuit assembled on the perf-board without shielding.



Waveform at point G.



Spectrum analyser display at point G.

Circuit assembled on the perf-board with shielding.

APPENDIX B

Table-1 : Table of Butterworth and Chebyshev filter coefficients.

Program in BASIC for filter values calculation.

Data sheets for 2N2222A transistors and 40673 mixer.

g_k Values for Chebyshev and Butterworth ($A = 0$) Low Pass Filters.
(Normalized to $R_L = 1\ \Omega$ and a ripple bandwidth of 1 rad s^{-1})

A, dB	n	g_1	g_2	g_3	g_4	g_5	R_g^{-1}	ω_c, −3 dB
0	3	1.000	2.000	1.000	—	—	1.000	1.000
	4	0.7654	1.8478	1.8478	0.7654	—	1.000	1.000
	5	0.6180	1.618	2.000	1.6180	0.618	1.000	1.000
0.1	2	0.8430	0.6220	—	—	—	0.7378	1.9432
	3	1.0316	1.1474	1.0316	—	—	1.000	1.3890
	4	1.1088	1.3062	1.7704	0.8181	—	0.7378	1.2131
	5	1.1468	1.3712	1.9750	1.3712	1.1468	1.000	1.1347
0.25	2	1.1132	0.6873	—	—	—	0.6174	1.5981
	3	1.3034	1.1463	1.3034	—	—	1.000	1.2529
	4	1.3782	1.2693	2.0558	0.8510	—	0.6174	1.1398
	5	1.4144	1.3180	2.2414	1.3180	1.4144	1.000	1.0887
0.5	2	1.4029	0.7071	—	—	—	0.504	1.3897
	3	1.5963	1.0967	1.5963	—	—	1.000	1.1675
	4	1.6703	1.1926	2.3661	0.8419	—	0.504	1.0931
	5	1.7058	1.2296	2.5408	1.2296	1.7058	1.000	1.0593
0.75	2	1.6271	0.7002	—	—	—	0.4304	1.2852
	3	1.8243	1.0436	1.8243	—	—	1.000	1.1236
	4	1.8988	1.1243	2.6124	0.8172	—	0.4304	1.0689
	5	1.9343	1.1551	2.7833	1.1551	1.9343	1.000	1.0439
1.00	2	1.8219	0.6850	—	—	—	0.3760	1.2176
	3	2.0236	0.9941	2.0236	—	—	1.000	1.0949
	4	2.0991	1.0644	2.8311	0.7892	—	0.3760	1.0530
	5	2.1349	1.0911	3.0009	1.0911	2.1349	1.000	1.0338
1.50	2	2.1688	0.6470	—	—	—	0.2983	1.1307
	3	2.3803	0.9069	2.3803	—	—	1.000	1.0574
	4	2.4586	0.9637	3.2300	0.7335	—	0.2983	1.0322
	5	2.4956	0.9850	3.4017	0.9850	2.4956	1.000	1.0205

Table - 1

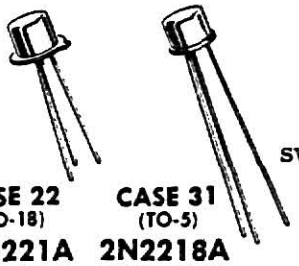
Butterworth and Chebyshev filter coefficients.

Program in BASIC for filter values calculation.

```
10   DIM G(5), L(5), C(5)
20   G(1)=.618
30   G(2)=1.618
40   G(3)=2
50   G(4)=1.618
60   G(5)=.618
70   INPUT F0,R0
80   PRINT#1 "FREQ=",F0,"IMPEDANCE=",R0
90   F1=2*(22/7)*F0
100  FOR K=1 TO 5 STEP 2
110  C(K)=G(K)/R0*F1
120  C(K)=C(K)/1000
130  PRINT#1 C(K)," ",
140  NEXT K
150  FOR K=2 TO 4 STEP 2
160  L(K)=G(K)*R0/F1
170  PRINT#1 L(K)," ",
180  NEXT
190  PRINT#1 " "
200  END
```

Data sheets for 2N2222A transistor.

2N2218A (SILICON)
2N2219A
2N2221A
2N2222A



CASE 22 (TO-18) **2N2221A 2N2222A**

CASE 31 (TO-5) **2N2218A 2N2219A**

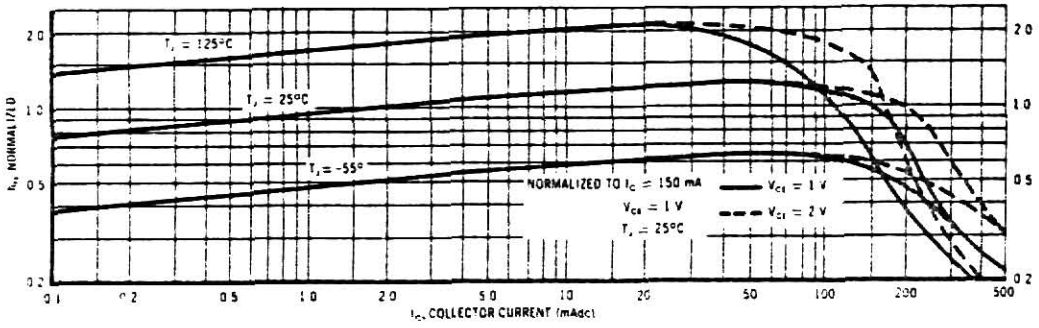
NPN silicon annular Star transistors for high-speed switching and DC to VHF amplifier applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	2N2218A 2N2219A (TO-5)	2N2221A 2N2222A (TO-18)	Unit
Collector-Base Voltage	V_{CB}	75	75	Vdc
Collector-Emitter Voltage	V_{CEO}	40	40	Vdc
Emitter-Base Voltage	V_{EB}	6	6	Vdc
Total Device Dissipation at 25°C Case Temperature Derating Factor Above 25°C	P_D	3 20	1.8 12	Watts mW/°C
Total Device Dissipation at 25°C Ambient Temperature Derating Factor Above 25°C	P_D	0.8 5.33	0.5 3.33	Watts mW/°C
Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

TYPICAL CURRENT GAIN CHARACTERISTICS



2N2218A, 2N2219A, 2N2221A , 2N2222A (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Static Characteristics		Symbol	Min	Max	Unit
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		BV_{CBO}	75	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		BV_{CEO}	40	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	6	—	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)		I_{CBO}	—	0.01	μAdc
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)			—	10	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		I_{CEX}	—	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		I_{BL}	—	20	nAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)		I_{EBO}	—	10	nAdc
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{CE(sat)}$*	—	0.3	Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	1.0	
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{BE(sat)}$*	0.6	1.2	Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	2.0	
DC Forward Current Transfer Ratio* (I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A	h_{FE}*	20	—	—
	2N2219A, 2N2222A		35	—	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		25	—	
	2N2219A, 2N2222A		50	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		35	—	
	2N2219A, 2N2222A		75	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = -55°C)	2N2218A, 2N2221A		15	—	
	2N2219A, 2N2222A		35	—	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		40	120	
	2N2219A, 2N2222A		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)	2N2218A, 2N2221A		20	—	
	2N2219A, 2N2222A		50	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		25	—	
	2N2219A, 2N2222A		40	—	

* Pulse Test ≤ 300 μs, duty cycle ≤ 2%

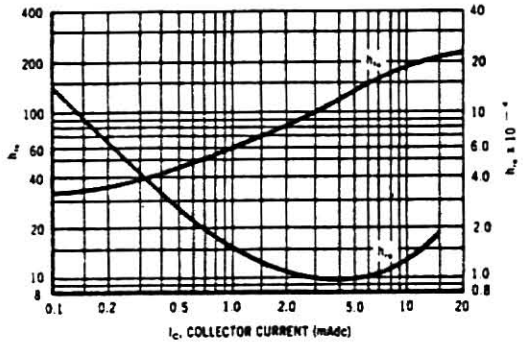
SMALL SIGNAL CHARACTERISTICS		Symbol	Min	Max	Unit
Small Signal Current Gain (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{fe}	30	150	—
	2N2219A, 2N2222A		50	300	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		50	300	
	2N2219A, 2N2222A		75	375	
Voltage Feedback Ratio (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{re}	-	5	X10^{-4}
	2N2219A, 2N2222A		-	8	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		-	2.5	
	2N2219A, 2N2222A		-	4	
Input Impedance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{ie}	1	3.5	k ohms
	2N2219A, 2N2222A		2.0	8	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		0.2	1.0	
	2N2219A, 2N2222A		0.25	1.25	
Output Admittance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{oe}	3	15	μmhos
	2N2219A, 2N2222A		5	35	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		10	100	
	2N2219A, 2N2222A		25	200	
Collector-Base Time Constant (I_C = 20 mA, V_{CE} = 20 V, f = 31.8 MHz)		r'_bC_c	-	150	ps
Noise Figure (I_C = 100 μA, V_{CE} = 10 V, Rg = 1 kΩ, f = 1 kHz)	2N2219A, 2N2222A	NF	-	4	dB

2N2218A, 2N2219A, 2N2221A , 2N2222 A (continued)

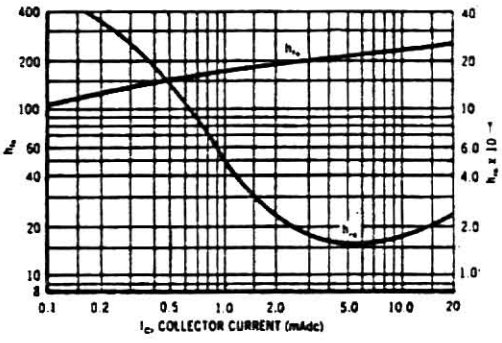
SMALL SIGNAL FORWARD CURRENT GAIN AND VOLTAGE FEEDBACK RATIO versus COLLECTOR CURRENT

$V_{CE} = 10$ V @ 1 KHz

2N2218A, 2N2221A



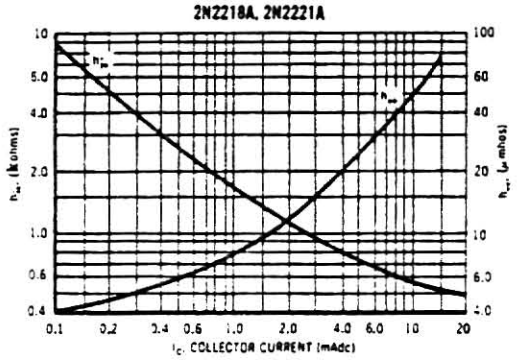
2N2219A, 2N2222A



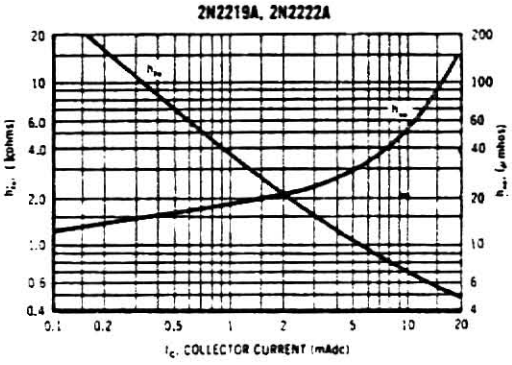
SMALL SIGNAL INPUT IMPEDANCE AND OUTPUT CONDUCTANCE versus COLLECTOR CURRENT

$V_{CE} = 10$ V @ 1 KHz

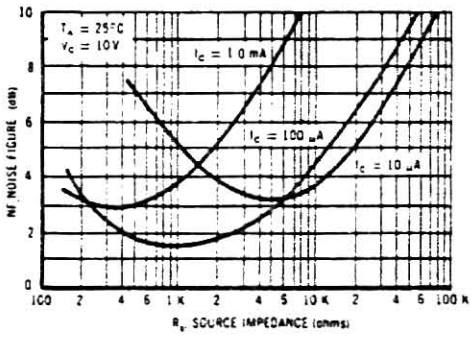
2N2218A, 2N2221A



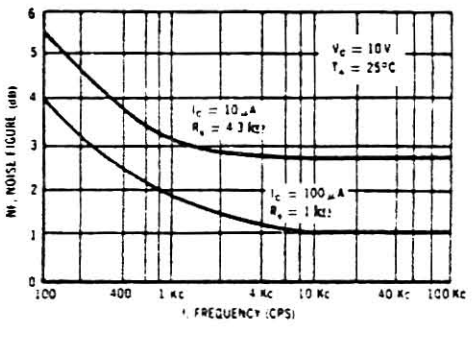
2N2219A, 2N2222A



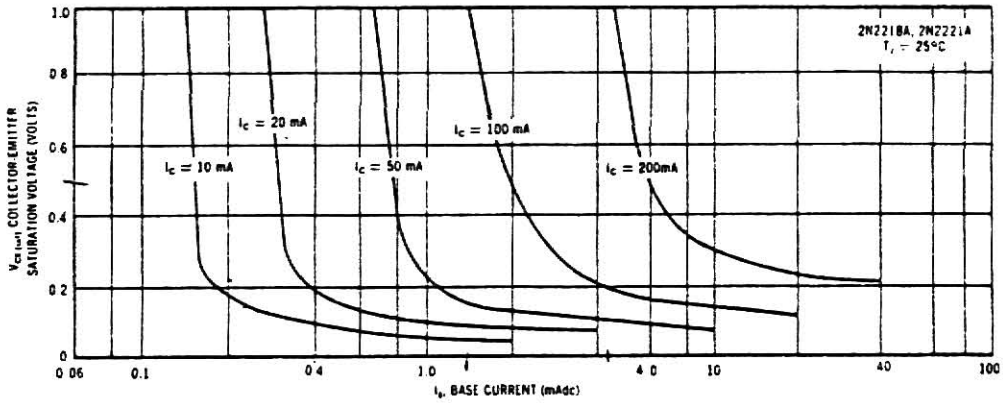
1 KC NOISE FIGURE versus SOURCE IMPEDANCE

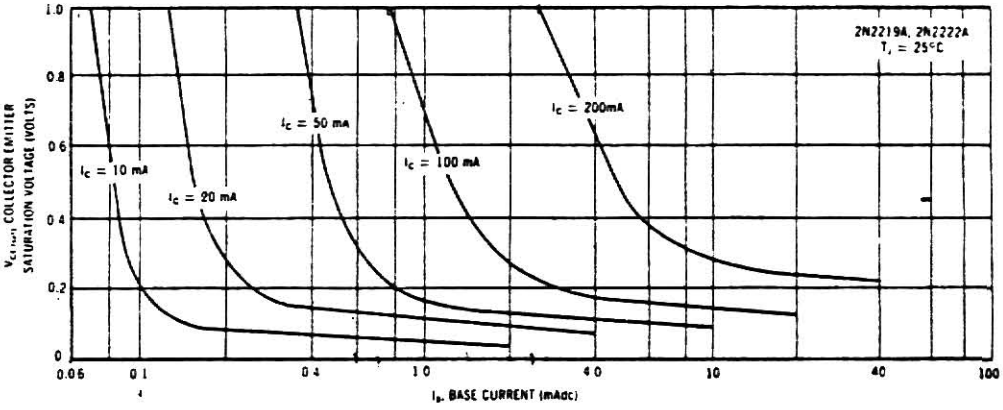


NOISE FIGURE versus FREQUENCY

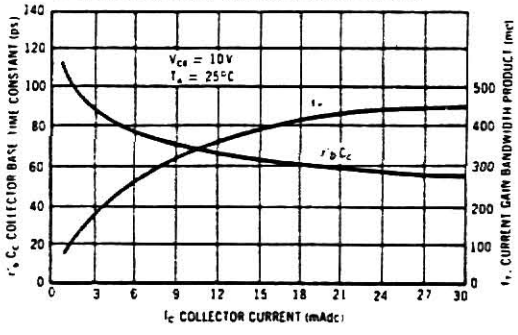


COLLECTOR SATURATION VOLTAGE versus BASE CURRENT

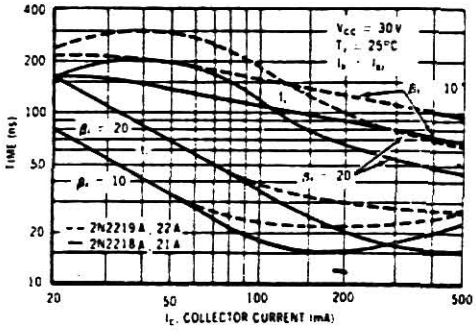




CURRENT-GAIN — BANDWIDTH PRODUCT and COLLECTOR BASE TIME CONSTANT versus COLLECTOR CURRENT



STORAGE AND FALL TIME versus COLLECTOR CURRENT



RCA MOSFET 40673

200 M Hz Mixer

Usable frequency range : upto 400 M Hz

Absolute maxium ratings # at Ta = 25 degrees C.

Drain to source volts Vds	-0.2 to +20V
Gate 1 to source volts Vg1s	+1 to -6V DC
	±6 V AC p/p
Gate 2 to source volts Vg2s	-6 to 30% of Vds DC volts
	±6 V AC p/p

Electrical charecteristics at Ta = 25 degrees C.

Typical power gain Gps	18 dB
Typical noise figure NF	3.5 dB
Noise figure and power gain test frequency	200 M Hz
Typical forward transconductance gfs	12000 umho
Maximum gate leakage current Igss	50 mA
Typical output capacitance Ciss	6 pF
Typical gate and source cutoff volts : Gate 1 Vg1s	-2 V
Gate 2 Vg2s	-2 V
Typical reverse transfer capacitance (Feedback) Crss	0.02 pF

APPENDIX C

Data sheets for Intersil ICL 8013.

Data sheets for op-amps LF 356 and uA 741.

INTERSIL

ICL8013

Four Quadrant Analog Multiplier

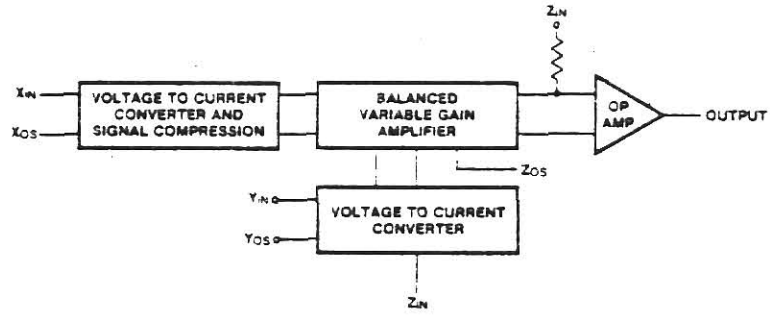
FEATURES

- **Accuracy of ±0.5% ("A" version)**
- **Full ±10V I/O voltage range**
- **1 MHz bandwidth**
- **Uses standard ±15V supplies**
- **Built in op amp provides level shifting, division and square root functions.**

GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 makes it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and systems process controls.

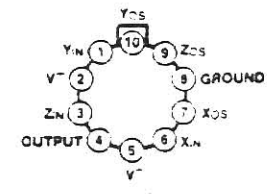
BLOCK DIAGRAM (MULTIPLIER)



ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	MULTIPLICATION ERROR		ORDER PART NUMBER
ICL8013AM	−55°C to +125°C	±.5%	MAX	ICL8013AM TZ
ICL8013BM	−55°C to +125°C	±1%		ICL8013BM TZ
ICL8013CM	−55°C to +125°C	±2%		ICL8013CM TZ
ICL8013AC	0°C to +70°C	±.5%	MAX	ICL8013AC TZ
ICL8013BC	0°C to +70°C	±1%		ICL8013BC TZ
ICL8013CC	0°C to +70°C	±2%		ICL8013CC TZ
DICE	0°C to +70°C	±2% TYP		ICL8013C/D

PIN CONFIGURATION



TOP VIEW

(outline dwg TO-100)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) ..... 500 mW
Input Voltages (X, Y, Z, X_O, Y_O, Z_O) ..... V_{SUPP}
Lead Temperature (soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C

NOTE 1: Derate at 6.8 mW/°C for operation at ambient temperature above 75°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified T_A = 25°C, V_{SUPP} = ±15V, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER	CONDITIONS	ICL8013A			ICL8013B			ICL8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	−10 < X < 10 −10 < Y < 10			.5			1.0		2.0*	2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	X = −10 X = −1		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough	X = 0 Y = $20V_{p-p}$ f = 50Hz Y = 0 X = $20V_{p-p}$ f = 50Hz			50 50			100 100		200* 150*	200 150	mV_{p-p} mV_{p-p}
Nonlinearity X Input	X = $20V_{p-p}$ Y = ±10Vdc		±0.5			±0.5			±0.8		%
Y Input	Y = $20V_{p-p}$ X = ±10Vdc		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (−3dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	V_{IN} = ±10V		1			1			1		μs
Overload Recovery (to ±2% of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance X Input			10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current X or Y Input			2	5			7.5			10	μA
Z Input			25			25			25		μA
Power Supply Variation Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	−10 < X < 10, −10 < Y < 10		1.5			2			3		% Full Scale
Average Temperature Coefficient of Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current X or Y Input				5			5			10	μA
Z Input				25			25			35	μA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	$R_L \geq 2k$ C_L < 1000 pF		±10			±10			±10		V

CIRCUIT DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 1.

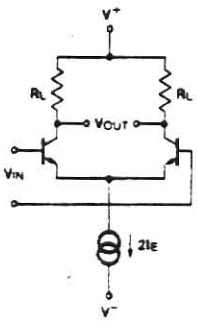


Figure 1: Differential Amplifier

The small signal differential voltage gain of this circuit is given by

$$AV = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{I}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN} \frac{R_L}{r_e} = V_{IN} \cdot \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 2, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D = \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y} (V_X \cdot V_Y)$$

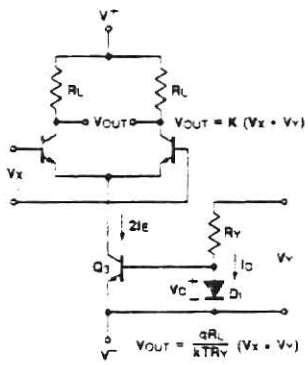


Figure 2: Transconductance Multiplier

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D

2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 3, uses another differential pair but with considerable emitter degeneration. In this circuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

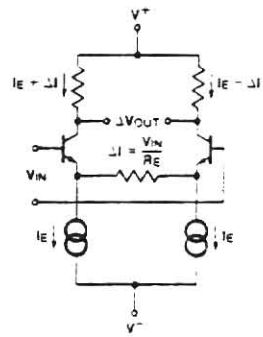


Figure 3: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 4A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 4A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.

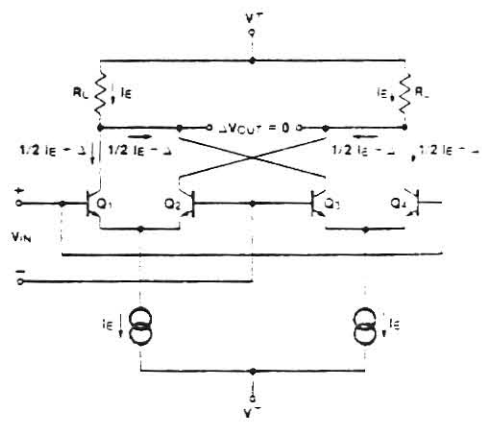


Figure 4A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

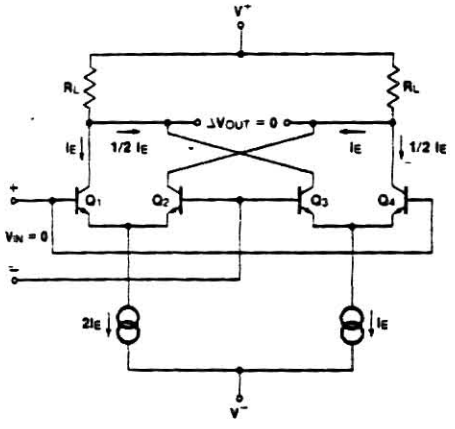


Figure 4B: No Input Signal with Unbalanced Current Sources
Δ VOUT = 0V

In Figure 4B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 4C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 3 we have a balanced multiplier circuit capable of four quadrant operation (Figure 5).

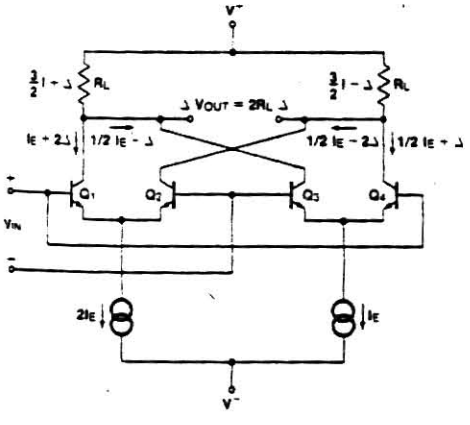


Figure 4C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

This circuit of Fig. 5 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.

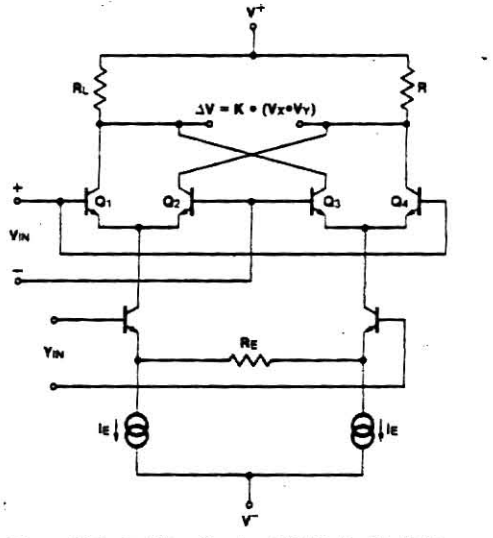


Figure 5: Typical Four Quadrant Multiplier-Modulator

Figure 3 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Fig. 6A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 6A is the

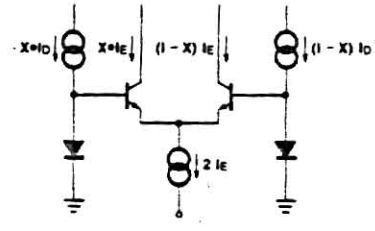


Figure 6A: Current Gain Cell

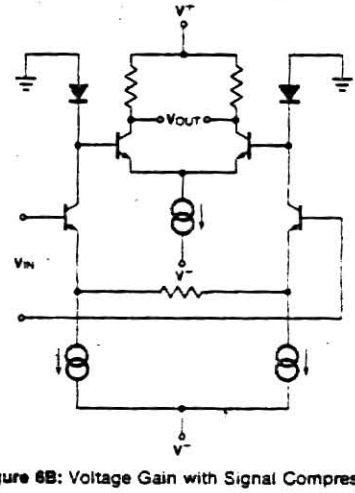


Figure 6B: Voltage Gain with Signal Compression

difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Fig. 3, we have Fig. 6B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 7. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

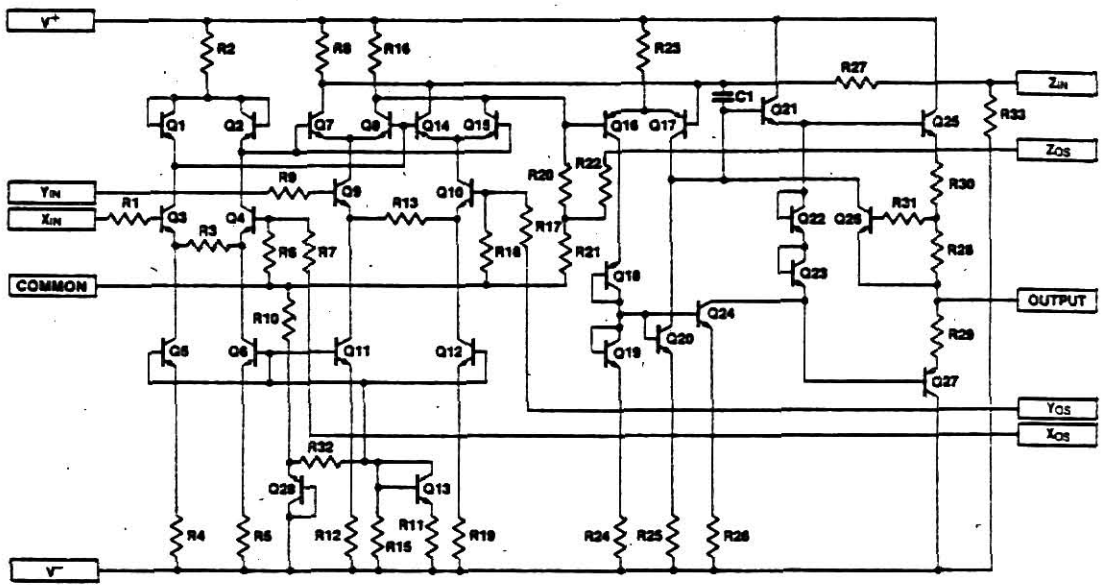


Figure 7: ICL8013 Schematic

MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

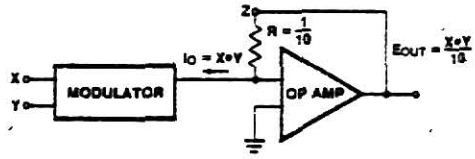


Figure 8A: Multiplier Block Diagram

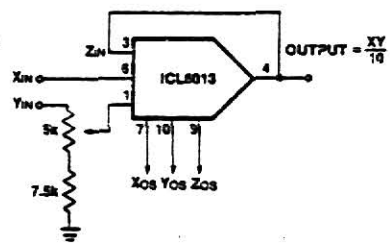


Figure 8B: Actual Circuit Connection

MULTIPLIER Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a ±10V low frequency (≤100Hz) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With X_{IN} = 10.0V DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output − Y_{IN}) = Zero.

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X \cdot Y = \frac{Z}{R} = 10Z$$

$$\text{Since } Y = E_{OUT},\ E_{OUT} = \frac{10Z}{X}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

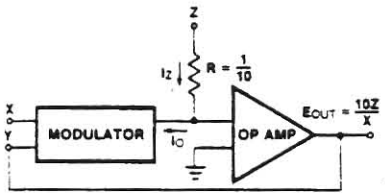


Figure 9A: Division Block Diagram

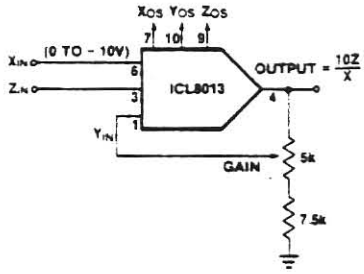


Figure 9B: Actual Circuit Connection

DIVIDER Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With Z_{IN} = 0V, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from −10V through −1V.
3. With Z_{IN} = 0V and X_{IN} = −10.0V adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from −10V to −1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN} = X_{IN}$ (and/or $Z_{IN} = -X_{IN}$) adjust the gain control until the output is the closest average around −10.0V (−10V for $Z_{IN} = -X_{IN}$) as X_{IN} is varied from −10V to −3V.

SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2 \omega = 1/2 (\cos 2\omega + 1)$.

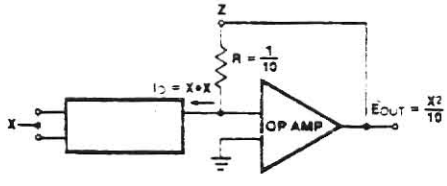


Figure 10A: Squarer Block Diagram

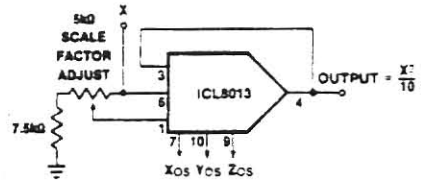


Figure 10B: Actual Circuit Connection

SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X \bullet Y = (-E_{OUT})^2 = 10Z$$

$$E_{OUT} = -\sqrt{10Z}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

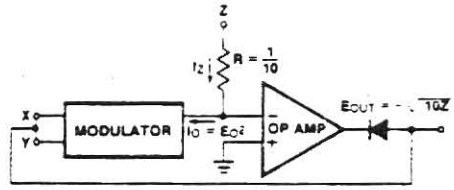


Figure 11A: Square Root Block Diagram

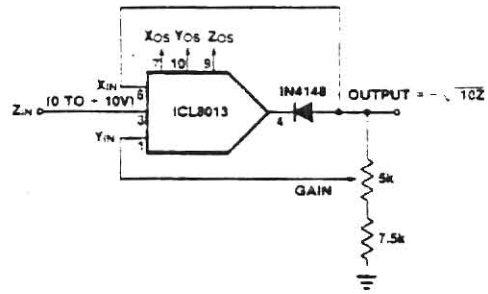


Figure 11B: Actual Circuit Connection

SQUARE ROOT Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

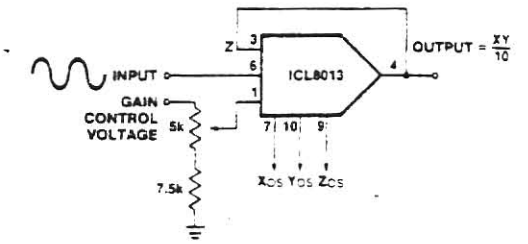
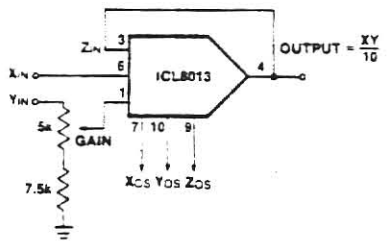


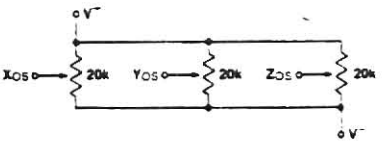
Figure 12: Variable Gain Amplifier

TYPICAL APPLICATIONS

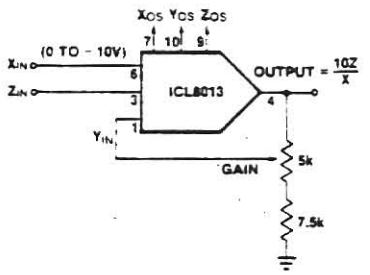
MULTIPLICATION



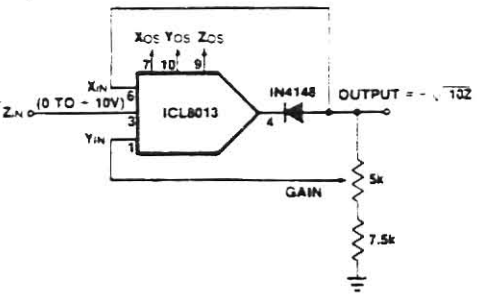
POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH



DIVISION

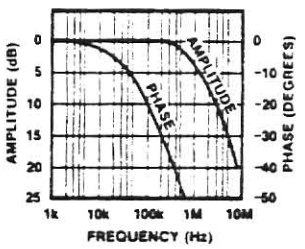


SQUARE ROOT

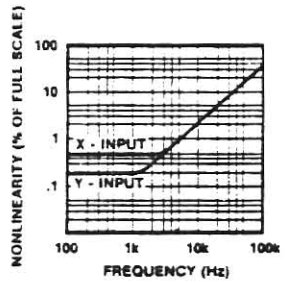


TYPICAL PERFORMANCE CURVES

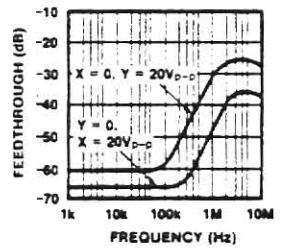
AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



NONLINEARITY AS A FUNCTION OF FREQUENCY



FEEDTHROUGH AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

LF155/LF156/LF157

Monolithic JFET Input Operational Amplifiers

DISTINCTIVE CHARACTERISTICS

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000pF) without stability problems
- Internal compensation and large differential input voltage capability

GENERAL DESCRIPTION

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

The LF155, LF156, LF157 series are direct replacements for National LF155, LF156, LF157 series.

COMMON FEATURES
(LF155A, LF156A, LF157A)

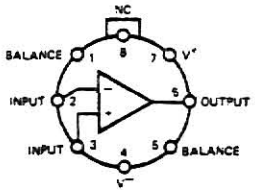
Low input bias current	30pA
Low input offset current	3.0pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1.0mV
Low input offset voltage temperature drift	3.0μV/°C
Low input noise current	0.01pA/√Hz
High common-mode rejection ratio	100dB
Large dc voltage gain	106dB

UNCOMMON FEATURES

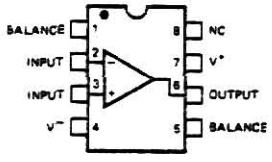
	LF155A	LF156A	LF157A (A_V = 5)	Units
Extremely fast settling time to 0.01%	4.0	1.5	1.5	μs
Fast slew rate	5.0	12	50	V/μs
Wide gain bandwidth	2.5	5.0	20	MHz
Low input noise voltage	20	12	12	nV/√Hz

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



Notes: 1. On Dual-In-Line Pin 1 is marked for orientation.
2. On Metal Can Pin 4 is connected to case.

LIC-714

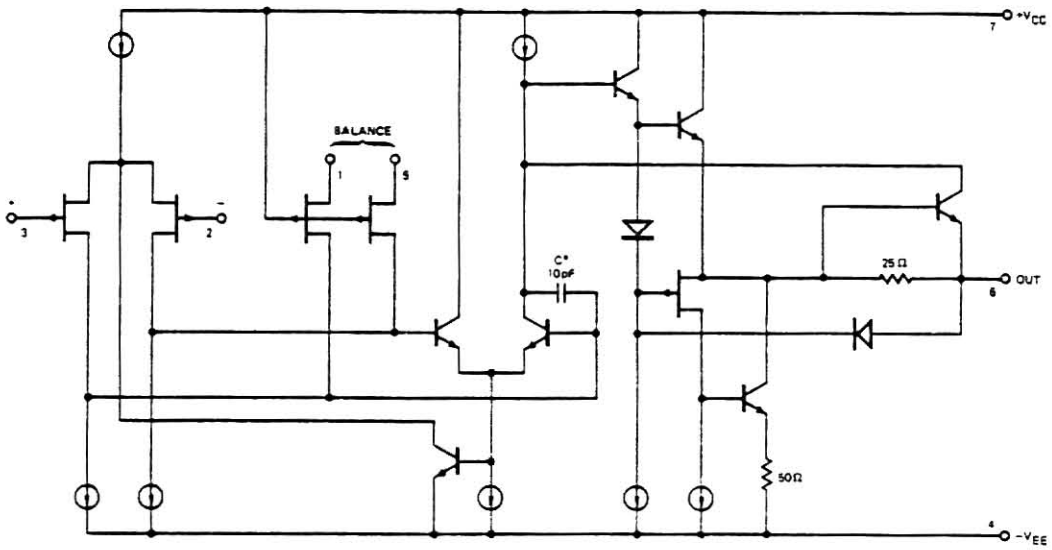
APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
LF355	Metal Can	0°C to +70°C	LF355H
	Molded DIP	0°C to +70°C	LF355N
	Dice	0°C to +70°C	LD355
LF255	Metal Can	−25°C to +85°C	LF255H
LF155	Metal Can	−55°C to +125°C	LF155H
	Dice	−55°C to +125°C	LD155
LF355A	Metal Can	0°C to +70°C	LF355AH
	Dice	0°C to +70°C	LD355A
LF155A	Metal Can	−55°C to +125°C	LF155AH
	Dice	−55°C to +125°C	LD155A
LF356	Metal Can	0°C to +70°C	LF356H
	Molded DIP	0°C to +70°C	LF356N
	Dice	0°C to +70°C	LD356
LF256	Metal Can	−25°C to +85°C	LF256H
LF156	Metal Can	−55°C to +125°C	LF156H
	Dice	−55°C to +125°C	LD156
LF356A	Metal Can	0°C to +70°C	LF356AH
	Dice	0°C to +70°C	LD356A
LF156A	Metal Can	−55°C to +125°C	LF156AH
	Dice	−55°C to +125°C	LD156A
LF357	Metal Can	0°C to +70°C	LF357H
	Molded DIP	0°C to +70°C	LF357N
	Dice	0°C to +70°C	LD357
LF257	Metal Can	−25°C to +85°C	LF257H
LF157	Metal Can	−55°C to +125°C	LF157H
	Dice	−55°C to +125°C	LD157
LF357A	Metal Can	0°C to +70°C	LF357AH
	Dice	0°C to +70°C	LD357A
LF157A	Metal Can	−55°C to +125°C	LF157AH
	Dice	−55°C to +125°C	LD157A

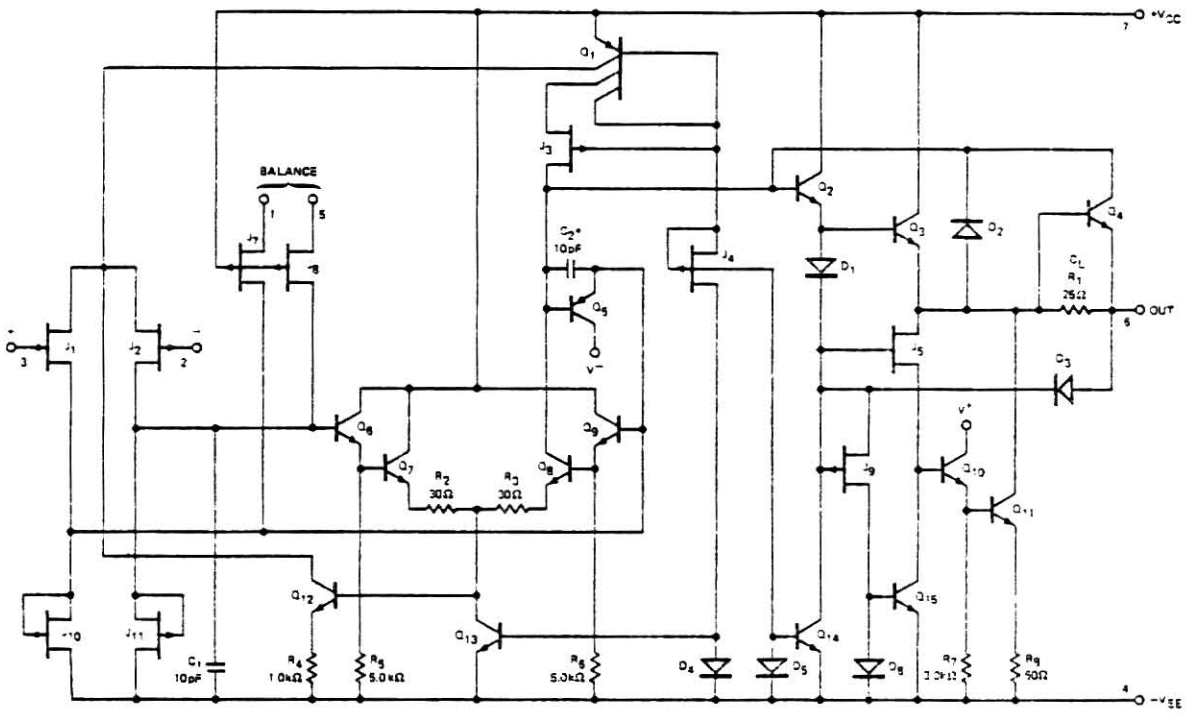
SIMPLIFIED SCHEMATIC



*C = 2pF on LF157

LIC-715

DETAILED SCHEMATIC



*C = 2pF on LF157

LIC-716

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF155/6/7	LF255/6/7	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H Package)	670mW	670mW	570mW	500mW
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
T_J(Max.)	150°C	150°C	115°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Note 3)

DC CHARACTERISTICS

Parameters	Description	Test Conditions	LF155A/6A/7A Min.	Typ.	Max.	LF355A/6A/7A Min.	Typ.	Max.	Units
V_{OS}	Input Offset Voltage	R_S = 50Ω, T_A = 25°C		1.0	2.0		1.0	2.0	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 50Ω		3.0	5.0		3.0	5.0	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S = 50Ω, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_J = 25°C, (Note 3, 5)		3.0	10		3.0	10	pA
		$T_J \leq T_{HIGH}$			10			1.0	nA
I_B	Input Bias Current	T_J = 25°C, (Notes 3, 5)		30	50		30	50	pA
		$T_J < T_{HIGH}$			25			5.0	nA
R_{IN}	Input Resistance	T_J = 25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	200		50	200		V/mV
		V_O = ±10V, R_L = 2kΩ Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±13		±12	±13		Volts
		V_S = ±15V, R_L = 2kΩ	±10	±12		±10	±12		Volts
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15.1 −12		±11	+15.1 −12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

AC CHARACTERISTICS (T_A = 25°C, V_S = ±15V)

Parameters	Description	Test Conditions	LF155A/355A Min.	Typ.	Max.	LF156A/356A Min.	Typ.	Max.	LF157A/357A Min.	Typ.	Max.	Units
SR	Slew Rate	LF155A/6A: A_V = 1	3.0	5.0		10	12					V/µs
		LF157A: A_V = 5							40	50		V/µs
GBW	Gain-Bandwidth Product			2.5		4.0	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4.0			1.5			1.5		µs
e_n	Equivalent Input Noise Voltage	R_S = 100Ω f = 100Hz		25			15			15		nV/√Hz
		f = 1000Hz		20			12			12		
i_n	Equivalent Input Noise Current	f = 100Hz		0.01			0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01			0.01		
C_{IN}	Input Capacitance			3.0			3.0			3.0		pF

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

DC CHARACTERISTICS (Note 3)

Parameters	Description	Test Conditions	LF155/6/7 Min.	LF155/6/7 Typ.	LF155/6/7 Max.	LF255/6/7 Min.	LF255/6/7 Typ.	LF255/6/7 Max.	LF355/6/7 Min.	LF355/6/7 Typ.	LF355/6/7 Max.	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^\circ C$		3.0	5.0		3.0	5.0		3.0	10	mV
		Over Temperature			7.0			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5.0			5.0			5.0		$\mu V/^\circ C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/^\circ C$ per mV
I_{OS}	Input Offset Current	$T_J = 25^\circ C$, (Notes 3, 5)		3.0	20		3.0	20		3.0	50	pA
		$T_J \leq T_{HIGH}$			20			1.0			2.0	nA
I_B	Input Bias Current	$T_J = 25^\circ C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5.0			8.0	nA
R_{IN}	Input Resistance	$T_J = 25^\circ C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25^\circ C$	50	200		50	200		25	200		V/mV
		$V_O = \pm 10V$, $R_L = 2k\Omega$ Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	± 12	± 13		± 12	± 13		± 12	± 13		Volts
		$V_S = \pm 15V$, $R_L = 2k\Omega$	± 10	± 12		± 10	± 12		± 10	± 12		Volts
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	$+15.1$ -12			$+15.1$ -12		± 11	$+15.1$ -12		Volts
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC CHARACTERISTICS ($T_A = 25^\circ C$, $V_S = \pm 15V$)

Parameters	LF155A/355A LF155/255 Typ.	LF155A/355A LF155/255 Max.	LF355 Typ.	LF355 Max.	LF156A LF156/256 Typ.	LF156A LF156/256 Max.	LF356A/356 Typ.	LF356A/356 Max.	LF157A LF157/257 Typ.	LF157A LF157/257 Max.	LF357A/357 Typ.	LF357A/357 Max.	Units
Supply Current	2.0	4.0	2.0	4.0	5.0	7.0	5.0	10	5.0	7.0	5.0	10	mA

AC CHARACTERISTICS ($T_A = 25^\circ C$, $V_S = \pm 15V$)

Parameters	Description	Test Conditions	LF155/255/ LF355 Typ.	LF156/256 Min.	LF156/256/ LF356 Typ.	LF157/257 Min.	LF157/257 LF357 Typ.	Units
SR	Slew Rate	LF155/6: $A_V = 1$,	5.0	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain-Bandwidth Product		2.5		5.0		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4.0		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000Hz	20		12		12	
i_n	Equivalent Input Noise Current	f = 100Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000Hz	0.01		0.01		0.01	
C_{IN}	Input Capacitance		3.0		3.0		3.0	pF

Notes: 1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.

2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

3. These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55^\circ C \leq T_A \leq +125^\circ C$ and $T_{HIGH} = +125^\circ C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25^\circ C \leq T_A \leq +85^\circ C$ and $T_{HIGH} = 85^\circ C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0^\circ C \leq T_A \leq +70^\circ C$ and $T_{HIGH} = +70^\circ C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

4. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

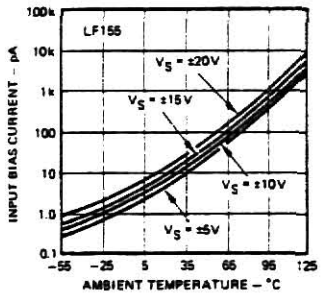
5. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_j = T_A + \Theta_{jA} P_d$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

6. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

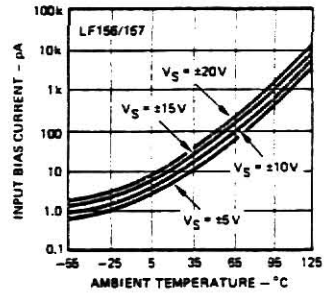
7. Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

TYPICAL DC PERFORMANCE CHARACTERISTICS

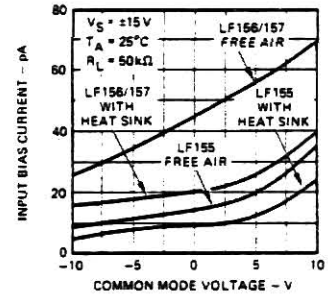
Input Bias Current



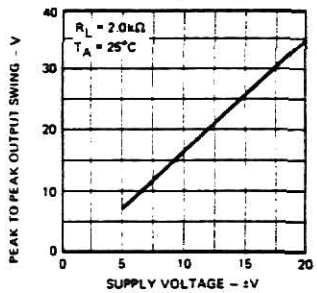
Input Bias Current



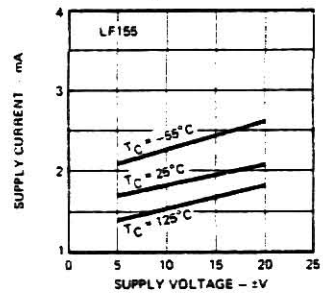
Input Bias Current



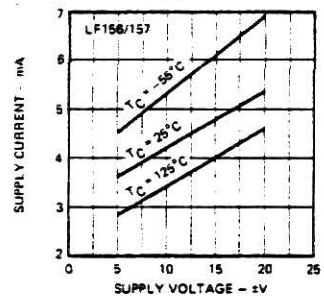
Voltage Swing



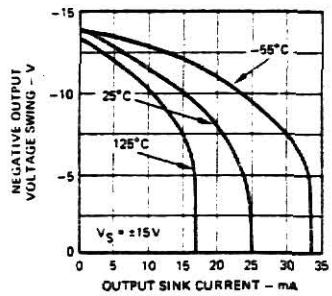
Supply Current



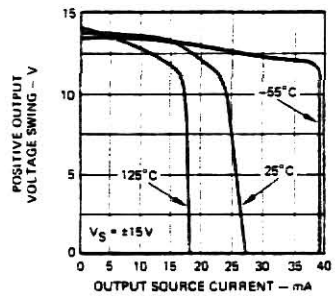
Supply Current



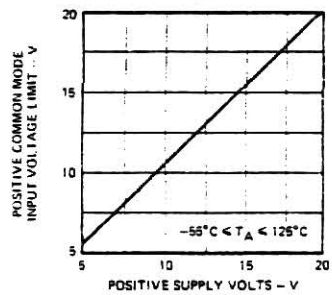
Negative Current Limit



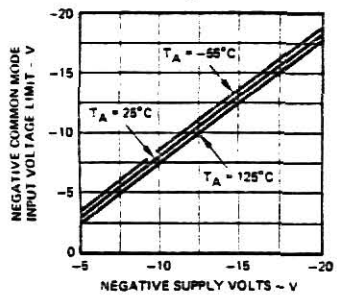
Positive Current Limit



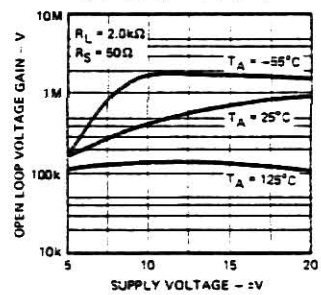
Positive Common-Mode Input Voltage Limit



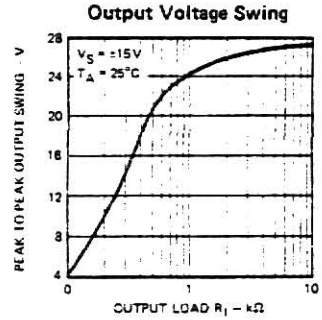
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



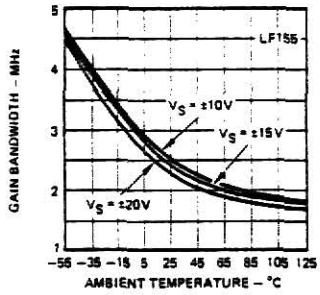
Output Voltage Swing

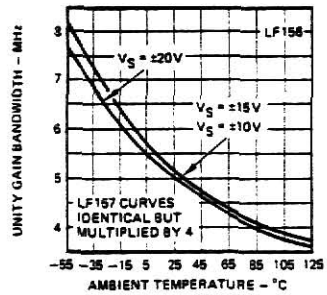


LIC-717

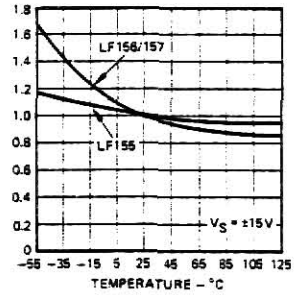
TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

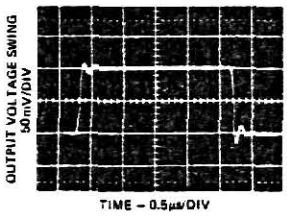




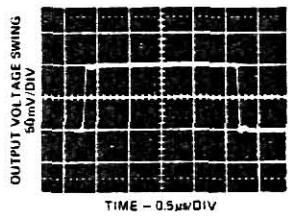
Normalized Slew Rate



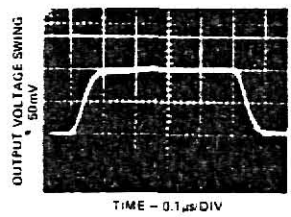
LF155 *Small Signal Pulse* Response, A_V = +1



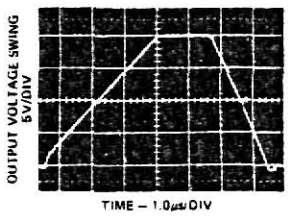
LF156 Small Signal Pulse Response, A_V = +1



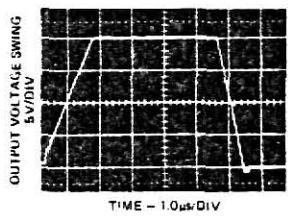
LF157 Small Signal Pulse Response, A_V = +5



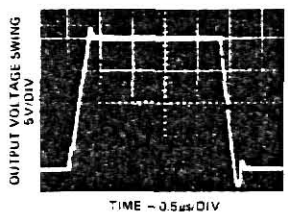
LF155 Large Signal Pulse Response, A_V = +1



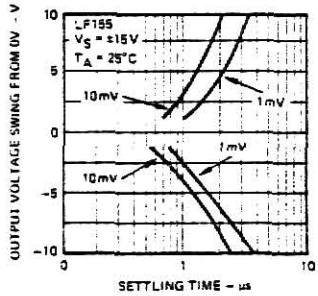
LF156 Large Signal Pulse Response, A_V = +1



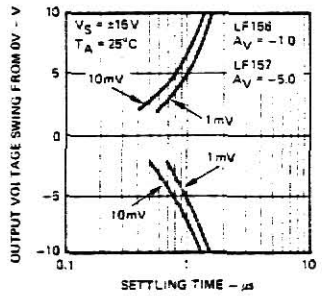
LF157 Large Signal Pulse Response, A_V = +5



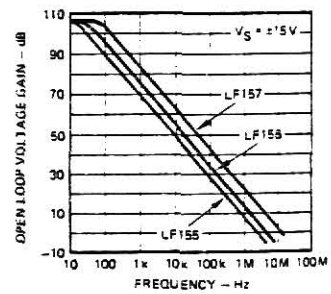
Inverter Settling Time



Inverter Settling Time

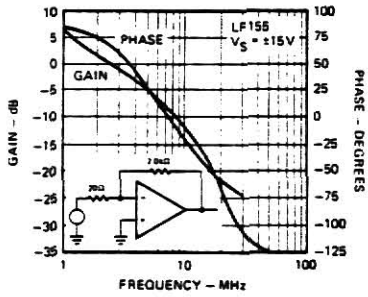


Open Loop Frequency Response

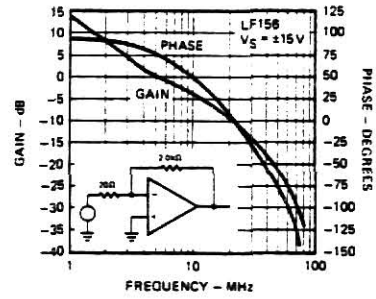


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont.)

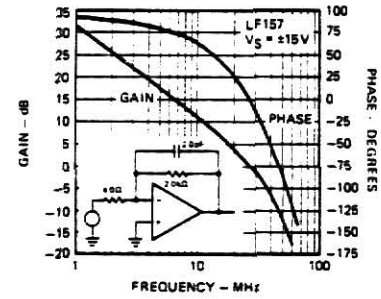
Bode Plot



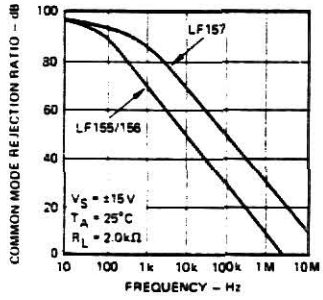
Bode Plot



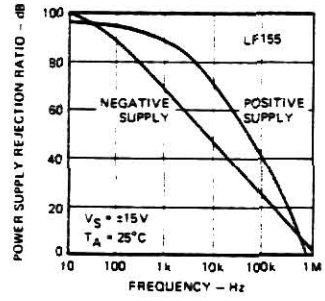
Bode Plot



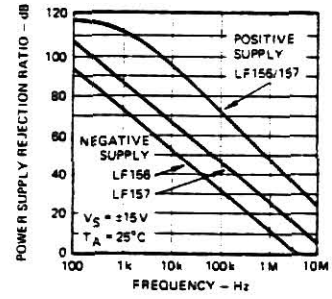
Common-Mode Rejection Ratio



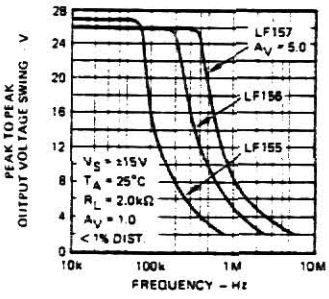
Power Supply Rejection Ratio



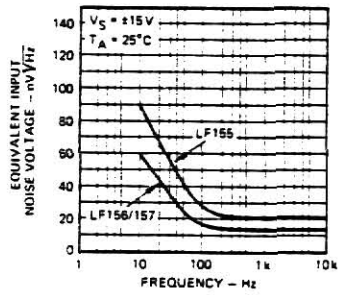
Power Supply Rejection Ratio



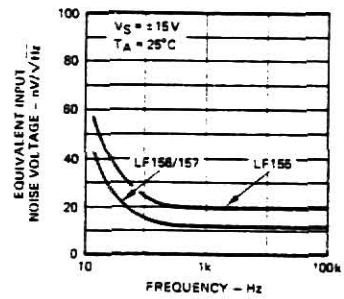
Undistorted Output Voltage Swing



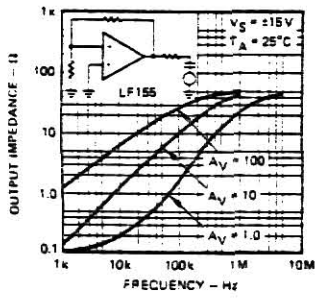
Equivalent Input Noise Voltage



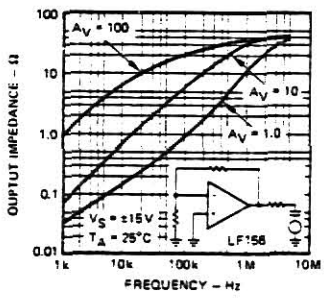
Equivalent Input Noise Voltage (Expanded Scale)



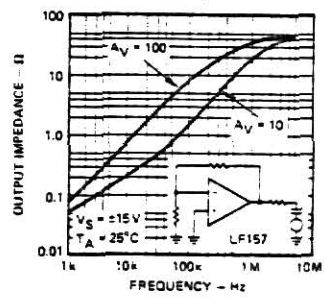
Output Impedance



Output Impedance



Output Impedance



LIC-719

µA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

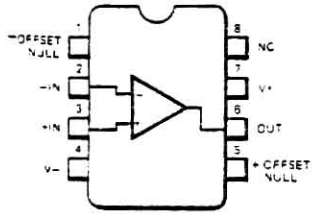
GENERAL DESCRIPTION — The µA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the µA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
µA741A, µA741, µA741E	±22 V
µA741C	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Molded and Hermetic DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Hermetic DIP, and Flatpak	−65°C to +150°C
Mini DIP, Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (µA741A, µA741)	−55°C to +125°C
Commercial (µA741E, µA741C)	0°C to +70°C
Pin Temperature (Soldering)	
Metal Can, Hermetic DIPs, and Flatpak (60 s)	300°C
Molded DIPs (10 s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

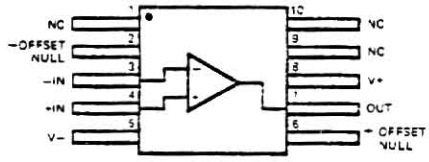
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES R T



ORDER INFORMATION

TYPE	PART NO.
µA741C	µA741TC
µA741C	µA741RC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F

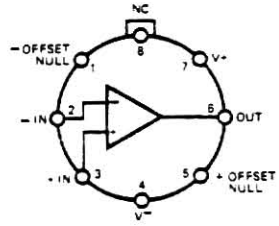


ORDER INFORMATION

TYPE	PART NO.
µA741A	µA741AFM
µA741	µA741FM

CONNECTION DIAGRAMS

8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B
PACKAGE CODE H

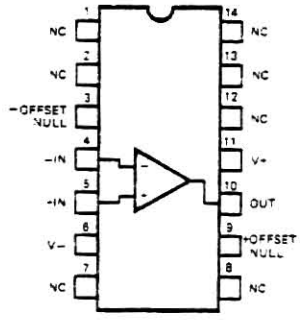


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
µA741A	µA741AHM
µA741	µA741HM
µA741E	µA741EHC
µA741C	µA741HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
µA741A	µA741ADM
µA741	µA741DM
µA741E	µA741EDC
µA741C	µA741DC
µA741C	µA741PC

μA741A

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift						0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		$V_S = +20, -20$; $V_S = -20, +10V$, $R_S = 50\Omega$			15	50	μV/V
Output Short Circuit Current				10	25	40	mA
Power Dissipation		$V_S = \pm 20V$			80	150	mW
Input Impedance		$V_S = \pm 20V$		1.0	6.0		MΩ
Large Signal Voltage Gain		$V_S = \pm 20V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 15V$		50			V/mV
Transient Response	Rise Time				0.25	0.8	μs
(Unity Gain)	Overshoot				6.0	20	%
Bandwidth (Note 4)				.437	1.5		MHz
Slew Rate (Unity Gain)		$V_{IN} = \pm 10V$		0.3	0.7		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Common Mode Rejection Ratio		$V_S = \pm 20V$, $V_{IN} = \pm 15V$, $R_S = 50\Omega$		80	95		dB
Adjustment For Input Offset Voltage		$V_S = \pm 20V$		10			mV
Output Short Circuit Current				10		40	mA
Power Dissipation		$V_S = \pm 20V$	$-55°C$			165	mW
			$+125°C$			135	mW
Input Impedance		$V_S = \pm 20V$		0.5			MΩ
Output Voltage Swing		$V_S = \pm 20V$,	$R_L = 10k\Omega$	±16			V
			$R_L = 2k\Omega$	±15			V
Large Signal Voltage Gain		$V_S = \pm 20V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 15V$		32			V/mV
		$V_S = \pm 5V$, $R_L = 2k\Omega$, $V_{OUT} = \pm 2$ V		10			V/mV

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for the metal can, 8.3mW/°C for the DIP and 7.1mW/°C for the Flatpak.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.
4. Calculated value from: $BW(MHz) = \frac{0.35}{\text{Rise Time } (\mu s)}$

μA741

ELECTRICAL CHARACTERISTICS: V_S = ±15 V, T_A = 25°C unless otherwise specified.

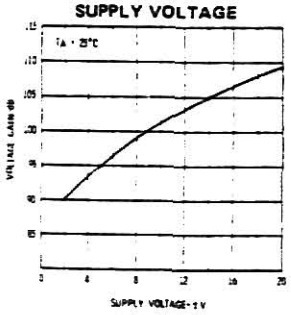
CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	50,000	200,000		
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	V_{IN} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2\ k\Omega$		0.5		V/μs

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

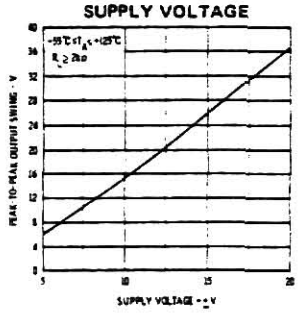
Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	6.0	mV
Input Offset Current		T_A = +125°C		7.0	200	nA
		T_A = −55°C		85	500	nA
Input Bias Current		T_A = +125°C		0.03	0.5	μA
		T_A = −55°C		0.3	1.5	μA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	25,000			
Output Voltage Swing		$R_L \geq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Supply Current		T_A = +125°C		1.5	2.5	mA
		T_A = −55°C		2.0	3.3	mA
Power Consumption		T_A = +125°C		45	75	mW
		T_A = −55°C		60	100	mW

TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

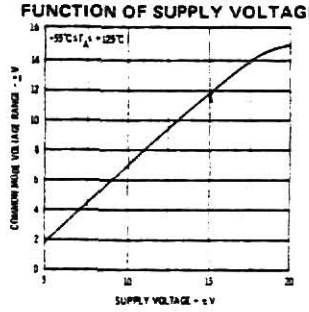
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

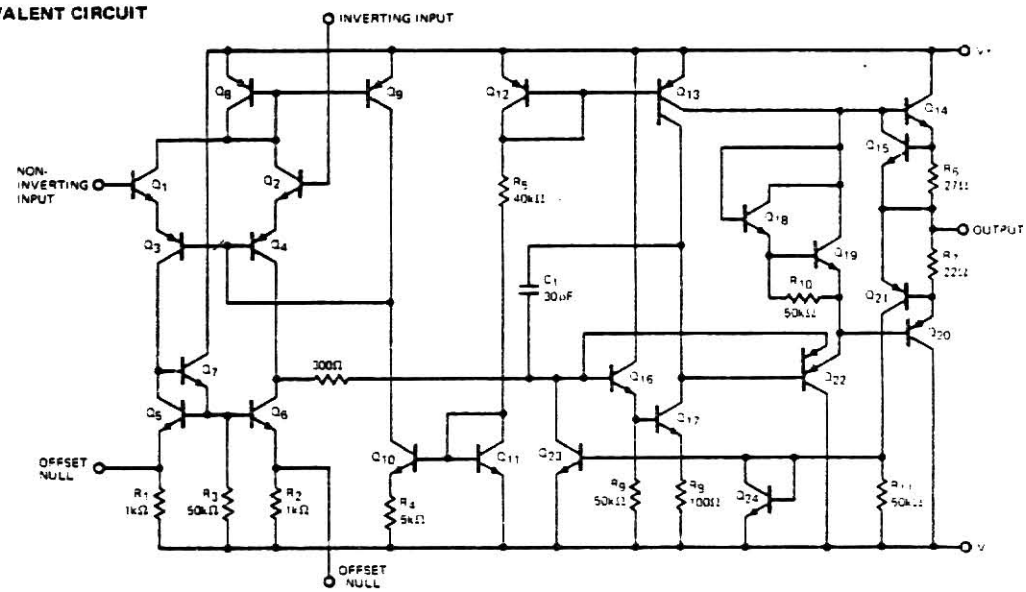


μA741E

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

CHARACTERISTICS (see definitions)		CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50\Omega$			0.8	3.0	mV
Average Input Offset Voltage Drift						15	μV/°C
Input Offset Current					3.0	30	nA
Average Input Offset Current Drift						0.5	nA/°C
Input Bias Current					30	80	nA
Power Supply Rejection Ratio		$V_S = +10, -20$; $V_S = +20, -10$V, $R_S = 50\Omega$			15	50	μV/V
Output Short Circuit Current				10	25	40	mA
Power Dissipation		$V_S = \pm 20$V			80	150	mW
Input Impedance		$V_S = \pm 20$V		1.0	6.0		MΩ
Large Signal Voltage Gain		$V_S = \pm 20$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 15$V		50			V/mV
Transient Response	Rise Time				0.25	0.8	μs
(Unity Gain)	Overshoot				6.0	20	%
Bandwidth (Note 4)				.437	1.5		MHz
Slew Rate (Unity Gain)		$V_{IN} = \pm 10$V		0.3	0.7		V/μs
The following specifications apply for $0°C \leq T_A \leq 70°C$							
Input Offset Voltage						4.0	mV
Input Offset Current						70	nA
Input Bias Current						210	nA
Common Mode Rejection Ratio		$V_S = \pm 20$V, $V_{IN} = \pm 15$V, $R_S = 50\Omega$		80	95		dB
Adjustment For Input Offset Voltage		$V_S = \pm 20$V		10			mV
Output Short Circuit Current				10		40	mA
Power Dissipation		$V_S = \pm 20$V				150	mW
Input Impedance		$V_S = \pm 20$V		0.5			MΩ
Output Voltage Swing		$V_S = \pm 20$V,	$R_L = 10k\Omega$	±16			V
			$R_L = 2k\Omega$	±15			V
Large Signal Voltage Gain		$V_S = \pm 20$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 15$V		32			V/mV
		$V_S = \pm 5$V, $R_L = 2k\Omega$, $V_{OUT} = \pm 2$ V		10			V/mV

EQUIVALENT CIRCUIT



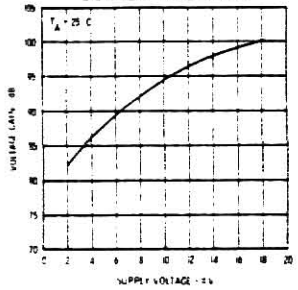
μA741C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

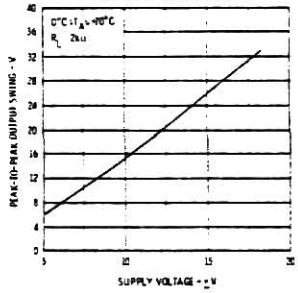
CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	20,000	200,000		
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Rise time	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Input Offset Voltage					7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000			
Output Voltage Swing		$R_L \geq 2$ kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

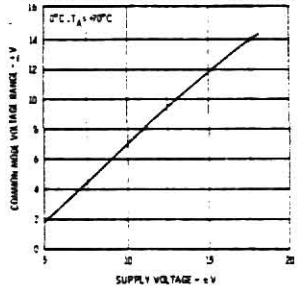
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

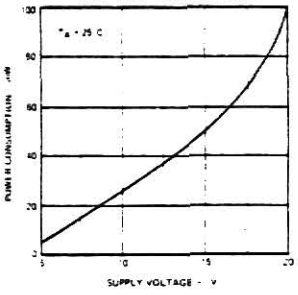


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

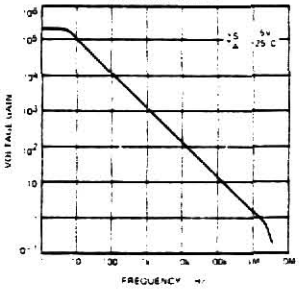


TYPICAL PERFORMANCE CURVES FOR μA741A, μA741, μA741E AND μA741C

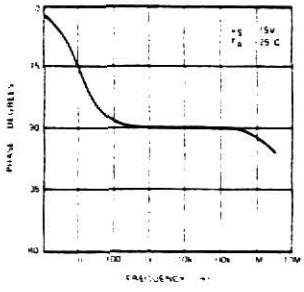
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



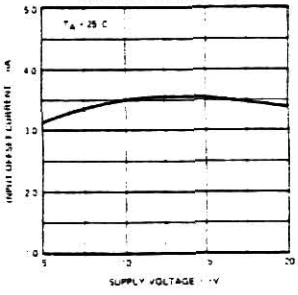
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



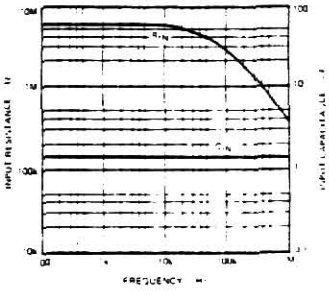
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



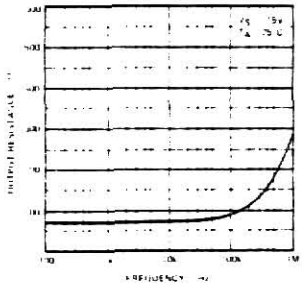
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



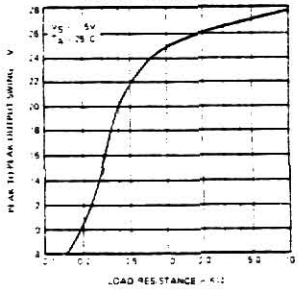
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



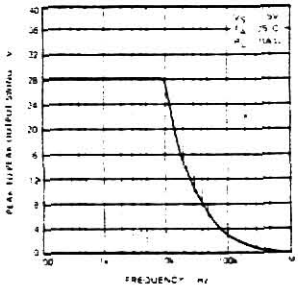
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



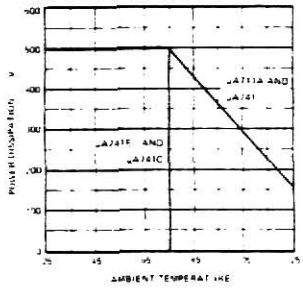
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



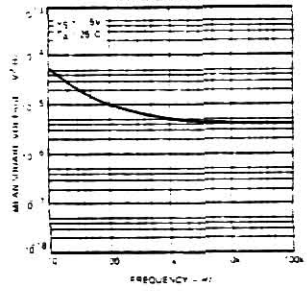
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



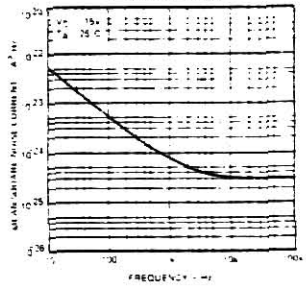
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



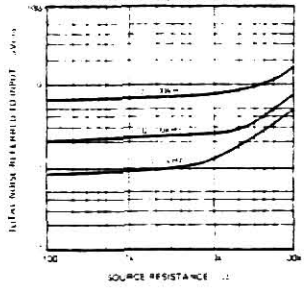
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

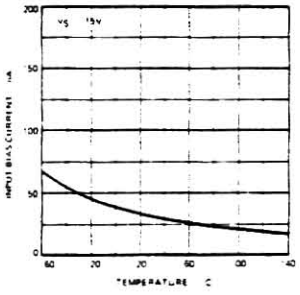


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

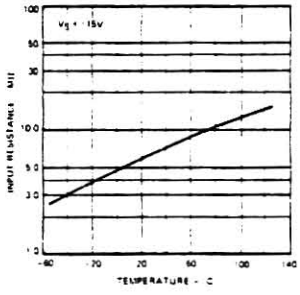


TYPICAL PERFORMANCE CURVES FOR μA741A AND μA741

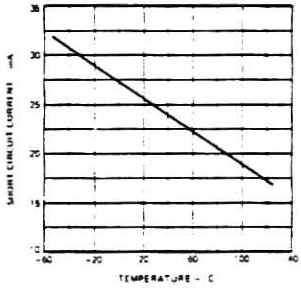
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



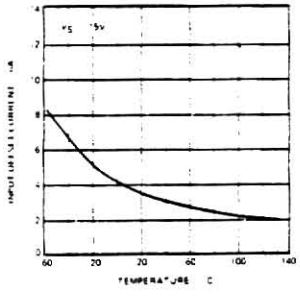
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



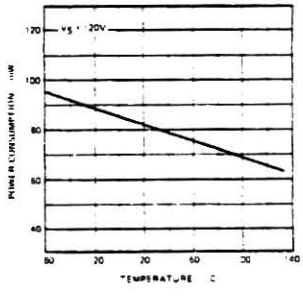
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



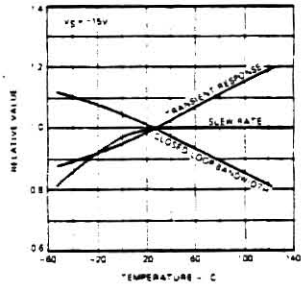
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

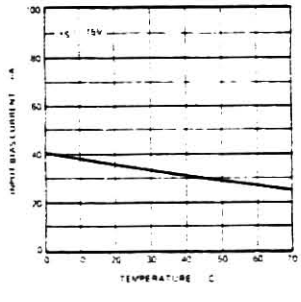


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

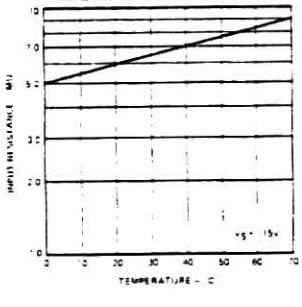


TYPICAL PERFORMANCE CURVES FOR μA741E AND μA741C

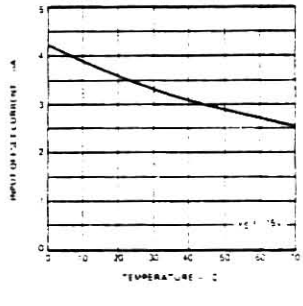
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



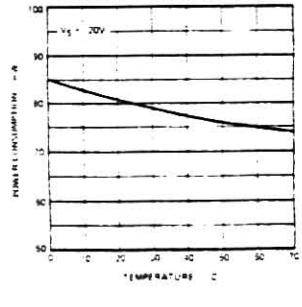
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



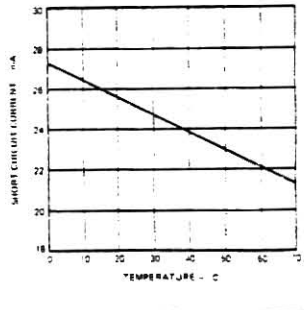
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



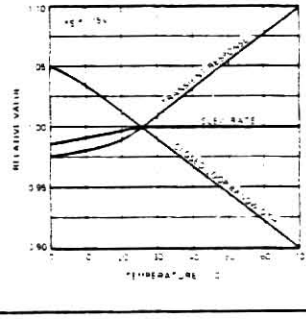
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



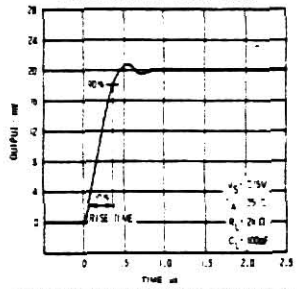
OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



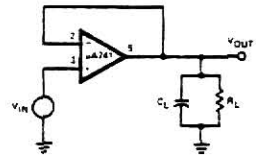
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



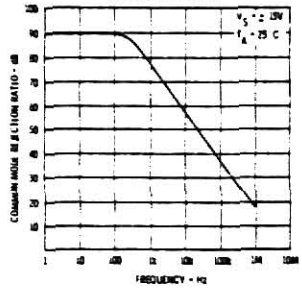
TRANSIENT RESPONSE



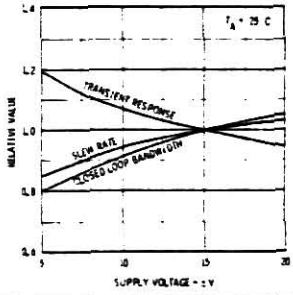
TRANSIENT RESPONSE TEST CIRCUIT



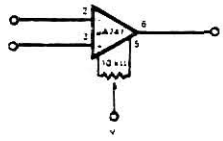
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



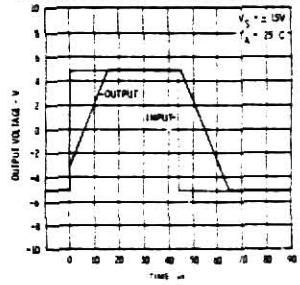
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

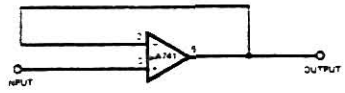


VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



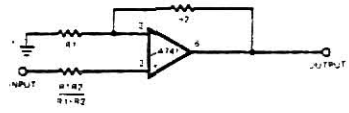
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



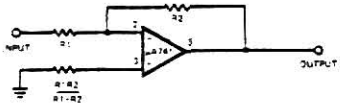
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{OUT} << 1 Ω
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



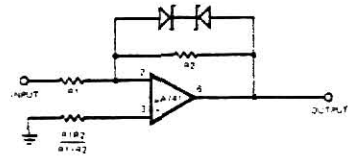
GAIN	R1	R2	B W	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	290 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R1	R2	B W	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER



$$\frac{E_{OUT}}{E_{IN}} = \frac{R2}{R1} \text{ if } |E_{OUT}| \leq V_Z + 0.7\ V$$

where V_Z = Zener breakdown voltage

APPENDIX D

Software program listing for the digital technique.

```
 TYPE SINGEN.FOR
C
C THIS PROGRAM GENERATES A SINE WAVE FOR A SELECTED AMPLITUDE
C AND FOR A DESIRED VALUE OF FREQUENCY FROM 0 TO 100 K HZ.
C
        INTEGER Z(500)
        REAL Y(500)
C
C MENU FOR THE PROGRAM
C
        TYPE 10
10      FORMAT(10X,'ENTER SAMPLING TIME BETWEEN SAMPLES')
        ACCEPT 20,ITIME
20      FORMAT(I6)
        TYPE 30
30      FORMAT(10X,'ENTER # OF DIVISIONS / CYCLE <=500 ')
        ACCEPT 40,LIMIT
40      FORMAT(I5)
        TYPE 50
50      FORMAT(10X,'ENTER THE AMPLITUDE SCALE : 0<SCALE<=1')
        ACCEPT 60,S
60      FORMAT(F5.3)
C
C LOAD THE MEMORY WITH AMPLITUDE VALUES
C SCALE THE AMPLITUDE VALUES FOR DAC CONVERSION
C
        DO 80 I=1,LIMIT
        X = (2*3.14159/LIMIT)*(I-1)
        Y(I) = SIN(X)*S
        W = (Y(I)+1)/2*4095
        Z(I) = INT(W)
        TYPE 70,Y(I),Z(I)
70      FORMAT(10X,'SINE VALUE=',F8.3,10X,'DAC VALUE=',I5)
80      CONTINUE
C
C CALL THE DAC SUBROUTINE FOR CONVERSIONS AND DISPLAY
C
90      DO 110 J=1,LIMIT
        CALL DAC(Z(J),0)
C
C DELAY ROUTINE TO TAKE CARE OF THE TIME BETWEEN SAMPLES
C AND HENCE THE FREQUENCY.
C
        DO 100 K=1,ITIME
100     CONTINUE
110     CONTINUE
        GO TO 90
        STOP
        END
```

```
 RUN SINGEN
          ENTER SAMPLING TIME BETWEEN SAMPLES
10
          ENTER # OF DIVISIONS / CYCLE <=500
32
          ENTER THE AMPLITUDE SCALE : 0<SCALE<=1
1.0
          SINE VALUE=    0.000          DAC VALUE= 2047
          SINE VALUE=    0.195          DAC VALUE= 2446
          SINE VALUE=    0.383          DAC VALUE= 2831
          SINE VALUE=    0.556          DAC VALUE= 3185
          SINE VALUE=    0.707          DAC VALUE= 3495
          SINE VALUE=    0.831          DAC VALUE= 3749
          SINE VALUE=    0.924          DAC VALUE= 3939
          SINE VALUE=    0.981          DAC VALUE= 4055
          SINE VALUE=    1.000          DAC VALUE= 4095
          SINE VALUE=    0.981          DAC VALUE= 4055
          SINE VALUE=    0.924          DAC VALUE= 3939
          SINE VALUE=    0.831          DAC VALUE= 3749
          SINE VALUE=    0.707          DAC VALUE= 3495
          SINE VALUE=    0.556          DAC VALUE= 3185
          SINE VALUE=    0.383          DAC VALUE= 2831
          SINE VALUE=    0.195          DAC VALUE= 2446
          SINE VALUE=    0.000          DAC VALUE= 2047
          SINE VALUE=   -0.195          DAC VALUE= 1648
          SINE VALUE=   -0.383          DAC VALUE= 1263
          SINE VALUE=   -0.556          DAC VALUE=  909
          SINE VALUE=   -0.707          DAC VALUE=  599
          SINE VALUE=   -0.831          DAC VALUE=  345
          SINE VALUE=   -0.924          DAC VALUE=  155
          SINE VALUE=   -0.981          DAC VALUE=   39
          SINE VALUE=   -1.000          DAC VALUE=    0
          SINE VALUE=   -0.981          DAC VALUE=   39
          SINE VALUE=   -0.924          DAC VALUE=  155
          SINE VALUE=   -0.831          DAC VALUE=  345
          SINE VALUE=   -0.707          DAC VALUE=  599
          SINE VALUE=   -0.556          DAC VALUE=  909
          SINE VALUE=   -0.383          DAC VALUE= 1263
^C        SINE VALUE=   -0.195          DAC VALUE= 1648
^C

.
```

SIMPLE LOW COST TECHNIQUES FOR FREQUENCY SYNTHESIS

by

KRISHNA CHANDRA SHEKAR

B.E., Bangalore University (India), 1976

AN ABSTRACT OF A MASTER'S REPORT

Submitted in partial fulfillment of the
requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY

Manhattan, Kansas

1984

ABSTRACT

Studies were made of three different low cost techniques for frequency synthesis and comparisons were made between them. The first method is a radio frequency technique where two frequencies are mixed and the required output filtered out. In the second method two lower frequencies are run through an analog multiplier and the output frequency again filtered out. The third method is a digital technique where the stored waveform amplitude values are output via a digital to analog converter at different rates to give the required range of frequencies.

For the first two methods the circuits were built and experimentally analysed and tested. The third method of analysis was simulated on the PDP-11/03 computer system, and a software program written to generate and display a variable frequency sine wave on an oscilloscope. All three methods involve low cost components and are quite simple to build.

The three methods have been compared and the third method of digital frequency synthesis is the one that is recommended for use in the instrumentation laboratory.