A NONLINEAR TRANSISTOR MODEL AND DEVICE CHARACTERIZATION

by

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1. INTRODUCTION

As the requirements for computer circuit performance becomes more demanding, there is an ever increasing need for a more efficient method of describing transistor circuits. Before this need can be met, a transistor model must be available which will permit accurate prediction.

There are numerous models available which (3) permit accurate prediction. Many parameters associated with these models are not easily evaluated, and the evaluations often require facilities and measurement techniques which are not commonly available. These models cannot be easily simulated on the computer; such a simulation often requires advanced type computer, and program execution times are lengthy. In short, these models are cumbersome to use in practice. There is need for a model which is based on theoretical principles but which can be easily used in practice. Such a model 1) should be a good compromise between accuracy and tractibility, 2) should have the property of ease of evaluation of its parameters with conventional facilities and reasonable precision, 3) should permit simulation on the computer easily with a reasonable execution time, 4) should be valid for large as

well as small imput signals. Large signal input can be as large as to derive the transistor into saturation, but should not be so large to cause high injection effects.

The model to be described in this report is not a complex model. In fact, it has been around for quite some time. However, with the addition of the nonlinear characteristics and with careful device characterization, this model can provide the necessary means of predicting response to large as well as small input signal.

The characteristics of the p-n junction have been studied by many authors (2). By concentrating study on only one junction, one can understand more readily some of the more important transistor characteristics. In developing this model, each junction of a common base transistor is studied, while the other terminal is shorted to base. The use of superposition is made in obtaining the model. Because the model is nonlinear, the use of superposition may at first be considered invalid. The model is to be simulated on the computer, and the computer obtains the solution to the differential equations by means of numerical integration. By choosing small enough intervals of integration, nonlinearity can be observed as linearity within each interval. The program re-evaluates the nonlinear elements for each given interval. Then using the system of

nonlinear differential equations describing the model, in conjunction with the internal subprograms, the value of the voltages corresponding to that interval are predicted and corrected. If the predicted value is not within specified allowable error from the corrected value, then the program modifies the interval of integration and repeats the cycle until the specified allowable error is met. Thus use of superposition is validated.

Most of the methods described in this report to evaluate the parameters of the model are standard methods; however, they are modified when necessary.

Although the model is tested with fast rise-time input pulses, the model has more general applications. The input pulse tests are more severe than simple a-c or d-c input tests. By fourier-series expansion it can be shown that the pulse has both a-c and d-c components.

2. EQUIVALENT CIRCUIT

The model being derived is based on the Ebers and Moll's equations for transistors (1), Equation (1) and (2). The direction of the currents and polarity of the voltage terminals are shown in Fig. (1).



Fig. 1. The direction of current and polarity of the voltage which corresponds to Equations (1) and (2).

Where:

I.	=	Emitter Current
IC	Ξ	Collector Current
VE	=	Emitter-to-Base Voltage
v_{c}^{-}	=	Collector-to-Base Voltage

$$I_{E} = a_{11} (e^{qV_{EB}/kT} - 1) - a_{12} (e^{qV_{CB}/kT} - 1)$$
(1)

$$I_{C} = a_{21} (e^{qV_{EB}/kT} - 1) - a_{22} (e^{qV_{CB}/kT} - 1)$$
(2)

Where:

q	Electron Charge													
k	Boltzmann's Constant													
г	Temperature													
a _{11'}	a ₂₂ ,	a ₂₁ ,	and	a ₁₂	are	Constants								

The constants a11, a12, a21 and a22 are functions of transistor material and junction temperature. The meanings given to these constants in this paper are different from the meanings that are given in the reference (1). This will be further discussed. Equations (1) and (2) are derived solely from the diffusion equation for the d-c condition. The assumptions made in deriving Equations (1) and (2) are: that drift current is negligible compared to diffusion current, and that there are no mobile charges in the depletion layers (7). The above assumptions are valid for the first derived model. The model obtained in this manner will be called the intrinsic model. The intrinsic model will be further completed by introducing some of the extrinsic elements. The extrensic elements considered are: depletion junction capacitance, bulk resistance, and header capacitances. The model resulted by introducing extrinsic elements into intrinsic model is called extrinsic model. The extrinsic model further be completed by introducing additional nonlinear elements to the model to account for base width modulation and other effects caused by forward baising collector junction, and this model will be called complete model.

The solution to Equation (1) and (2) for I_E and I_C are obtained by superposition. This is done 1) by setting the

voltage $V_{CB}^{=}$ 0 and obtaining the I_E and I_C only due to V_{EB} ; 2) by setting the voltage $V_{EB}^{=}$ 0 and obtaining the I_E and I_C only due to V_{CE} ; 3) the I_E and I_C that satisfies equations (1) and (2) are the summation of I_E 's obtained from condition (1) and (2) and summation of I_C 's obtained from condition (1) and (2).

The value of V_{CB} is set equal to zero by shorting the collector to base. The equations (1) and (2) are then reduced to equations (3) and (4) respectively.

$$I_{E1} = a_{11} (e^{qV_{EB}/kT} - 1)$$
(3)
$$I_{C1} = a_{21} (e^{qV_{EB}/kT} - 1)$$
(4)

Equation (3) is analogous to the voltage v.s. current characteristics of a p-n junction diode. The current-voltage characteristics of a p-n junction can be represented by equation (5).

$$I = I_{s} \left(e^{qV/kT} - 1 \right)$$
(5)

where:

Is back saturation current of a p-n junction.

I_s is function of cross sectional junction area, diffusion constant, diffusion length and dopping of acceptors and holes in p region and n region.

A close comparison between equations (3) and (5) yields that constant a_{11} is some sort of back saturation current of a p-n junction. So a_{11} will be defined as I_{SE} , the back saturation current of the emitter-to-base junction when the collector is shorted to base. By substituting I_{SE} in equation (3), equation (6) is obtained.

 $I_{E1} = I_{SE} (e^{qV_{EB}/kT} - 1)$ (6) By Kirchboff's current law:

$$I_{\rm E} = -(I_{\rm C} + I_{\rm B}) \tag{7}$$

By dividing equation (4) into equation (6) a_{21} is obtained, equation (8).

$$a_{21} = \frac{ICI}{I_{E1}} \cdot I_{SE}$$
(8)

$$A_1$$
 is defined as $\frac{I_{C1}}{I_{E1}} = A_1$ (9)

Further manipulation results equation (10).

$$I_{C1} = A_1 I_{SE} (e^{qVEB/kT} - 1)$$
 (10)
Or $I_{C1} = A_1 I_{E1}$

Equations (6) and (11) suggest that the below model can be derived, Fig. (2). The model Fig. (2) suggests that for understanding the behavior or the emitter junction, one can investigate the modified diode of Fig. (2). Hence, the characteristics of the diode will be investigated. The voltage vs. current characteristics of the diode p-n junction is shown in Fig. (3), and for an ideal diode, the functional relationship representing this V-I characteristic is given by equation (12).

The functional relationship describing the conductance of the junction due to the diffusion mechanism is defined in equation (13).

$$G_{\rm D} = \frac{I}{V} = \frac{I_{\rm S} \left(e - 1\right)}{V}$$
(13)

V is applied Voltage.



Fig. 2. Model representation of emitter junction when $V_{CB} = 0$.



Fig. 3. V-I Characteristic of Diode.

$$I = I_{S} (e^{V} - 1)$$
(12)
= q/kT



Fig. 4. M_{O} del representation of emitter junction with nonlinear elements, when $V_{CB} = 0$.

Where:

$$G_{DB} = \frac{I_{SE} (e^{V V EB} - 1)}{V_{EB}}$$
(15)

$$c_{\rm DB} = \gamma_{\rm b} \, \mathbf{I}_{\rm SE} e^{\mathbf{X} \mathbf{V}_{\rm EB}} \tag{16}$$

The functional relationship describing the diffusion capacitance of the junction is given by equation (14).

$$c_{\rm D} = \Upsilon_{\rm bdV} \stackrel{\rm dI}{=} \Upsilon_{\rm b} I_{\rm Se} {}^{\rm V} \tag{14}$$

 $\Upsilon_{\rm b}$ the effective minority lifetime in the base.

The model in Fig. (2) can be presented as shown in Fig. (4).

Now, by setting the value of $V_{\rm EB}$ equal to zero in equations (1) and (2), characteristics of the collector junction may be obtained which are similar to the emitter characteristics when $V_{\rm CB}$ = 0.

$$I_{E2} = -a_{12} (e^{\mu V_{CB}} - 1)$$
 (17)

$$I_{C2} = -a_{22} (e^{\mu V_{CB}} - 1)$$
(18)

$$\mu = q/kT$$

$$A_2$$
 is defined as $A_2 = \frac{I_{E2}}{I_{C2}}$ (19)

A close comparison between equations (5) and (18) yields that constant a_{22} is some sort of back saturation current of a p-n junction. Then a_{22} will be defined as I_{SC} , the back saturation current of the collector to base junction when the emitter is shorted to the base. By substituting

 I_{SC} in equation (18), equation (20) is obtained.

$$I_{C2} = -I_{SC} (e^{\mu V CB} - 1)$$
 (20)

Further manipulations similar to the manipulation done for the emitter junction yield equations (21-22) for collector junction.

$$I_{C2} = -I_{SC} (e^{\mu V_{CB}} - 1)$$
(21)
$$I_{E2} = A_2 I_{C2}$$
(22)

The equations (21) and (22) suggest that model Fig. (5) can be derived. The model in Fig. (5) can be presented as shown in Fig. (6) by introducing nonlinear elements.

Now the solution to the equations (1) and (2) are:

$$I_{E} = I_{E1} + I_{E2}$$
 (23)

 $I_{C} = I_{C1} + I_{C2}$ (24)



Fig. 5. Model representation of collector junction when $V^{}_{\rm EB}$ = 0.



Fig. 6. Model representation of collector junction with nonlinear elements, when $V_{\rm EB}$ = 0.

Therefore:

$$I_{E} = I_{SE} (e^{\forall V_{EB}} - 1)$$
 (25)

$$I_{C} = A_{1}I_{E1} - I_{SC}(e^{\mu V_{CB}} - 1)$$
 (26)

Equations (25) and (26) suggest that model in Fig. (7) can be derived. The Model in Fig. (7) can be represented as in Fig. (8) by introducing nonlinear elements.

An equivalent circuit for the common emitter configuration of the equivalent circuit of Fig. (8) will be obtained. The first step is to redraw the circuit of Fig. (8) into a "T" equivalent circuit as shown in Fig. (9). Further manipulations of Fig. (9) suggest the below equations.

$$I_{B} = I_{E1} + A_{2}I_{C2} - A_{1}I_{E1} - I_{C2}$$
 (35)

Or
$$I_B = -I_{E1}(1 + A_1) - I_{C2}(1 + A_2)$$
 (36)

And
$$I_{C} = A_{1}I_{E1} + I_{C2}$$
 (37)

Or
$$I_{C} = I_{C2}(1 - A_2) + I_{C2}A_2 + A_1I_{E1}$$
 (38)

Equations (36) and (37) suggest Fig. (10).

 A_1 and A_2 can be related to hFE and hFEI respectively. This is done as follows. The transistor is operated inversely and $V_{\rm EB}$ is set equal to zero.



Fig. 7. Model representation of a common base transistor.

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$$I_{E1} = I_{SE} (e^{\forall V_{EB}} - 1)$$
(27)

$$I_{C2} = -I_{SC} (e^{\mu V_{CB}} - 1)$$
 (28)

$$I_{E2} = A_2 I_{C2} \tag{29}$$

$$I_{Cl} = A_l I_{El} \tag{30}$$



Fig. 8. Intrinsic Model representation of a Common base configuration of transistor with nonlinear elements.

Where: $G_{DB} = \frac{I_{SE}(e^{\delta V_{EB}} - 1)}{V_{EB}}$ $C_{DB} = \gamma'_{b} I_{SE}e^{\delta V_{EB}}$ $\delta = q/kT$ $G_{SB} = \frac{I_{SC}(e^{\mu V_{CB}} - 1)}{V_{CB}}$ $C_{SB} = \gamma'_{b}hFE I_{SC}e^{\mu V_{CB}}$ $\mu = q/kT$

hFE - short-circuit current gain for common-emitter mode of transistor operation.



Fig. 9. "T" Equivalent Circuit of Fig. 8.



Fig. 10. Intrinsic Common Emitter Equivalent Circuit of Transistor.

$$I_{E1} = I_{SE} (e^{-VV_{BE}} - 1)$$
 (39)

$$I_{C2} = -I_{SC} \left(e^{\beta (V_{CE} - V_{BE})} - 1 \right)$$
(40)

The parameter hFEI is defined as short-circuit common-emitter current gain for a transistor operated inversely.

$$\frac{I_{\rm E}}{I_{\rm B}} = \rm hFEI$$
 (41)

$$A_2 = \frac{I_E}{I_C}$$
(42)

$$Or \quad A_2 = \frac{I_E}{I_E + I_B}$$
(43)

Or
$$A_2 = -\frac{1}{1+I_B} = -\frac{hFEI}{1+hFEI}$$
 (44)

Now $V_{\rm CE}$ is set equal to zero, therefore:

$$\frac{I_{C}}{I_{B}} = \frac{A_{1}}{1 - A_{1}} = hFE$$
(45)

$$Or \quad A_1 = \frac{hFE}{1 + hFE}$$
(46)

The Intrinsic Model representation of a common-emitter configuration of transistor with nonlinear elements is shown in Fig. (11).

The model in Fig. (11) is based on the diffusion mechanism only, and is called an intrinsic model. This model can be further completed by introducing extrinsic elements in the model which are: junction depletion capacitance, bulk resistances, and header capacitance. Although the extrinsic elements are not derived from diffusion equation, they may be dependent on the junction current or junction voltage. This will be discussed.



Fig. 11. Intrinsic Model for a Common-Emitter Configuration.

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Where:

$$G_{D} = \frac{I_{SE}(e^{-\delta V_{BE}} - 1)}{(hFE + 1)V_{BE}}$$

$$G_{S} = \frac{I_{SC}(e^{-\beta (V_{BE} - V_{CE})} - 1)}{(hFEI + 1)(V_{CE} - V_{BE})}$$

$$C_{D} = \frac{\gamma_{h}I_{SE}e^{-\delta V_{BE}}}{(hFE + 1)}$$

$$C_{S} = \frac{\gamma_{h}hFE}{(hFEI + 1)}$$

$$C_{S} = \frac{\gamma_{h}hFE}{(hFEI + 1)}$$

$$I_{1} = hFE V_{BE}G_{D}$$

$$I_{2} = hFEI G_{S}(V_{BE} - V_{CE})$$

The variation of the depletion layer capacitance of the diode p-n junction as a function of the applied voltage depends on the nature of the charge distributed on the junction. This capacitance for the abrupt charge density distribution is in the form of equation (47).

$$C_{J} = \frac{C_{1}}{(V\phi - V)^{\frac{1}{2}}}$$
(47)

Where: C_1 is a constant function of the dopping level, area of the junction and permittivity of the junction. V_{ϕ} is the built-in depletion layer voltage which is a function of semi-conductor material. V is the externally applied voltage across the junction.

The depletion layer capacitances for the linearly graded charge density is in the form of equation (48).

$$c_{\rm J} = \frac{c_{\rm l}}{(V \phi - V) \, 1/3} \tag{48}$$

The charge distributions used in the transistor junctions are usually either abrupt or linearly graded. However, they are not ideally abrupt or linearly graded, so that the value m is chosen instead of the powers 1/2 or 1/3 for $(V\phi - V)$.

Thus
$$C_J = \frac{C_1}{(V_{\phi} - V)^m}$$

It should be pointed out that the assumption was made that there are no mobile carriers in the depletion layer.

The bulk resistance of the emitter region or the collector region is obtained from the conductivity of the emitter region or the collector region respectively. However, these resistances are small enough to be ignored for all practical purposes. The bulk resistances of the base region is not only due to the conductivity of the base region, but also depends on the recombination of the carriers in the base region which is strongly dependent on the magnitude of emitter current. This phenomena is not well understood.

The header capacitances are due to the lead wires to transistor and the transistor encopsilation. These capacitances could affect the performance of the transistor at high speed application.

The model including the extrinsic parameter for the common emitter configuration is shown in Fig. (12).

The functional relationship representing the parameters of Fig. (8) for PNP and NPN transistor are on page of this report.





The parameters corresponding to Fig. (9) for PNP and NPN transistors are given below:

PNP

NPN

$$C_{E} = \frac{C_{E1}}{(V_{E} - V_{B'E})^{m}}$$
 $C_{E} = \frac{C_{E1}}{(V_{B'E} - V_{E})^{m}}$

$$c_{C} = \frac{c_{C1}}{(v_{CE} - (v_{CE} - v_{B'E}))^{n}} \qquad c_{C} = \frac{c_{C1}}{((v_{CE} - v_{B'E}) - v_{C})^{n}}$$

$$c_{\rm D} = \frac{\gamma_{\rm b} \ I_{\rm SE} \ e^{-\zeta V_{\rm B'E}}}{(h_{\rm FE} \ + \ 1)} \qquad \qquad c_{\rm D} = \frac{b \ I_{\rm SE} e^{\zeta V_{\rm B'E}}}{(h_{\rm FE} \ + \ 1)}$$

$$G_{D} = \frac{I_{SE}(e^{-V_{B}'E} - 1)}{(h_{FE} + 1)V_{B'E}} \qquad G_{D} = \frac{I_{SE}(e^{\delta V_{B}'E} - 1)}{(h_{FE} + 1)V_{B'E}}$$

$$c_{s} = \frac{\gamma_{b} \frac{I_{schFE}}{(h_{FEI} + 1)}}{(h_{FEI} + 1)} \qquad c_{s} = \frac{\gamma_{b} I_{schFE}}{(h_{FEI} + 1)} \frac{(e^{\mu(V_{CE} - V_{B'E})} - 1)}{(h_{FEI} + 1)}$$

$$G_{S} = \frac{I_{SC}(e^{-\mu(V_{CE}-V_{B'E})} - 1)}{(h_{FEI} + 1)(V_{B'E} - V_{CE})} \qquad G_{S} = \frac{I_{SC}(e^{\mu(V_{CE}-V_{B'E})} - 1)}{(h_{FEI} + 1)(V_{CE} - V_{B'E})}$$

0	Emitter innetion deplotion epopeitones
E	Emitter Junction depiction capacitance.
CEL	The value of C_E when $(V_E - V_{B+E}) = 1$.
m	The parameter related to the $C_{\rm E}$, evaluated emperically.
c _C ,	C_{C1} , n Collector parameters which are analogous to the C_{E} ,
	C _{El} , and m respectively.
CD	Emitter junction diffusion capacitance.
$r_{\rm b}$	The effective minority carrier lifetime in the base.
	It is a function of q/kT for emitter junction.
I _{SE}	Back saturation current for emitter junction.
h_{FE}	Short-circuit current gain for common-emitter mode, of
	normal transistor operation. Equation (45).
Vøe	The barrier potential of the emitter junction.
н, І	$S_{\rm C}, V_{{ m OC}}$ Collector parameters, which are analogous to the
	γ , I _{SE} , and V $_{m arsigma E}$, respectively.
hFEI	Short-circuit common-emitter current gain for a
	transistor operated inversely. Equation (41).

3. DEVICE CHARACTERIZATION

The techniques used to characterize the device will be discussed here. It will become apparent later from the sensitivity studies that not all device parameters discussed will need to be measured on each and every device (5). In practice nominal values will suffice for a given family of devices.

Because of the similarity in which the emitter and collector junctions are represented in the model it is sufficient to describe only the measurements performed on the emitter junction in detail. The few differences that exist in the measurement techniques for the collector are appropriately cited.

The parameter I_{SE} and å are determined with the emitter biased in the forward direction and the collector shorted to base. The emitter input is a ramp input. Although the value of q/kT is attached to the å in most device treatises, it is found experimentally that the å is equal to the $\frac{q}{akT}$ where \underline{a} is experimentally found. The existence of \underline{a} can be explained by the approximation used in evaluating G_D and C_D . Further manipulation of equation (5) reveals equation (50).

$$I_{E} = I_{SE} (e^{\delta V} - 1)$$
 (5)

$$Or \quad I_E = I_{SE} e^{\delta V} \qquad e^{\delta V} \gg 1 \tag{50}$$

And $\log_{10}I_E = \log_{10}I_{SE} + V(\delta \log_{10}e)$ (50)

The value of I_{SE} then, is obtained by plotting $\log_{10}I_E$ vs. V. The intersection of the extrapolated line with the $\log_{10}I_E$ axis is the value of log I_{SE} and the slope of the line is $\log_{10}e$. A plot of the V_{EB} vs. I_E is shown in Fig. 14. It is incorrect to use the terminal voltage V_{EB} for the value of V in equation (50), because the V in equation (50) is the intrinsic voltage applied across the junction. The value V in terms of V_{EB} is given in equation (51).

 $V = V_{BE} - I_E R_{SE}$ (51) Where R_{SE} is emitter bulk resistance.

The modified V-I characteristic is shown in Fig. (13). The graphical technique used to evaluate γ and I_{SE} for the transistor X is shown in Fig. (14). (See Appendix 1 for information on Transistor X).

The Barrier junction potential $V \not o$ can be evaluated by equation (52).



Fig. 13. The Diode V-I Characteristic.

Solid line is terminal voltage v.s. current. Dash line is corrected value of voltage v.s. current.



Fig. 14. Graphical technique to evaluate ${\rm I}_{\rm SE}$ and δ .

$$V \not = \frac{kT}{q} \ln \frac{NaNd}{Ni^2}$$
 (52)
Na = density of acceptor atoms.
Nd = density of donor atoms.
Ni = carrier density in an intrinsic semi-conductor

Equation (52) is very cumbersome to use in practice. Vø can be evaluated easily by approximation. The sensitivity study has revealed that the Vø is not a very sensitive parameter and a close approximation is accurate enough. A diode at high current can be approximated by a series circuit consisting of a battery equivalent to barrier potential, a resistance which is equivalent to the diffusion resistance of the diode, and an ideal diode. The extrapolation of the slope to the V-I characteristic will meet the V-axis approximately at Value Vø. The graphical evaluation of this barrier potential is shown in Fig. 13. The nominal value of .8 volts can be used for a silicon transistor (5).

 C_{E1} and m are obtained from capacity measurements on the emitter junction (collector open circuited). The capacitance remaining, after the contribution of the lands and header are removed, versus the true junction voltage is plotted on log-log paper. The junction voltage is the applied voltage less the contribution of the barrier potential. Fig. 15 is an example of how the values of C_{E1} and m are obtained.



Fig. 15. Graphical technique for obtaining the value ${\rm m}$ and ${\rm C}_{\rm El}.$

A computer program can be written to evaluate C_{El} , m and Vø simultaneously. This can be done by sequential least square fit, which will find those values of C_{El} , m and Vø to fit experimental data and equation (49).

Short circuit common emitter current gain is measured in the conventional manner. Fig. 16 is an example of the dependency of this parameter on emitter current.

The value of $\boldsymbol{\gamma}_{\mathrm{b}}$ may be obtained by

$$\Upsilon_{\rm b} = \frac{1.22}{(1-\alpha_{\rm N}) \ \omega_{\rm N}} \tag{53}$$

Where α_N is low frequency of short circuit current gain for common base circuit. Where W_N α cut off frequency for the common base short-circuit current gain for a normally operated transistor.

In practice it is cumbersome to use equation (53) for evaluation of $\mathcal{T}'_{\rm b}$. The charge method technique is more widely used for evaluation $\mathcal{T}'_{\rm b}$, which is:

$$\gamma'_{\rm b} = \frac{\Delta Q_{\rm B}}{\Delta I_{\rm B}} \tag{54}$$



Fig. 16. Common emitter, short circuit current gain versus emitter current.

By manipulating equations (55) and (54), equation (56) will result.

$$\mathcal{T}_{C} = \mathcal{T}_{B} \cdot hFE$$
 (56)

Commonly $\widetilde{\gamma}_{c}$ is found first and then $\widetilde{\gamma}_{B}$ is calculated. This is done because the error involved in evaluating $\widetilde{\gamma}_{c}$ is less than the error in evaluating $\widetilde{\gamma}_{B}$.

Base spreading resistance, R_B can be obtained from a small-signal bridge measurement of the $R_B \cdot C_C$ product, Fig. 17.

The values of R_B indicate that R_B is a function of the emitter current and decreases as the emitter current increases; however, these values level off at higher emitter current. For the transistor X, a nominal value of 15 ohms is obtained for the emitter current beyond 3ma. For emitter currents less than 3ma, R_B increases to about twice the nominal value at 1ma.

 I_{SC} , μ , C_{C1} , n and hFEI are determined in the same manner as I_{SE} , λ , C_{E1} , and m and hFE respectively, with the exception that the emitter and collector leads are interchanged.



Fig. 17. The diagram used to evaluate $R_{\rm B}^{}$.

 $\begin{array}{l} R \\ K \\ C_{K}^{K} \end{array} is Known Resistance. \\ C_{K} \\ is Known Capacitance. \\ D \\ is Detector. \end{array}$

And:

$$R_{\rm B} = \frac{R_{\rm k}C_{\rm k}}{C_{\rm C}}$$

4. SIMULATION ON THE COMPUTER

The model in Fig. 12 is programmed on IBM 7090. This program can be used on the IBM 709X series. The program is written in the FORTRAN II language. A brief discussion of the program is given below. (See Appendix B)

The time response of the circuit is found by forming node equations and solving for derivatives where there are reactive elements at the node. This yields a system of nonlinear differential equations. These equations are:

$$_{\rm B}v_{\rm B} - G_{\rm B}v_{\rm BP} + (C_{\rm BES} + C_{\rm CBS})v_{\rm B} - C_{\rm CBS}v_{\rm O} = 0$$
 (59)

$$-V_{B}G_{B} + (G_{B} + G_{D} + G_{S})V_{BP} - G_{S}V_{O} + (C_{E} + C_{D} + C_{C} + C_{S})$$

$$V_{EP} - (C_{C} + C_{S} + C_{CBS})\dot{V}_{O} = 0$$

$$-G_{S}V_{BP} + G_{S}V_{O} - C_{CBS}\dot{V}_{B} - (C_{C} + C_{S})\dot{V}_{BP} + (C_{CBS} + C_{C})$$

$$\dot{V}_{O} = -hFEV_{BP}G_{D} + hFEI G_{S}(V_{O} - V_{BP})$$
(61)

Where:

G

$$v_{\rm B} = v_{\rm BE} \qquad v_{\rm BP} = v_{\rm B} \mathbf{1}_{\rm E} \qquad v_{\rm O} = v_{\rm CE}$$
$$\dot{v}_{\rm B} = \frac{\mathrm{d} v_{\rm B}}{\mathrm{d} t} \qquad \dot{v}_{\rm O} = \frac{\mathrm{d}}{\mathrm{d} t} v_{\rm O}$$

Equations 59 - 61 are solved by a predictor-corrector numerical integration technique. Nonlinear elements are handled by computing their value at each interval of integration step. The

accuracy and running time of this program is highly dependent on the initial value of voltages, the integration interval, and the maximum allowable relative error for each integration interval. The value of 1.0E - 7 has yielded accurate results and is recommended for use. The interval at which the program prints also determines the minimum integration interval which in turn affects the accuracy of the solution. Accurate calculations of the initial condition of the voltages (V_B , V_{BP} , and V_O) will decrease running time and have a solutary effect on the computed response. The input signal to the transistor should not be programmed at the initial time T_O . This is to allow the transients introduced by inconsistent initial conditions to dissipate before applying the input signal.

The functional relationships describing the R_B and hFE as a function of the emitter current are of complex nature; also, these relationships are not very representative of the phenomenom occurring. The values of R_B and hFE as a function of the emitter current are given by the table of values to the computer. An error is introduced in this program to reduce the computing time. This is done by evaluating the present value of R_B and hFE through using the last value of I_E . This error is of no consequence, and the approximation is justifiable, because the variation of the R_B and hFE as a function of I_F for an integration interval is negligible.

5. MODEL TESTS

The model of Fig. 12 has been exercised in a single saturated inverter circuit, in an emitter follower circuit, and in a three stage d-c coupled amplifier (5). The saturated inverter circuit exhibits the behavior of the model under large signal application. The emitter follower circuit exhibits the behavior of the model under small signal application. The three stage amplifier exhibits behavior of the model under both small and large signal simultaneously. The results indicate that the model is capable of predicting in detail both the steady-state and transient response of the device.

In all three circuits the components were chosen so as not to obscure the device performance. Although planar silicon transistors (Fairchild 1312) were used in the experimental work, the model has more general application. The systems of simultaneous nonlinear differential equations resulting from these circuits have been programmed on the 7090 in conjunction with the described program in part 4 of this paper.

5.1 CIRCUIT CHARACTERIZATION

The circuits used for these studies were carefully constructed to minimize stray inductance and capacitance. The remaining stray capacitances present were measured in the absence of the transistor and added to respective header and land capacitances to form C_{CBS} , C_{EBS} , and C_{CES} . The remaining circuit elements were measured by entirely conventional means. The equivalent resistance of the pulse generator and its termination were added to the lumped resistor in the base lead to form R_G . A carefully calibrated sampling scope driving an X-Y plotter was used to measure the .7 nanosecond ramp input pulse and the output voltage. Shunt capacitance of the scope probes were taken into account where appropriate (5).

5.2 SATURATED INVERTER CIRCUIT

The saturated inverter of Fig. A was driven under the conditions of the resistance R_G with a value of 525 ohms, V_{int} was a pulse with the peak value of 2.5 volts, and the rise time of the .7 nanosecond. Fig. 18 programmed on the 7090 computer as is described. The system of nonlinear differential



Fig. 18. Nonlinear transistor model in saturating inverter circuit.

$$(G_{g} + G_{B}) - G_{B}V_{BP} + (C_{CBS} + C_{CES})\dot{v}_{B} - C_{CBS}\dot{v}_{0} = G_{g}V_{in}(t)$$
(62)
$$-G_{B}V_{B} + (G_{B} + G_{D} + G_{S})V_{BP} - G_{S}V_{0} + (C_{E} + C_{D} + C_{C} + C_{S})\dot{v}_{BP} - (C_{S} + C_{C} + C_{CBS})V_{0} = 0$$
(63)
$$-G_{S}V_{BP} + (G_{L} + G_{S})V_{0} - C_{CBS}\dot{v}_{B} - (C_{C} + C_{S})\dot{v}_{BP} + (C_{CBS} + C_{L} + C_{C} + C_{S})\dot{v}_{0} = -h_{FE}V_{BP}G_{D} + E_{CC}G_{L} + h_{FEI}G_{S}(V_{0} - V_{BP})$$
(64)

equations describing Fig. 18 are given in equations 62 - 64.

The input voltage to the computer was described as shown in Fig. 19 and the functional relationships representing Fig. 19 were given in equations 65 - 71.

$$v_{in} = v_K \qquad 0 \leq T < T_0 \qquad (65)$$

$$v_{in} = v_{K} + v_{R} (1 - e^{-\delta(T - T_{0})}) \qquad T_{0} \leq T < T_{R}$$
(66)

$$v_{in} = v_L \qquad T_R \leq T < T_F \qquad (67)$$

$$v_{in} = v_L + (1 - e^{-\alpha (T - T_F)}) v_F \quad T_F \leq T < T_Q \quad (68)$$

$$\delta = \frac{-\ln\left(\frac{\nabla_{R} - \nabla_{L}}{\nabla_{R} - \nabla_{K}}\right)}{T_{R} - T_{O}}$$

$$T \in T_{Q}$$

$$T \in T$$

$$\alpha = \frac{\ln\left(\frac{V_{\rm L} - V_{\rm F}}{V_{\rm K} - V_{\rm F}}\right)}{T_{\rm Q} - T_{\rm F}}$$
(71)

The comparison of experimental and predicted result for saturated inverter Fig. 18 is shown in Fig. 20. The experimental performance of the device agreed with the predicted values better than 10 percent for turn-on delay, turn-on, and turn-off. Only the prediction of storage time did not agree with experimental results. This will be further discussed in section 6 of this paper.



Fig. 19. This form of the input is simulated on the Computer.

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T -- 4 nanosecond/division

Fig. 20. Comparison of experimental and predicted results for saturated inverter.

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Solid line is experimental results.
Dotted line is predicted results.
V_{in} = 2.5 volts with .7 nanosecond rise time.
R_g = 525 ohms.
```

5.3 EMITTER-FOLLOWER CIRCUIT

The stability of the emitter-follower has been investigated by many authors. It has been pointed out that the input of a transistor in the emitter-follower configuration appears, under certain conditions, to be a capacitance shunted with negative resistance. Therefore, if the driving source to this device appears to be inductive, instability and oscillation are quite likely to occur. Fig. 21 presents an equivalent circuit for a simple emitter-follower. The device model is the same as that used in the saturated inverter circuit with the exception that G_s and C_s were set to zero. The deriving source contains the inductance L necessary for instability. This inductance L in practice is usually caused by lead wire inductance. Fig. 22 shows a comparison of theoretical and experimental results for a representative device (transistor X) and for a value of inductance. The device value used to obtain the emitter-follower results were precisely those used to obtain saturated inverter of Fig. 20. This result demonstrates that this model need not be restricted to large signal applications but is equally useful in representing the device in the "linear" region.



Fig. 21. Nonlinear transistor model in emitterfollower circuit.

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Fig. 22. Comparison of experimental and predicted results for emitter-follower.

L	=	160	nh	$R_q = 50 \text{ ohms.}$
RO	Ξ	250	ohms	$v_{in(t)} = 1$ volt

5.4 THREE STAGE D-C COUPLED AMPLIFIER CIRCUIT

The model was exercised further in a three stage d-c coupled amplifier of Fig. 23. The device model was the same as that used in the saturated inverter circuit. The circuit used for this study was carefully constructed to minimize stray inductance. Stray inductances due to the circuit-wire were found to be negligible. No inductance was programmed as it was done for emitter-follower. Fig. 24 shows a comparison of the theoretical and experimental results for a representative device (transistor X). The result indicates that the use of a nonlinear model makes it possible to obtain both the steady-state and transient solution simultaneously.

In the analysis, T_1 , T_2 and T_3 are represented by the nonlinear transistor model of Fig. 12.



Fig. 23. Three-stage D-C Coupled Amplifier.



Fig. 24. Comparison of predicted and experimental results for the circuit of Fig. 23.

V = 5 mV pulse, 500 sec. in duration.

6. MODIFICATION OF THE MODEL

The extrinsic model of Fig. 12 is capable of predicting the turn-on, turn-on delay, turn-off delay, and d-c characteristics of the transistor in detail. However, it fails to predict the turn-off (storage time) in detail. This suggests that the extrinsic model should be further completed. Fig. 25 is a plot of collector deplation capacitance versus junction voltage. The equation (49) is used to describe this phenomena. The result indicates that the equation (49) is only capable of the predicting of the depletion layer capacitance for reversed biased condition. This indicates that the functional relationship used to describe the deplation junction capacitance was inadequate and failed to predict forward biased characteristic. This failure used to be blamed on the 1) difficulty of reproducing the forward biased data characteristic of deplation capacitance, 2) the diffusion capacitance. A careful capacitance measurement with a-c signal as small as 20 microvolts has made it possible to reproduce the forward biased data. The diffusion capacitance values were calculated and they indicated that for emitter junction the calculated value of the diffusion capacitance were very close to the

observed values. However, for collector junction the diffusion capacitance was by order of magnitude smaller than observed value. As a result, a new functional relationship for describing deplation layer capacitance is being adopted. The new functional relationship is capable of predicting depletion layer capacitance for the forward biased condition as well as reversed biased condition within five percent of the measured value. The results are plotted in Fig. 25 and the functional relationship is given by equation (72).

$$C_{\rm C} = \frac{C_{\rm C1}}{(V_{\phi \rm C} - V_{\rm CB})^{\rm III}} + \frac{C_{\rm FC1}}{(V_{\phi \rm C} - V_{\rm CB})^{\rm P}}$$
(72)

Where C_{C1} , m, C_{FC1} and p are found empirically.

Although this new functional relationship is not in exact exponential form, it closely resembles the work done by C. T. Sah and will predict the same result at the limits. C. T. Sah attributes this effect to free carriers in the transistor region (8).

The new functional relationship makes it possible to predict storage time within a few percent. The results are plotted in Fig. 26. The extrinsic model is called complete model when substituting equation (72) for equation (49).



Fig. 25. Collector depletion layer capacitance v.s. voltage across the junction.



T -- 4 nanosecond/Division

Fig. 26. Comparison of predicted and experimental results for the circuit, Fig. 18.

Solid line = experimental results. Dotted line = predicted results.

7. SENSITIVITY OF PREDICTED RESULT TO DEVICE AND CIRCUIT PARAMETERS

Every measurement made is subject to a number of errors. In order to determine the influence of measurement errors on the predicted results, nominal values for each parameter were used in the inverter program (5). These results were compared to the results obtained when each nominal value was incremented independently by 5 percent. The sensitivity results indicate that C_C and the parameters that determine base current V_{in} , $R_G + R_B$, and were by far the most important parameters for this circuit. The circuit response is relatively insensitive to parameters such as hFE and \mathcal{T}_b . The results of the sensitivity study make it possible to determine which device parameters need only be specified nominally, thus reducing drastically the number of parameters to be measured.

The program from which these results were obtained has facilities for emitter current dependence of hFE and R_B . However, all the results presented assume constant values for hFE and R_B . The predicted result from nonlinear hFE and R_B agree to the third place with the linear results. If a circuit with a saturation current approaching ma for the transistor X had been chosen, it would be anticipated that results would be a great deal different.

8. CONCLUSION

The results shown in this paper demonstrate the feasibility of using a nonlinear, equivalent circuit model to represent a transistor in large signal, small signal and both large signal and small signal operation simultaneously. Although the range of devices and circuit conditions is quite limited in this study, it is significant to note that none of the devices strayed more than ten percent from their predicted behavior, and the majority of this is attributed to the great dependence the circuit has to $V_{in}(t)$.

The model does not require any advanced programming and machine running time is not lengthy. Machine running time for the results of saturated inverter circuit was forty seconds, including read and write tape.

The model does an excellent job in predicting transient time. The model is not a cumbersome model. It does not introduce any new circuit elements. It is compatible with the other circuit elements to which it is to be connected and it does not require a circuit designer to be accustomed to new circuit elements. The relationship to device physics is relatively clear, and the model is capable of providing device people with information about their products.

The linear form of the model has found wide acceptance in the design of small signal amplifiers. The introduction of nonlinear elements intensifies the value of this model for small signal design since it permits simultaneous a-c and d-c analysis.

Parameters of the model can be evaluated easily with conventional techniques. Circuit elements and device parameters may be optomized long before the devices are available. This approach is particularly useful in the design of integrated circuit where the trimming of a circuit is impractical. The model can be used as the basis of an integrated specification which would include large signal and small signal application.

The model and the paragram can be combined to a subroutine paragram. The subroutine can be used instead of transistor in the circuit, and the performance of the circuit can be predicted easily.

In short, this model is a practical model.

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APPENDIX A

Transistor X is a NPN planar silicon transistor manufactured by Fairchild and was designated type 2B8.

The breakdown voltage of either junction is about 9 volts. The hFE of the transistor is about 75, the detail hFE characteristic is given in Fig. 16 of this paper. Other characteristics of this transistor are given in the device characteristics of this paper.

Other types of transistors were used in the experimental work, which all have exhibited similar results as transistor X. However, all the data and results represented in this paper are of transistor X.

APPENDIX B

The listing of the program used to predict the theoretical value is given in this Appendix. The data and programming of this Appendix is a portion of a published paper by the International Business Machines Corporation which is a supplement to reference (X). The paper identification is as follows.

Identification

Nonlinear Transistor model for the prediction of circuit transient response

R. J. Wilfinger/P. Kiankhooy-Fard/S. C. Plumb

Program Description - A. Selby, Scientific Computation, International Business Machines Corporation, Components Division, Fishkill, New York

```
С
                           CF ADDITION
     TRANSIST V
С
C
C
      VERSION WITH HYPERBOLIC FORM OF CF
     DIMENSION A(80), AIR(50), AIH(50), RB(50), HFE(50), V(4), VP(4),
     $ VC(4), TBL(16)
      EQUIVALENCE (V(1), VBP), (V(2), VO), (V(3), VB), (VP(1), DVBP),
     $ (VP(2), DVO), (VP(3), DVB), (V(4), VG), (DVG, VP(4))
      READ INPUT TAPE 20 50 A
 5
      FORMAT (20A4)
      READ INPUT TAPE 2, 2, IVSN, ERR
 1
      FORMAT (15, 5%, E5.0)
 2
      READ INPUT TAPE 2, 3, VG,VB,VB,VO,DT,TMAX
      READ INPUT TAPE 2, 3, VK, VL, VR, TO, TR
      READ INPUT TAPE 2, 3, VF, TF, TQ
      READ INPUT TAPE 2, 3, RG, CBES, CCBS, RL, CL, ECC
      READ INPUT TAPE 20 30 CCESOR2OC2OR3OROC
      READ INPUT TAPE 2. 3. AISE, GAM, Q. P. TB, VPHI
      READ INPUT TAPE 2, 3, CE1, EM, CC1, EN, AA, BB
      READ INPUT TAPE 20 30AISC 0 AMU 0 VPHC0. TS0 HFEI 0HFX
 3
      FORMAT (6E12.4)
      READ INPUT TAPE 2, 4, N, (AIH(I), HFE(I), I = 1,N)
      READ INPUT TAPE 20 40 Mo (AIR(I) + RB(I) + I = 10M)
      FORMAT (15/ (2E12.4))
 4
      CALL GIRL
      CALL TITLE
      WRITE OUTPUT TAPE 3, 6, A(1), VB, A(2), VBP, A(3), VO, A(4), DT,
     SA(5), TMAX
      WRITE OUTPUT TAPE 3, 6, A(6), VK, A(7), VL, A(8), VR, A(9), TO, A(
     $10), TR
     WRITE OUTPUT TAPE 3, 6, A(11), VF, A(12), TF, A(13), TQ, A(55), CCES
     WRITE OUTPUT TAPE 3, 6, A(14), RG, A(15), CBES, A(16), CCBS, A(17)
     $, RL, A(18), CL, A(19), ECC
     WRITE OUTPUT TAPE 3, 6, A(20), AISE, A(21), GAM, A(22), Q, A(23),
     $ P, A(24), AISC, A(25), AMU
     WRITE OUTPUT TAPE 3, 6, A(26), VPHI, A(27), CE1, A(28), EM, A(29),
     S CC1, A(30), EN, A(31), HFEI
     WRITE OUTPUT TAPE 3, 6, A(53), VG, A(56), R, A(57), C, A(58), R2,
     $ A(59), C2, A(60), R3
      GG = 1.7RG
      GL = 1./RL
      G = 1 \circ / R
     G_2 = 1.0/R_2
      G3 = 1.0/R3
      ALPHA = LOGF((VL - VF)/(VK - VF))/(TQ - TF)
      DELTA = -LOGF((VR - VL)/(VR - VK))/(TR - TO)
     WRITE OUTPUT TAPE 3, 6, A(32), TS, A(33), TB, A(51), ALPHA, A(52),
     $ DELTA, A(61), AA, A(62), BB
      WRITE OUTPUT TAPE 3, 6, A(64), VPHC
      FORMAT (1X, 6(A4, E12.5, 4X))
 6
      T = 0.
      TC =0.
      I = 0
      NN = 4
```

59 20 . 1 . 05 C. . / . V. . 22 20 20 0 20 6. 0 100 13 (- The A . . . 2 -The and the state of the state JU TO . CU . C. C. T. T. - V. Le si march Ĵ . VI. 1 . . . VILLE VE + JUL - JULE PE LEADERAN (I - TEX) 1F (T) 1-C. - T. 15 20 ATT = LIMACHES A D' PROB + (NO - ECC)AGE + DVORCE + GGR(VB - VIN) :_) 1. ALE - ATEIS, . . . 120,250 . 20 4=X = HEET. 30 10 150 07 140 1 = 290 18 0 18 - 2180 17 12 4150 140 - , 0 CONTRACE HEA = HEEIA) 30 10 160 -REX = NFE(I→1) + NALE → AIN(I+1)//(AIN(I) → AIR(I+1))*(HFE(I) → 150 3 HFENIML, J 100 10 10 165 :00 171 Rh. . KP't 10 10 210 10 DC 197 : = 2... 17 (ALE - ALRII,, 2.0 200.100 CRETINUE R X = RB ND 60 70 210 |<=>X == R6(|−1) = (AIE = AIR(I−1))/(AIR(I) = AIR(I−1))*(R6(I) = R6(I 5 - 111 X = EIPELCAREVSP, 2.0 Y = EXPERTURNING - VOID 210 OD HILISEW AHID / (THEXHID) #V8P; COMITE GAM (SEAN, / (HEX-1.)) I = CEI/ VPAI - VBP, ALEA CC = CC1/IVO - VBP + VPHC)**EN 35-1 A:SC*(Y-1)) /, HEE:+ 101*(VBP.-VO)) CS= ITS MANU AISC Y)/(HEEI WIW) WCF CA = 1. RAX (A = (NR - VOP) GE + VR*C2 + (VS - VIN *GG 18 - VARAGO + GD - GS, - V3*GB - V0*CS X. = VO*(GL + US) - VEP*GS + HEX*VBP*GD - ECC*GL - HEEI*GS*(VBP -XD = CRES + CCRG + CC 1. E CCB ... CONCERNENT CONCERNES = CC + CSX. = CCR3 + CL + CC + C + CC 3 >>> = ―(こうぶ(スケー・(ら (I/XG) ☆ > ◇>E)/(― E+ 2 + XD*(―XI**2/XG ☆ XJ))

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						1		1	· ·			t (* 1				
10	10	10 10	10	10 10	10	10	10	10	10	10	10	10	10 10	01 02	01 02	01 02
0.25000E 0.52911E	0.25000E 0.55272E	0.25000E 0.57961E	0.25000E 0.61106E	0.25000E 0.65905E	0.25000E 0.59640E	0.25000E 0.75475E	0.25000E 0.81692E	0.25000E 0.86846E	0.25000E 0.90655E	0.25000E 0.93515E	0.25000E 0.95342E	0.25000E 0.97851E	0.25000E 0.9969 5E	0.25000E 0.10143E	0.25000E 0.10309E	0.25000E 0.10471E
ζä∧ Cα	VI N CE	VIN CE	VI N CE	VIN CE	VIN CE	VIN CE	VIN CE	AI N CE	VI N CE	VI N CE	VIN CE	VIN CE	VI N CE	VI N CE	VI N CE	VIN CE
C.42496E-00 0.85477E-06	0.38741E-00 0.16325E-04	0.35512E-00 0.24148E-03	0.32674E-00 0.28618E-02	0.30278E-00 0.27725 <u>5</u> -01	0.27153E-00 0.21826E-00	0.21832E-00 0.12759E 01	0.13674E-00 0.45792E 01	0.75098E-01 0.97222E 01	0.47951E-01 0.14974E 02	0.30079E-01 0.19633E 02	0.27300E-01 0.23803E 02	0.19239E-01 0.27528E 02	0.19988E-01 0.31282E 02	0.28337E-01 0.34830E 02	0.15563E-01 0.38279E 02	0.20984E-01 0.41693E 02
0 48	0.00	DV8 00	010	0.0000000000000000000000000000000000000	0 V 8 C 0	0 V 8 C 0	0.00000	0 V 8 3 0	0 V B C D	0.0000000000000000000000000000000000000	0 V 8 C 0	0 V 8 C 0	000000000000000000000000000000000000000	0 V 8 C D	0.0000000000000000000000000000000000000	0 V 8 C 0
V8 0.31483E-00 GS 0.32610E-07 CF 0.82064E-04	VB 0.39597E-00 GS 0.33560E-07 CF 0.90796E-04	v8 0.47015E-00 GS 0.34550E-07 CF 0.10052E-03	V8 0.53826E 00 GS 0.35574E-07 CF 0.11123E-03	V8 0.60087E 00 GS 0.36622E-07 CF 0.12292E-03	V8 0.65784E 00 GS 0.37687E-07 CF 0.13556E-03	V8 0.70691E 00 GS 0.38776E-07 CF 0.14929E-03	VB 0.74241E 00 GS 0.39978E-07 CF 0.16540E-03	V8 0.76293E 00 GS 0.41514E-07 CF 0.18748E-03	VB 0.77428E 00 GS 0.43530E-07 CF 0.21903E-03	V8 0.78130E 00 GS 0.46043E-07 CF 0.26254E-03	V8 0.78637E 00 GS 0.49046E-07 CF 0.32066E-03	V8 0.79037E 00 GS 0.52562E-07 CF 0.39728E-03	V8 0.79379E 00 GS 0.56654E-07 CF 0.49808E-03	V8 0.79685E 00 GS 0.61430E-07 CF 0.63133E-03	V8 0.79944E 00 GS 0.67043E-07 CF 0.80887E-03	V8 0.80190E 00 GS 0.73724E-07
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A NONLINEAR TRANSISTOR MODEL AND DEVICE CHARACTERIZATION

by

PARVIZ KIANKHOOY-FARD

B. S., Missouri University, 1963

AN ABSTRACT OF A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

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An approach to transistor transient and steady state prediction for large signal, small signal, and both large signal and small signal simultaneously is described which uses a nonlinear equivalent circuit model. The model is based on the Eber and Moll's equations (intrinsic model). The model is modified by introducing extrinsic elements. The model is further completed by further investigation of collector junction under forward biased condition. A comparison of experimental and predicted results are presented for a saturated inverter circuit, an emitter-follower, and a three stage d-c coupled amplifier. The method of device characterization is outlined in detail. A sensitivity study is performed, and the relative sensitivity of the device parameter is pointed out. Theoretical results are obtained from numerics solution of a system of nonlinear differential equations describing the model and circuit diagram. The nature of the errors in the program are pointed out. The capability of the model to linear amplifier design is discussed and an integrated switching and linear amplifier specification is proposed. A subroutine program is proposed, which will enable the circuit designer to handle the transistor as one would have handled such circuit elements as the resistor, or the capacitor in a circuit without much knowledge about the material of the resistor or the capacitor.