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FERRITE CORE MEMORY DESIGN

by

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CHAPTER I

INTRODUCTION

A fundamental part of computers and as important part of most data processing systems is that portion which performs the function of storage. The terms "storage" and "memory" are synonymous, although the latter usually connotes high volume, long term storage.

Storage units may be divided into several classes, such as fast and slow, large and small, temporary and permanent, and volatile and nonvolatile, depending on the uses for which they are specified.

The main working memory, in which data is more or less temporarily stored and updated, usually consists of a high - speed array of thousands of ferrite cores or similar one-bit elements which can be almost instantaneously addressed for retrieval of data or insertion of new data. All of the data which might be required in the solution or processing of the problem at hand is normally placed in the main memory before the commencement of computation and recalled from the memory when needed during the steps of the computing process. (with exceptions, perhaps, for a process control or a computer which has data already stored in it by using Rom. Read only memory).

Data which must be held more permanently and recalled occasionally without the requirement for microsecond access is often stored on a magnetic drum or disc. This type of memory is always addressed, or interrogated, in the sequential mode; that is, every data location around the periphery is scanned in turn as the disc or drum rotates. If one

specific data location is to be read, the system must wait until that location comes under the read head. As a result of the restriction of sequential operation, access to a particular item on a disc or drum file typically requires several milliseconds,as compared with a few microseconds or less for a random access high speed memory.

Even more permanent forms of storage are used in applications where extremely large quantities of data can be filed and manually retrieved when needed. Commonly used long-term data storage are magnetic-tape, punched paper tape, and punched card files. Prior to the computation the data, in total or in groups of characters, is transfered from these permanent form of storage to a high speed memory unit in the data processor.

Once the data to be processed by a system has been transfered from permanent storage to a high-speed memory, a portion of the stored data is read from memory, as the problem requires, and delivered to a holding register which is a small, temporary storage unit. In the course of a problem, data words may be held in one of several registers, shifted through arithmetic or other logical processing blocks and finally either returned to the main memory or transferred to an output device.

Another distinction between classes of storage should be noted - volatility. An example of volatility is a storage device such as a flip-flop which requires uninterrupted supply of power and it loses its data if the power fails momentarily. All forms of the magnetic storage in a well designed system must retain their storage data reliably with or without power applied and are classified as nonvolatile.

Memory as a box

Memory can be treated as a complex box.

A memory has four major sets of terminals with which it may be connected to a computer, in addition to power supply connections.

These Four sets of terminals are,

1. Data in
2. Data out
3. Address input
4. Command-control input/output

According to Figure 1 the information to be stored is applied to the data input terminals. Bits of the data are in the form of logic " 0's " or " 1's ". A set of address inputs, called an address word, is applied to the address input terminals. This word tells the memory where to store the information. A write pulse or logic level is applied to a command terminal. The control logic then sequences the memory in the proper manner to write the information.

To read information which is known to be stored at a particular address (Refer to Figure 2), the address of the information is presented to the address input terminals. A read command pulse is applied to the appropriate command terminal and the desired information appears at the data output terminal after a short delay called the access time.

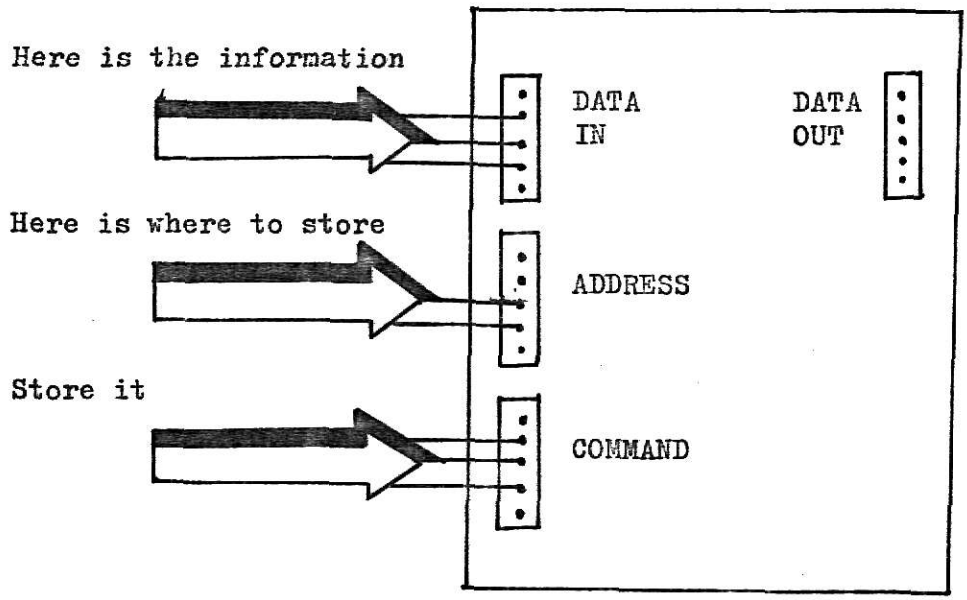


Figure 1. Data storage in a memory.

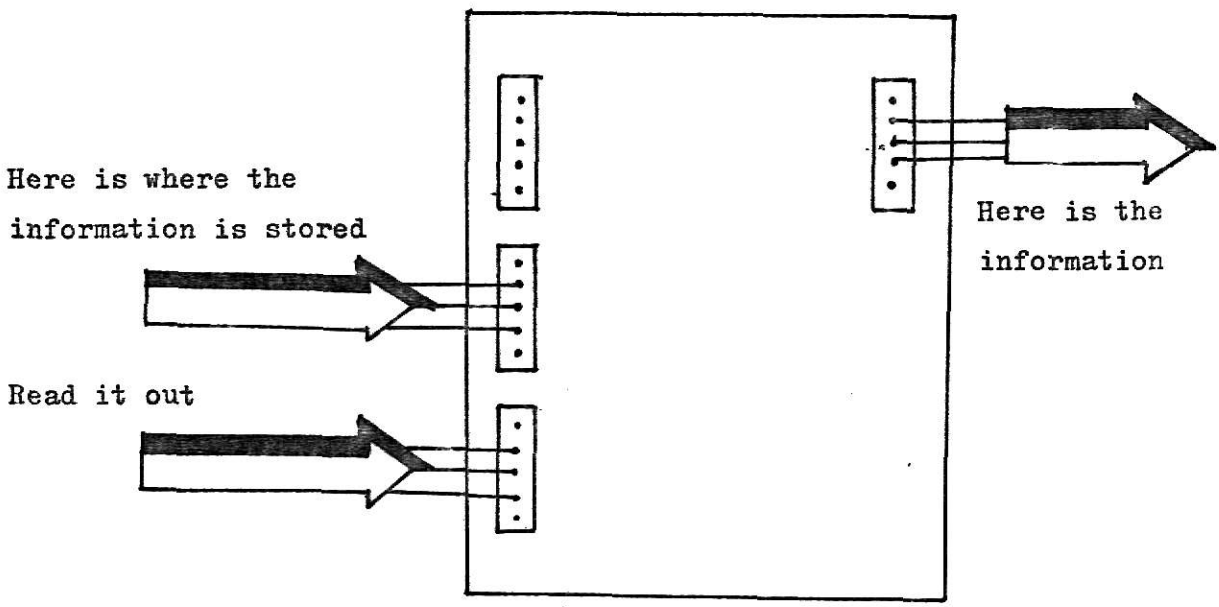


Figure 2. Data retrieval from a memory.

CHAPTER II

CHARACTERISTICS OF STORAGE MATERIAL

The most common type of high speed digital storage today is a ferrite core memory. Core memories can be built to provide millions of bits of storage with access times of less than a microsecond.

The basic storage element in a random access magnetic core memory is a toroidal or donut shaped ceramic magnet made from magnesium and manganese. The information stored in a ferrite core is represented by the direction of the magnetization in the core. If the magnetic flux is in one direction, the core is said to store a " 1 " and if in the reverse direction, a " 0 " (see Figure 3). To change the state from " 0 " to " 1 " or from " 1 " to " 0 " the direction of current must be changed.

Figure 4 shows the wiring of a core for the common three-dimensional four - wire memory. Four separate lines are threaded through the center of the core. These lines are designated X and Y for co-ordinate location, I for an inhibit line, and S for a sense line.

The magnetic characteristic (B-H curve) of the ferrite core is a nearly rectangular hysteresis loop (see Figure 5). If a current of + I amperes exists in the core winding for a sufficient time and then is removed, the core will retain a residual flux density + B. The existence of current -I for a sufficient amount of time will cause the core to retain a flux density -B (see Figure 6). When the core is arranged in the X - Y plane, a coincident of current both in X and Y lines is required to provide the full switching current $\pm I$; thus the X and Y lines

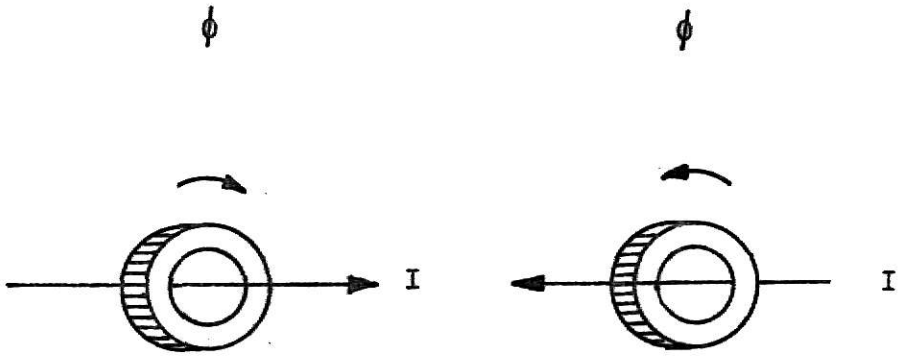


Figure 3. Magnetic flux ϕ with respect to current I in a core.

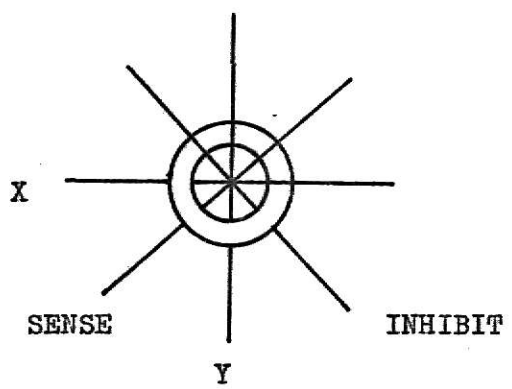


Figure 4. Core threading.

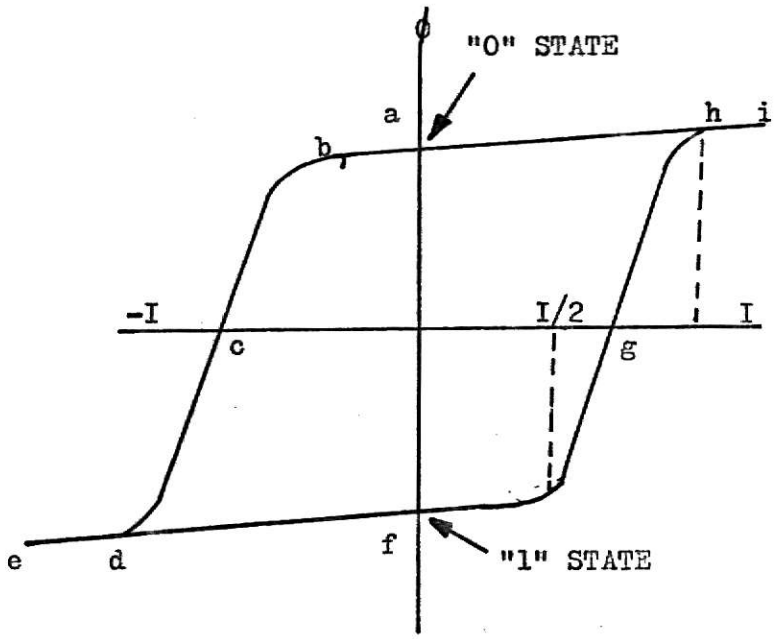


Figure 5. Magnetic flux ϕ versus current I for a typical ferrite core.

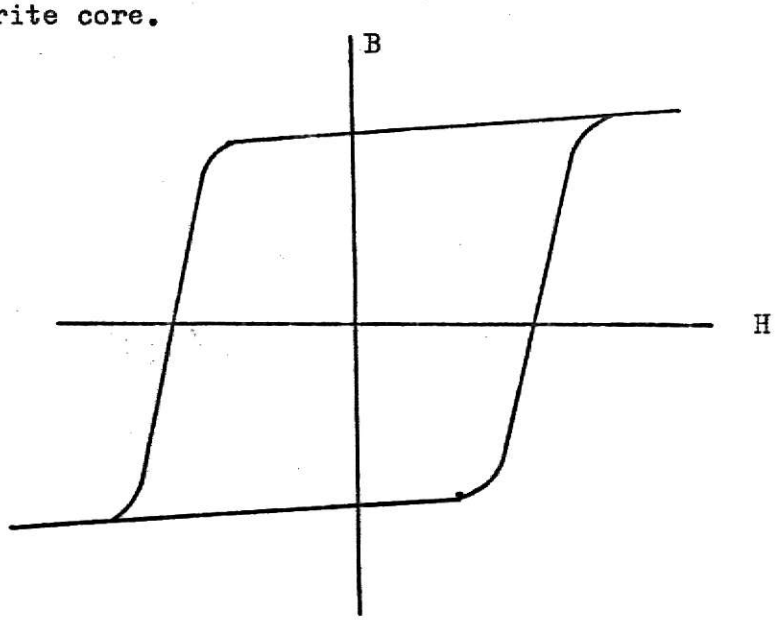


Figure 6. Magnetic flux density B versus magnetic field H for a typical ferrite core.

can each provide half of the total switching currents or $\pm I/2$.

During the write operation in the memory, negative or positive half currents are applied simultaneously to both X and Y windings for " 1 " or " 0 " states.

Assume that a " 0 " is stored in the core (stable state " a "). Applying only -I/2 current the operating point will move from " a " to " b ". If a negative drive current somewhat greater then -I is now applied to the winding, the operating point will move from " a " down through " c " and will stop at a point somewhere between point " d " and " e " on the -I curve (see Figure 5). When the -I/2 currents are removed from X and Y winding the operating point will move to " f " changing the core state from " 0 " to " 1 ". In a similar way positive -I/2 currents are required on X and Y windings to change a core from a " 1 " to " 0 " state.

During the READ operation of memory, positive currents I/2 are applied to both X and Y windings. If the core is storing a " 1 " at that instant, the read currents will change the state of the core from " 1 " to " 0 ", inducing across the sense wire a small voltage signal proportional to the rate of change of flux. If the core were previously in the " 0 " state, the read currents will have little effect on the core state and the relatively small flux change generates an even smaller voltage output (Figure 7). The read out is destructive; in both cases the core ends up storing a " 0 "; normally " 1'S " are immediately rewritten by the control logic.

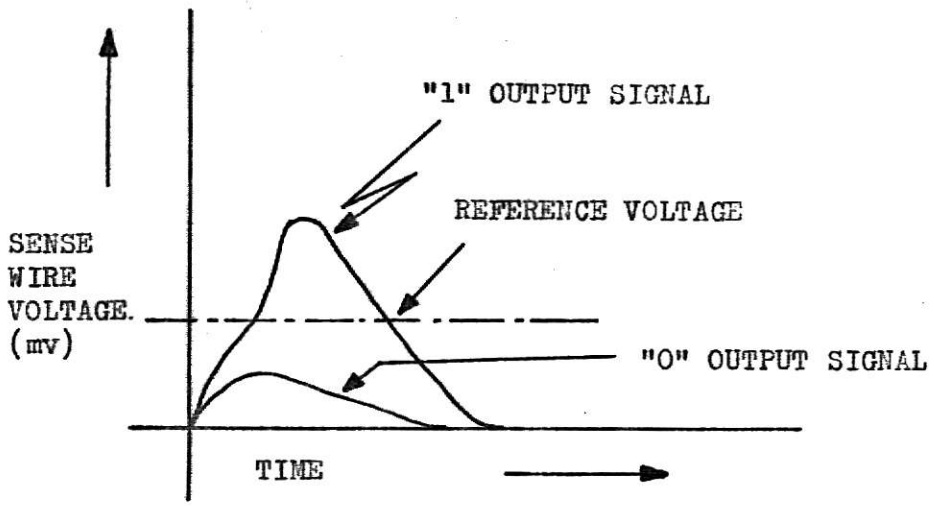


Figure 7. Sensing signal from core.

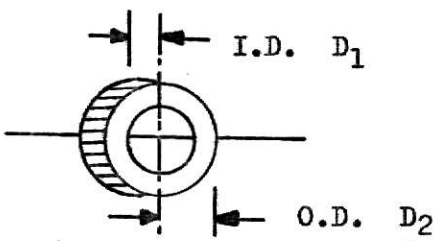


Figure 8. A typical ferrite core showing outer and inner diameter.

Core geometry & Switching time

Since even small cracks or chips will alter the properties of cores, the toroids must be complete and undamaged.

The switching time of the core is a function of intrinsic properties of the core and the applied current I. The applied current must remain on for a time duration equal to t_s.

$t_s = Sw/ (I-I_o)$

t_s = Switching time of core

s_w = Switching constant of core

I = Applied current (in milliampere)

I_o = Constant called the threshold current

The switching of core increases with increase of $I\Delta(I-I_o)$. Smaller diameter cores require somewhat less current for the same speed.

Switching current $\propto D_2$

D_2 = Outer diameter (Refer to Figure 8)

D_1 = Inner diameter

Current core sizes range from 80-90 mils down to 14-30 mils.

Temperature effects on Core

Cores are sensitive to temperature changes, operating normally at room temperature (60-80 F).

Increase in temperature causes the H dimension at the loop to become narrow, and flux density along B to increase (see Figure 9). As the H dimension becomes shorter cores may be switched by smaller currents.

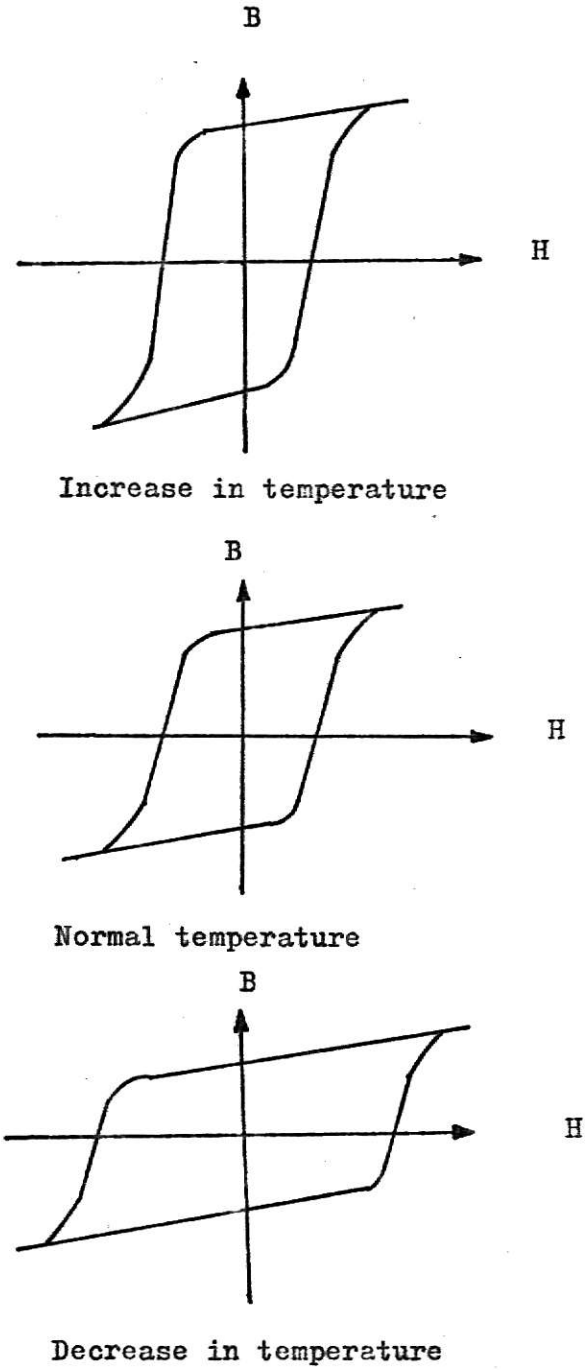


Figure 9. Temperature effect on B & H curve of a ferrite core.

Decrease in temperature decreases the flux density along B and widens the dimensions H along horizontal axis. In this case core requires a larger current to switch its state.

CHAPTER III

MEMORY ORGANIZATIONS

The basic magnetic core memory in most configurations stores a single bit of data in a single core element. There are as many core elements as there are binary bits to be stored. A single core stores a " 1 " or " 0 ". A single bit by itself is of little value. Hence, the next logical step is to consider how the individual bits are organized into a complete memory. Normally the bits are aligned in an array called a plane.

It is the read/write circuitry that determines the organization. All organizations trace back to two generic forms, bit organized and word organized.

3 D - Bit organized

The 3 D organized memory has a stack of bit-planes (arrays), each measuring X bits by Y bits. The number of planes in the memory equals the number of bits per word, or word length L. With this organization, the N^{th} plane contains the N^{th} bit of all words (thus the term bit organized). There are normally four wires through each core. This organization is popular because the number of switching circuits is the lowest of the three types of organization for storage ranging from 512 to 8192 words. Reading a bit is accomplished by the coincidence of two positive half current pulses on X and Y axes. Since sense and inhibit functions are only

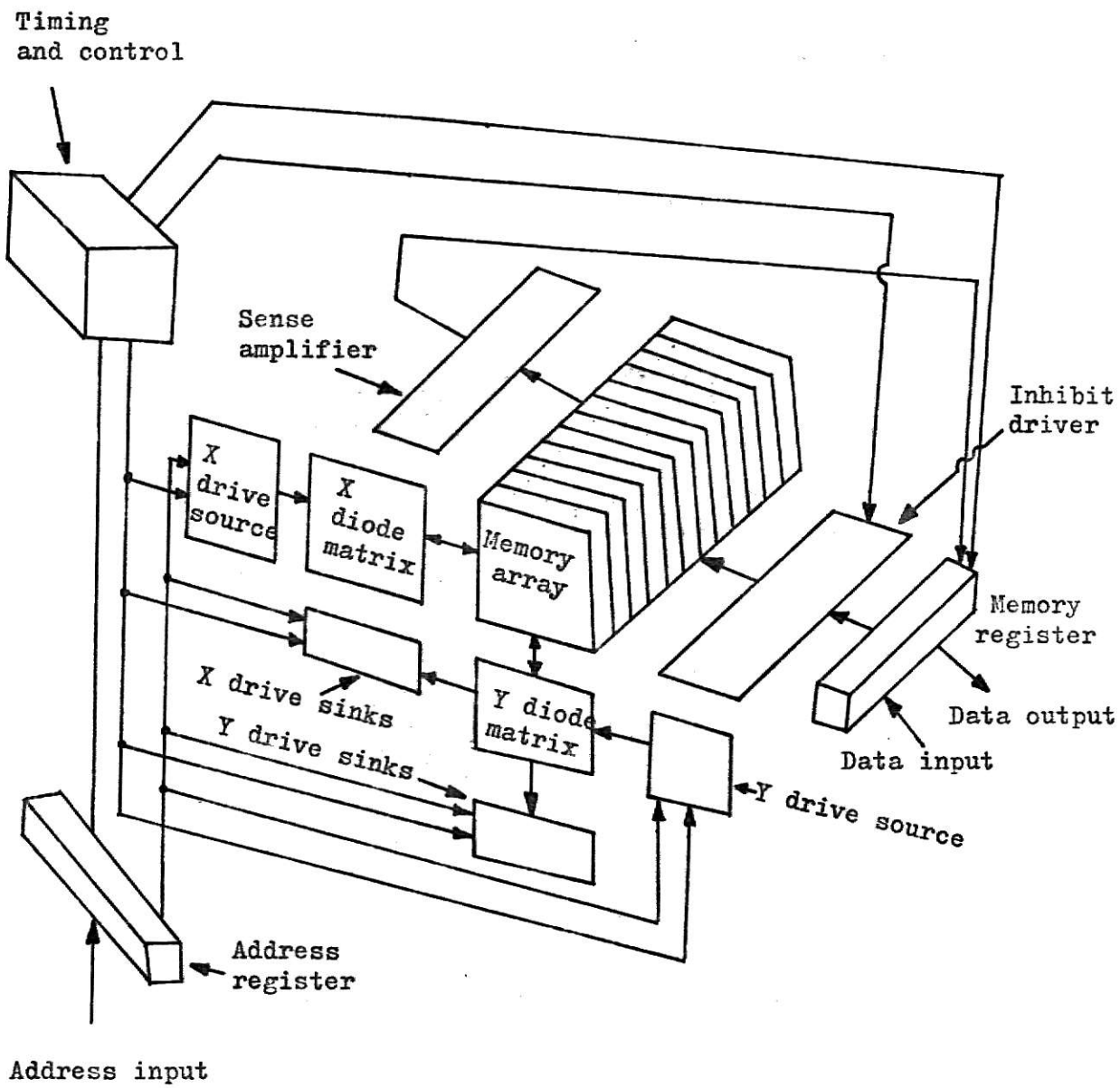


Figure 10. Organization of a typical 3 D core memory.

performed during read and write cycles, respectively, a 3 wire coincident current memory can be built by time sharing one wire. The operation of 3 D organization (Refer. Figure 10) is the same as shown in Figure 13.

2 D - Word organized

This organization was devised to meet the need for large, high-speed core memory systems. One memory line addresses all bit locations in one word (thus the term "word organized").

Only word current is used during read, and you can significantly overdrive the core to achieve extremely fast switching times. During read, a word-current pulse of sufficient amplitude to switch a core passes through all bits of a word. The bit lines are employed as sense lines and connected as inputs to sense amplifiers, one amplifier for each bit plane (L bits - L amplifiers).

Writing uses coincident-current. During write, the reduced word-current becomes insufficient to write " 1 ". Writing " 1 " demands simultaneous partial currents in the word and bit lines. Where " 0 " is required, inhibit is accomplished by omitting the bit current. The L bit lines are time shared. During read they act as sense lines.

The advantage of the word organize method (Refer. Figure 11) lies in the elimination of the inhibit driver of the 3 D organization which makes possible the use of only two wires through each bit element thus reducing core wiring costs.

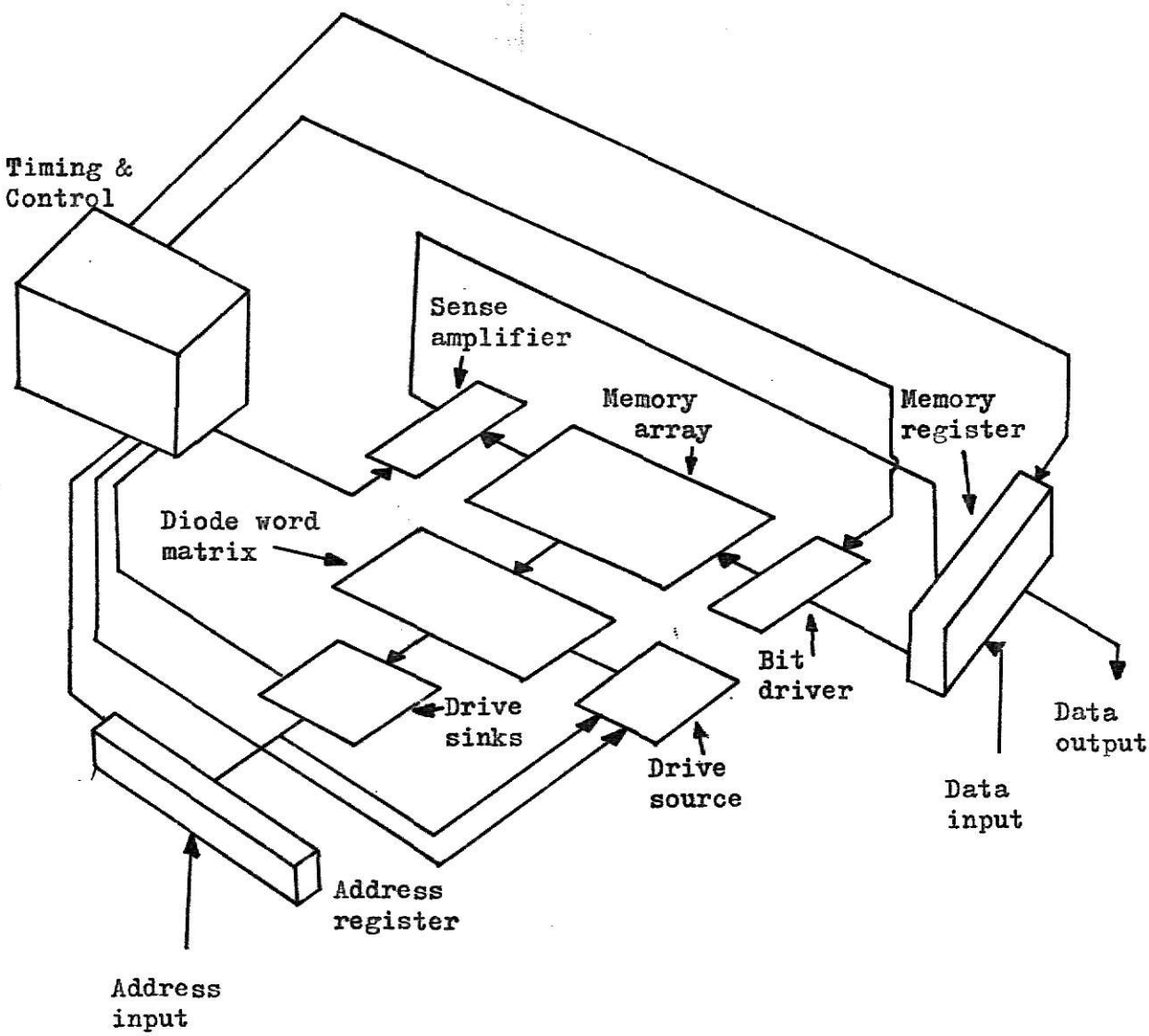


Figure 11. A 2D organization of a typical memory.

$2\frac{1}{2}$ D Organization

The designation of $2\frac{1}{2}$ D (See Figure 12) arises because this hybrid organization reads similarly to 3 D and writes similarily to 2 D. There are two types of hybrids depending on their speed and cost requirements.

In low cost, low speed hybrid organization output signals are superimposed on Y read current pulses and detected by special sense circuitry.

In the second type of hybrid organization there is a separate sense winding for each bit plane. The number of sense amplifiers is equal to the total number of Y bits.

For reading there are two coincident-currents, 2 I. One is in the X drive line, which is common to LY bits in a plane containing several words, including the desired one. The second current is in appropriate LY drive lines. A " 1 " is written by two coincident-currents, -2I. " 0's " are written by omitting the -I current in appropriate Y lines.

Coincident-Current Magnetic Core Memory Operation

The complete coincident-current memory system has many core arrays (planes) stacked on top of each other. Computers organization begins with the smallest element of information which is named a " bit " and is represented by a single core. Bits are grouped into words which can be of different bit length. The memory system in Figure 13 consists of 6 planes, each plane consisting of eight columns and eight rows of cores. Each core has column, row, and inhibit/sense windings threading through

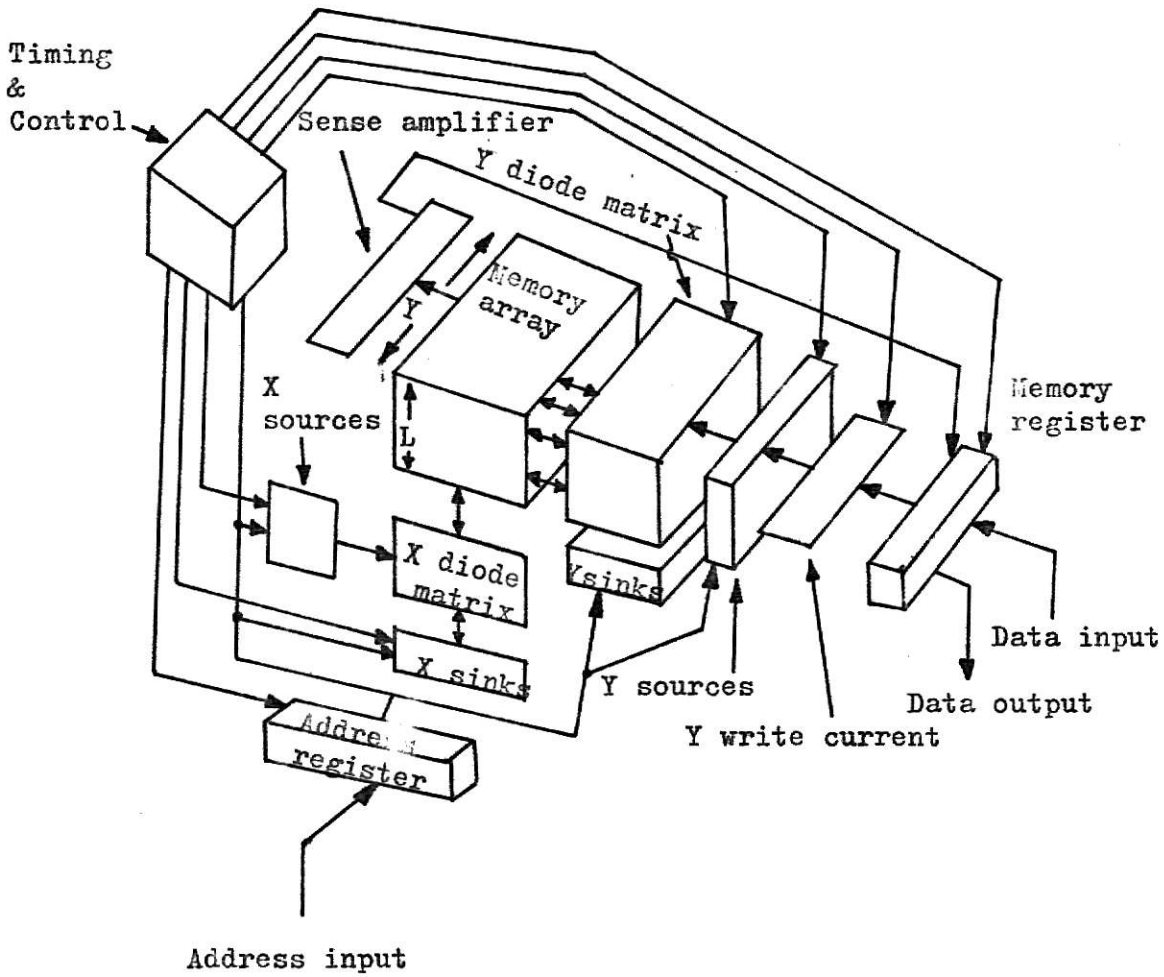


Figure 12. A $2\frac{1}{2}$D organized memory.

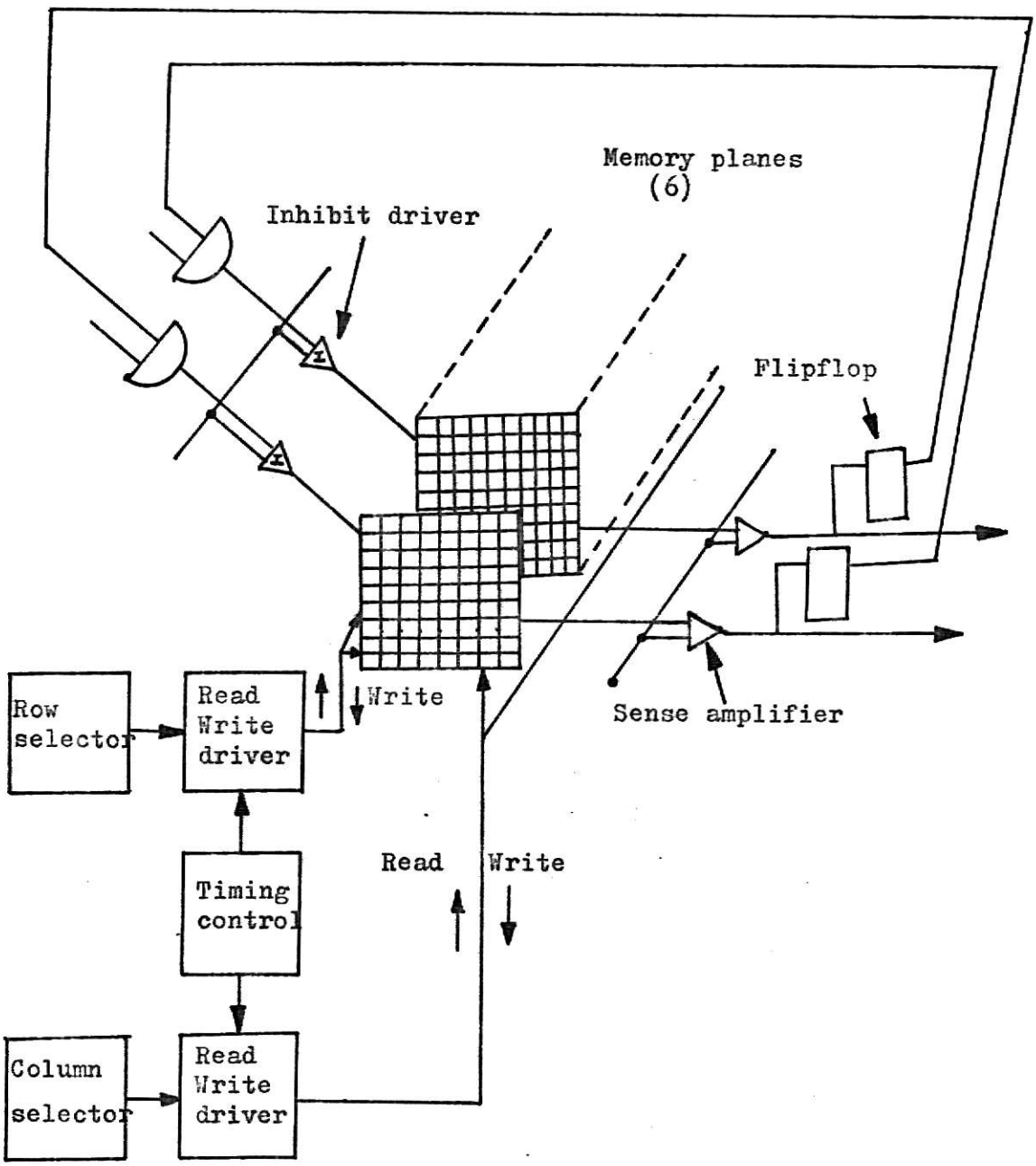


Figure 13. Typical organization of a Coincident current memory.

it. Column address and row address decoders select the core in each plane to be written into or read from. The drivers supply the necessary power and the proper polarity of current. The sense amplifier senses the voltage during read out and converts it to a " 1 " or a " 0 " according to its amplitude. Flip flops are used to feed a " 1 " back to the inhibit drivers to rewrite it into the core from which it had just been read out. Inhibit drivers convert the individual " 1 " and " 0 " into pulse. Memory is used by means of alternating read-write cycles so that data can be obtained from memory without destroying it.

Timing Sequence

The same timing sequence is generally used whether the computer is to write information into the memory or to read information from it. The total time taken by the entire timing sequence is called the memory cycle time and consists of two periods, the Read time and the Write time.

The Write Operation

To write a binary number 101011 into core location X_7Y_6 of memory, row 111 and column 110 should be selected. Therefore zeros are to be written into the selected cores of planes 2, and 4; so that the inhibit drivers for each of these planes are enabled to operate. That is, when the WRITE time begins (Figure 14) the drivers connected to the inhibit winding of planes 2, and 4 will drive current through the inhibit winding of these core planes.

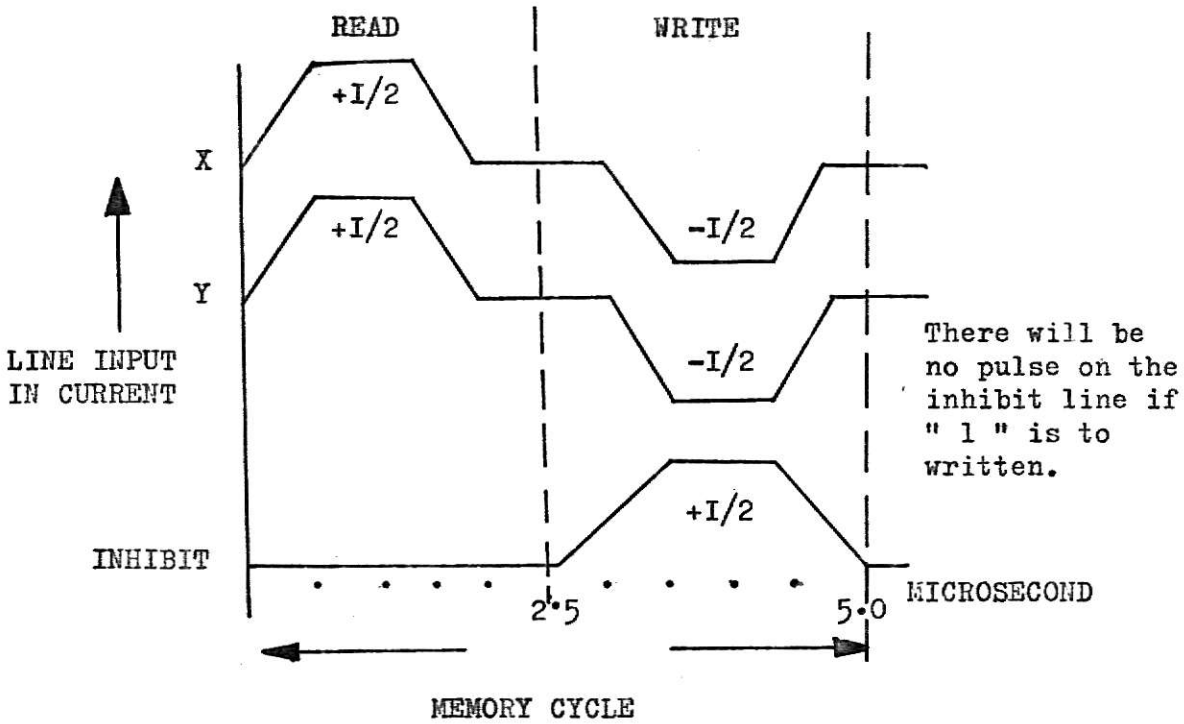


Figure 14. Memory cycle for a coincident current memory.

First, the correct drivers are selected. Since core X_7Y_6 in each plane is to be written, the drivers connected to X_7 and Y_6 lines are enabled to operate. When read pulses are applied, " 0's " are written into the X_7Y_6 core in each of the six planes. After 2 microsecond each one of the selected cores will contain " 0 ". At 2·5 microsecond after the sequence is initiated, the inhibit drivers connected to planes 2, and 4 are turned on Figure 14; 0·5 microsecond later WRITE time begins. " 1 " will be written into the selected cores of planes 1, 3, 5, and 6. The subtraction of the inhibit current (+Im/2) from the coincident current (-Im) through the selected cores in planes 2, and 4 will result in -Im/2 current. Thus selected cores of planes 2, and 4 remain in " 0 " state. After the end of memory cycle, selected cores in planes 1, 3, 5, and 6 will contain " 1 " and cores in planes 2, and 4 will contain " 0 ".

The Read Operation

To read information which is stored at location X_7Y_6 in memory, first the read currents (+Im/2) are applied to X_7Y_6 core in six memory planes. If a small signal is received at the sense amplifier connected to a given plane during this period, the selected core in that plane contains " 1 "; if no, or a very small, signal is received, the selected core in the plane contains " 0 ". The sense windings connected to planes 1, 3, 5, and 6 will produce a signal indicating " 1 " and the sense windings connected to the planes 2, and 4 will produce a small signal indicating " 0's " shown in Figure 8. Therefore the word stored was 101011. This word must be written back into the memory array. The output of each

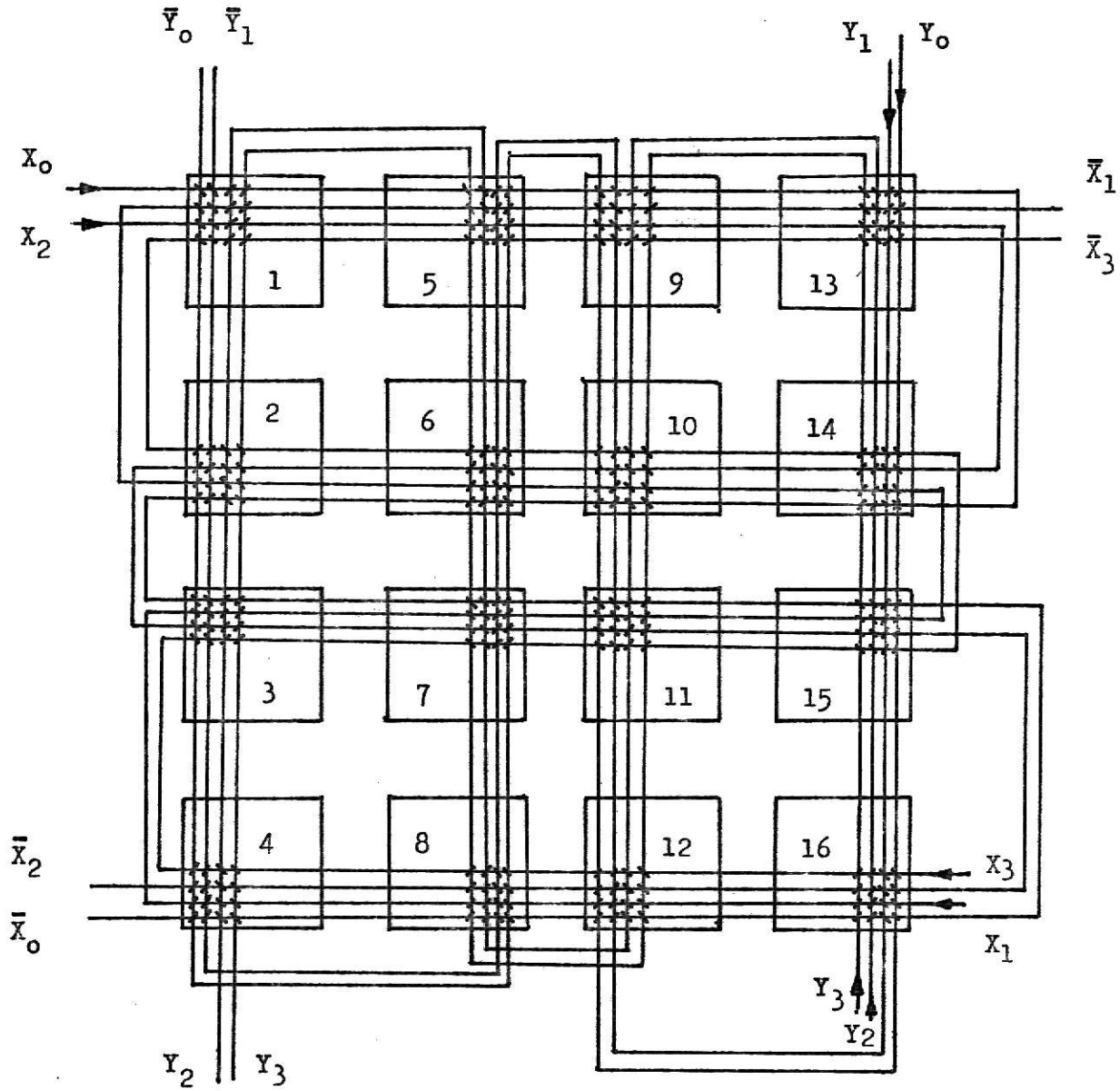
sense winding is amplified and stored in a flipflop. During the write cycle these flipflops control the inhibit winding drivers. Only the inhibit driver connected to planes 2 and 4 will be enabled by signals from the respective flipflops to conducts during the WRITE cycle. After the WRITE cycle, 101011 will be restored.

Coincident Current Memory Mats

In Figure 15, 4K x 16 stacks have 16 core mats of 4096 cores each. The figure also shows the core orientation in all mats for a 4K x 16 coincident-current stack and X and Y wiring to be used. In one mat there are 64 X lines and 64 Y lines. Consequently, combination of X and Y can select any one core from 4096 cores. This one is coincident current memory and memory consist of 16 mats. By selecting X_0Y_0 line 16 core can be selected, one core from each mat. There are 4096 cores (bits) in one mat. So memory has 4096 words, each word is 16 bits long.

4096 words x 16 bits = 4K x 16

Some general characteristics of coincident-current core memories is evident from this: the number of planes used generally equals the number of bits in the computer word; the number of X input lines times the number of Y input lines equals the number of words which can be stored in the array.



X_0Y_0 = One 16 bit word
X_0Y_1 = Second 16 bit word
X_0Y_2 = Third 16 bit word
There are 64 X lines (wires) and 64 Y lines (wires).
1 word 16 bit long
4096 words x 16 bits = 4K x 16

Figure 15. X & Y drive wiring of a typical 4K x 16 Coincident current memory.

Anti-Coincident Current Memory Mats

Figure 16 shows 8K x 8 Anti-coincident current memory mats and also X and Y drive windings. For the 8K x 8 memory mats, a change in X current direction will be requird to select the Anti-coincident mats. By applying current to X_o, and Y_o lines, mats 0, 1, 2, 3, 4, 5, 6, 7 can be selected, because they would get full current so information can be stored or taken out from X_oY_o core of mats. At the same time mat $\bar{0}$, $\bar{1}$, $\bar{2}$, $\bar{3}$, $\bar{4}$, $\bar{5}$, $\bar{6}$, $\bar{7}$ would not receive full current. They would not be selected. But by changing X_o current direction core mats $\bar{0}$, $\bar{1}$, $\bar{2}$, $\bar{3}$, $\bar{4}$, $\bar{5}$, $\bar{6}$, $\bar{7}$ would be selected and 0, 1, 2, 3, 4, 5, 6, 7 core mats wouldnot. As shown in Figure 23 the Anti-coincident 8K x 8 memory stack will have sixteen 4K mats on printed circuit board, eight mats on each side.

Sum of X_o & Y_o currents ONE WORD (Mat 0, 1, 2, 3, 4, 5, 6, 7)

Sum of $\bar{X}_o$ & Y_o currents SECOND WORD (Mat $\bar{0}$, $\bar{1}$, $\bar{2}$, $\bar{3}$, $\bar{4}$, $\bar{5}$, $\bar{6}$, $\bar{7}$)

1 Mat = 64 x 64 = 4096 Words = 4 K

2 x 4K x 8 = 8K x 8

8K = Total number of Words

8 = Length of Word

In Anti-coincident current memories, there will be less electronic circuitry. By changing the X current direction, two words can be selected.

Some general characteristic of Anti-coincident current core memories is opposite to that of coincident core memories. In this, organization number of bits in the computer word is half the number of planes used; twice the number of X input lines times the number of Y input lines equals the number of words which can be stored.

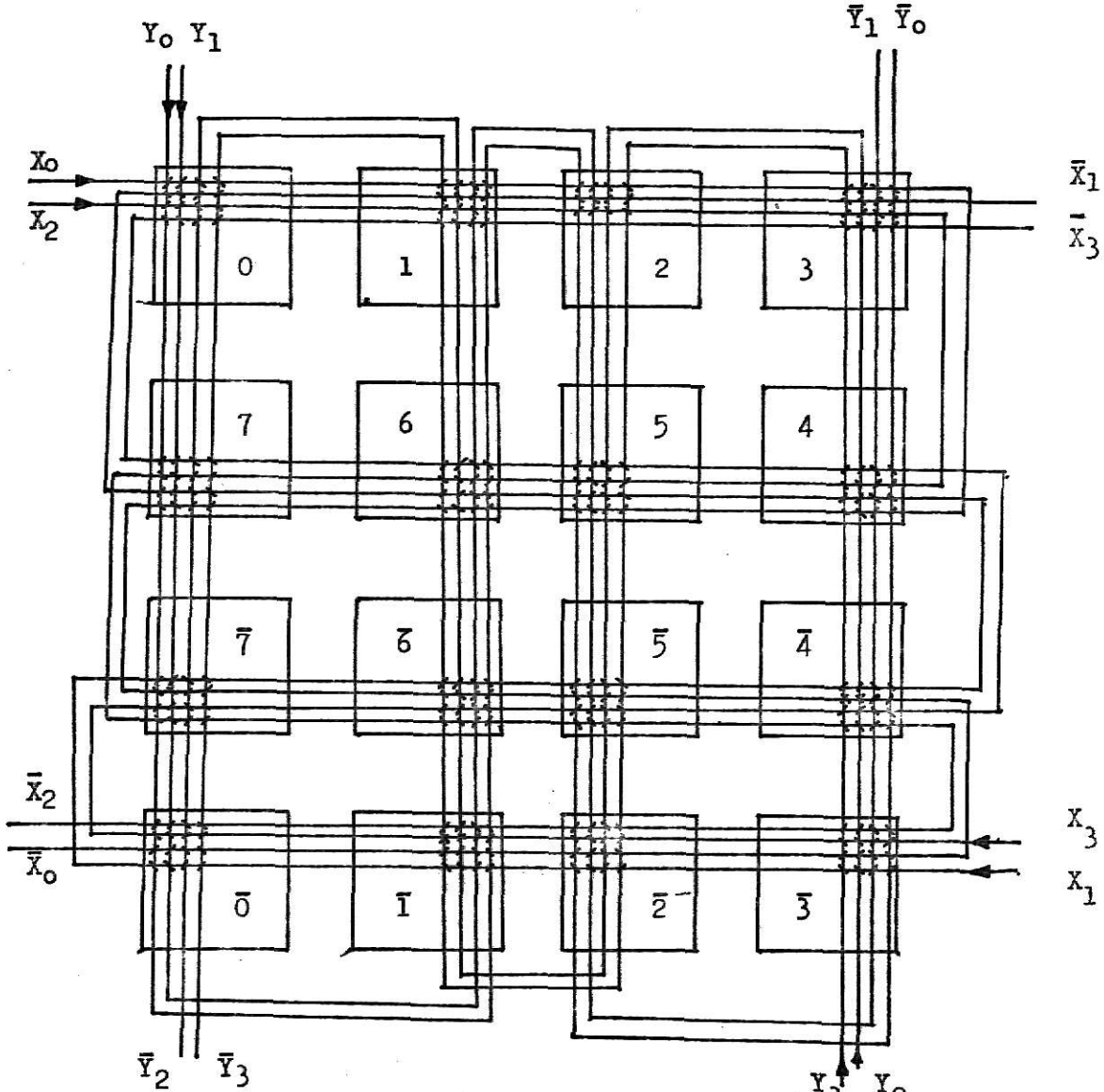


Figure 16. X & Y Drive Wiring of a typical 8K x 8

Anti-Coincident current memory.

TABLE I

COMPARISON BETWEEN
COINCIDENT AND ANTI-COINCIDENT CURRENT MEMORY

FOR 8K x 8 MEMORY

	COINCIDENT	ANTI-COINCIDENT
Decoding diodes	2	1
X & Y wires	4 (2 - X) (2 - Y)	3
Core matrix	1	1
Printed circuit board	1•2	1
Connector	1•5	1

CHAPTER IV

DRIVE AND RETURN WIRING

For a 4K memory, there are 64 X lines, and 64 Y lines. If there is one driver and one sink per line, it becomes more expensive. Also drivers and sinks take much of the room on a Printed Circuit board, so it is advantageous to look for some organization which reduces the number of drivers and sinks.

Let us examine an 8x8 core matrix. Without any type of arrangement for drivers and sinks, 8 drivers and 8 sinks are needed for X lines. It can be reduced by the arrangement shown in Figure 17.

As shown in Figure 17, there are 8 X lines, therefore (4x2) 4 sources (sinks) and 2 sinks (sources) can be used. To select line 0, source A and sink E is used. To select line 2, source B and sink E is used. In Figure 18 source A is driving lines 0, and 1. Sink E is sinking current from lines 0, 2, 4, and 6. Figure 19 illustrates 7 memory planes, inhibit driver, sources and sinks. During a read pulse to select line 0, source A and sink E are on. During a write pulse to select line 0, source E and sink A are on. For a 64 x 64 matrix, drive and return connections are shown in Figure 20.

Memory Driver

In Figure 21 there are 2 sources and 2 sinks. The device contains decoding capability with four address input lines. Two address input

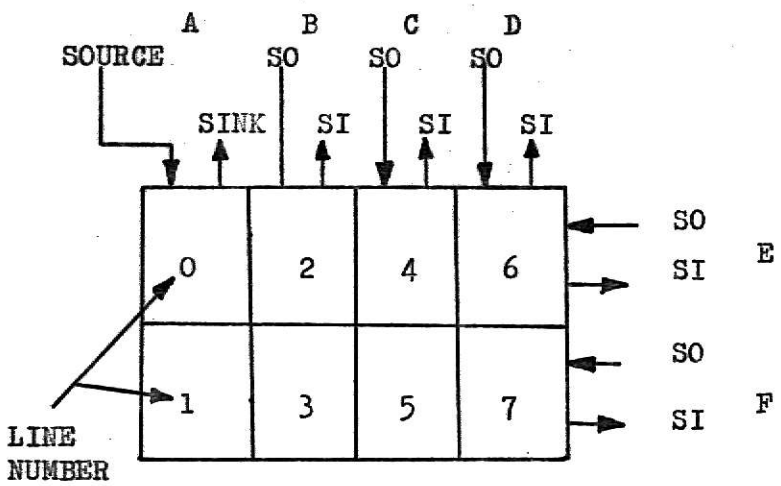


Figure 17. Line selection for source and sink.

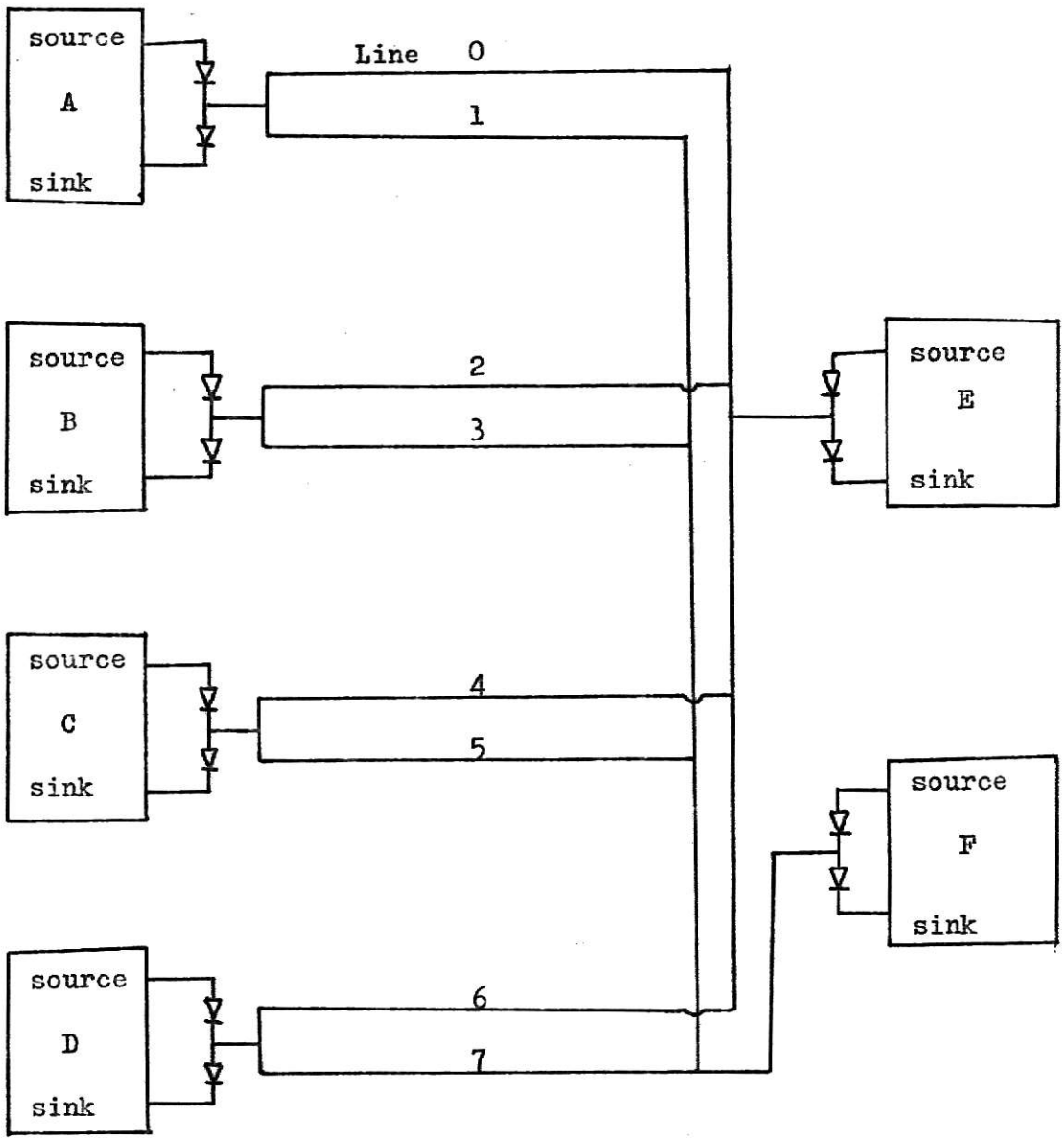


Figure 18. Diode matrix and Memory drivers for drive lines of cores.

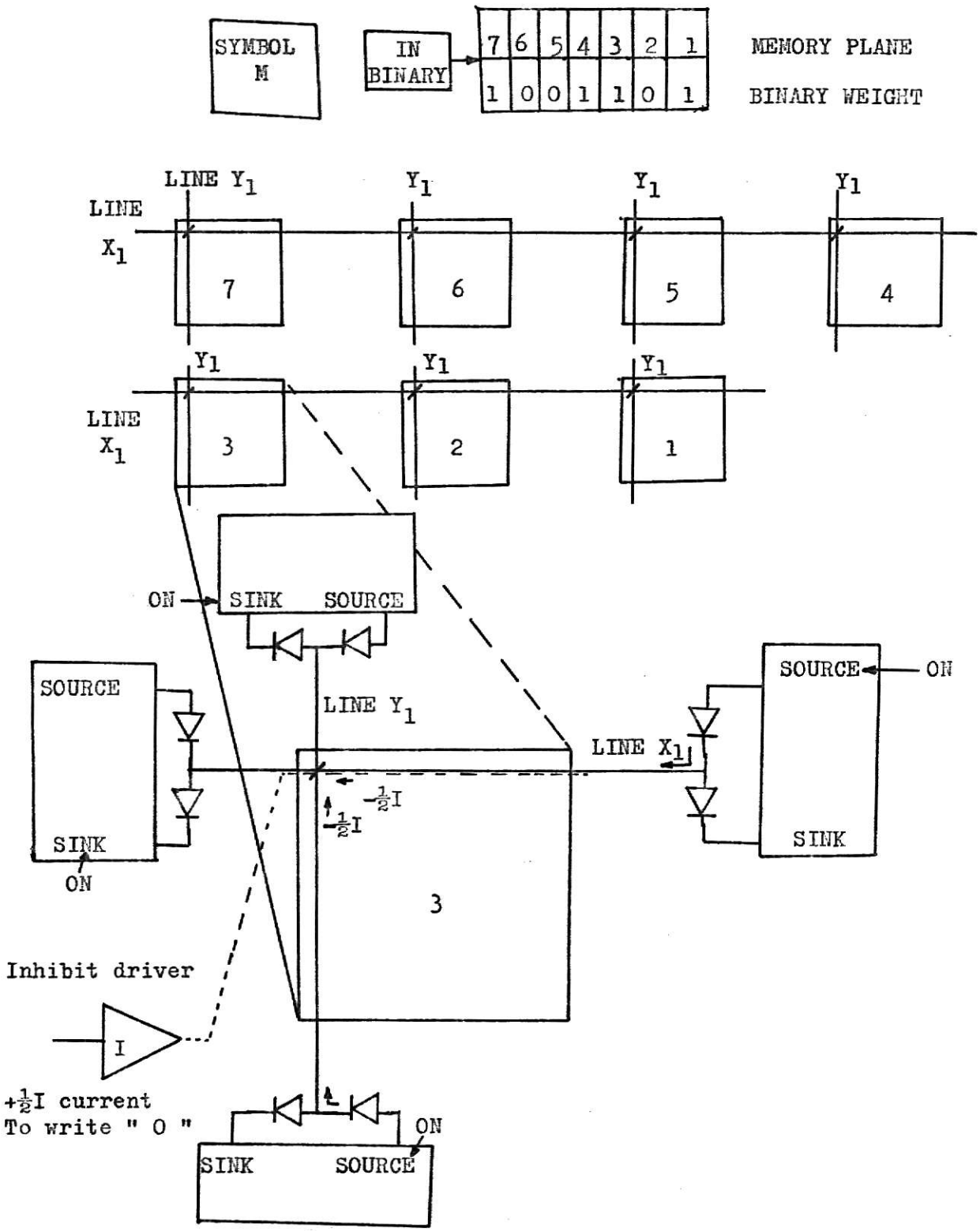


Figure 19. Memory planes, Inhibit driver, Sources and Sinks for a core memory.

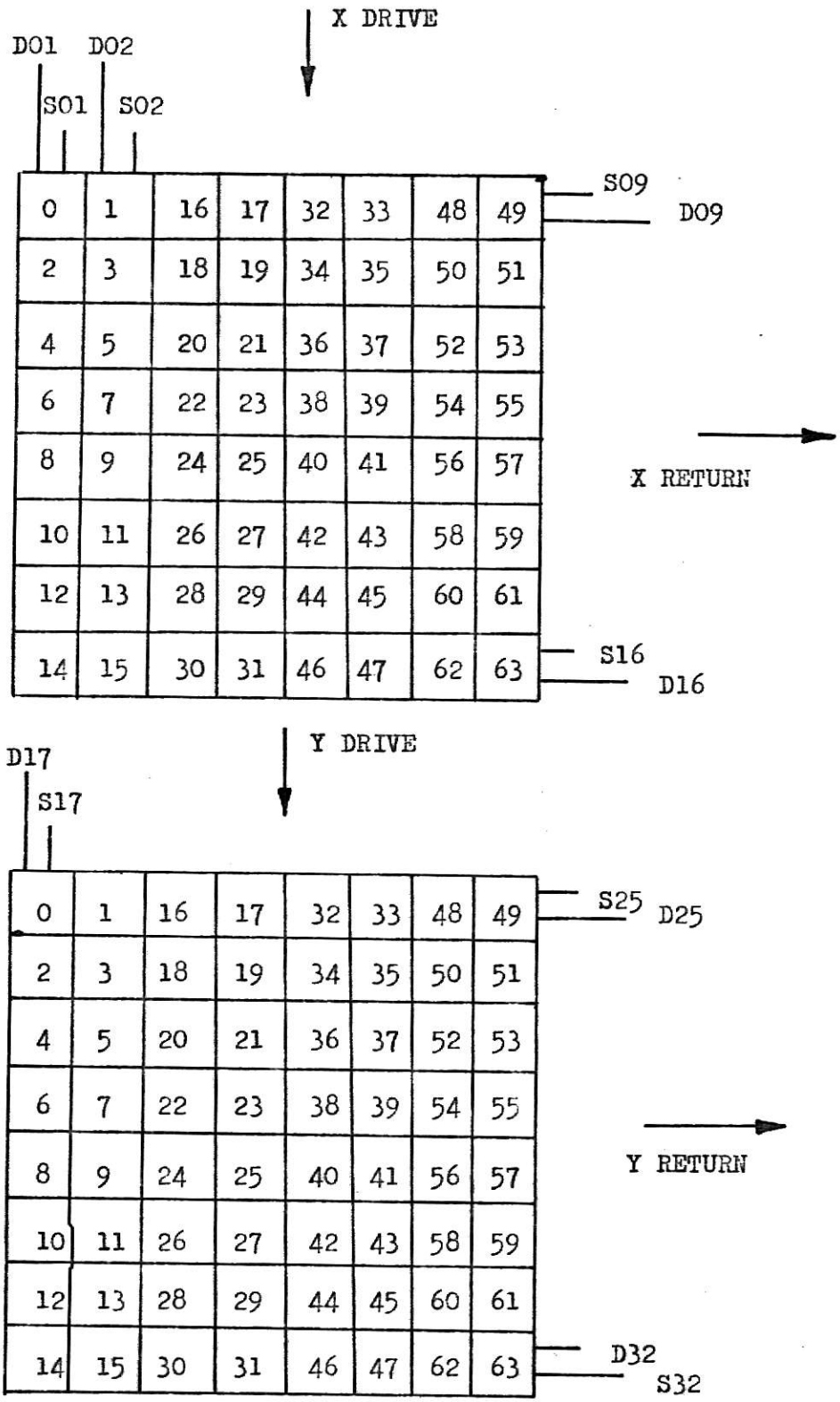
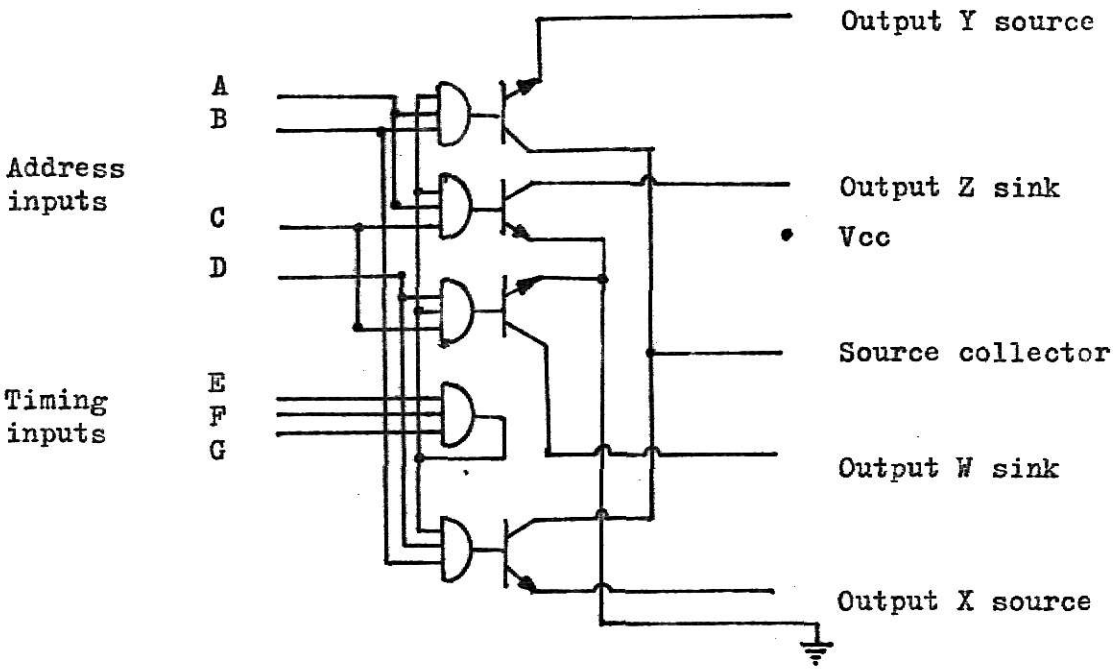


Figure 20. X and Y line selection for Source and Sink.



Vcc = Supply voltage to 5 AND gates

Source collector = Voltage for two source (X,Y)

TRUTH - TABLE

INPUTS							OUTPUTS			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON

Figure 21. Memory driver with decode inputs.

lines (B & C) are used to select mode (i. e. source or sink). Input address lines A and D are used to select Y/Z or W/X respectively. As shown in Figure 21 to select X source, address input lines B and D, and timing input lines E, F and G should be high (" 1 " state).

Design of Sense Winding

The X, Y, and inhibit windings are relatively simple to design. The configuration of sense winding dominates the design of the matrix because electrical disturbances introduced into the sense winding must be considered. The three types of disturbance introduced are as follows.

(1) Disturbance due to the cores themselves and due to selected X and Y cores.

(2) Magnetic pickup which occurs because the sense winding and the X and Y wires are inductively coupled loops. This problem is solved by reducing the effective area of the sensing loops to the minimum. The various memory organizations use different sense line configurations, and current drive techniques. However, in all the configurations the sense winding is routed so as to obtain an optimum signal-to-noise ratio. For this the sense winding goes through half the core of array in one direction and through the other half in the opposite direction.

(3) Electrostatic pickup is one of the most troublesome of all disturbances. The capacitance between the sense winding and the X and Y wires is large. It is difficult to prevent the sense winding from moving with X and Y wires. A correctly designed sense winding moves

in such a fashion that no net voltage appears across the two sense windings output. Information is coupled out of the sense winding either by means of a difference amplifier or by a balanced transformer.

Bifilar Sense Winding

Figure 22 illustrates a BIFILAR sense winding. The arrows on the X and Y lines show the manner in which these wires were driven with respect to each other to produce the same action. The signs next to each the cores show the polarity of the linkages of the sense winding. Moving from the center of the sense winding toward either A or B, the same pattern of polarities is encountered and the winding is symmetrical about the center. Moving from C toward A, the excited linkages induces negative and positive and cancellation occurs.

Multiple Sense Winding

It is possible to provide a multiplicity of sense windings in a large array. Using the output from the sense winding which links the desired core decreases the effective size of the plane as far as noise is concerned.

As shown in Figure 23 there is a 128 x 128 plane. If there are four sense winding, the large plane is as effective as four 64 x 64 planes.

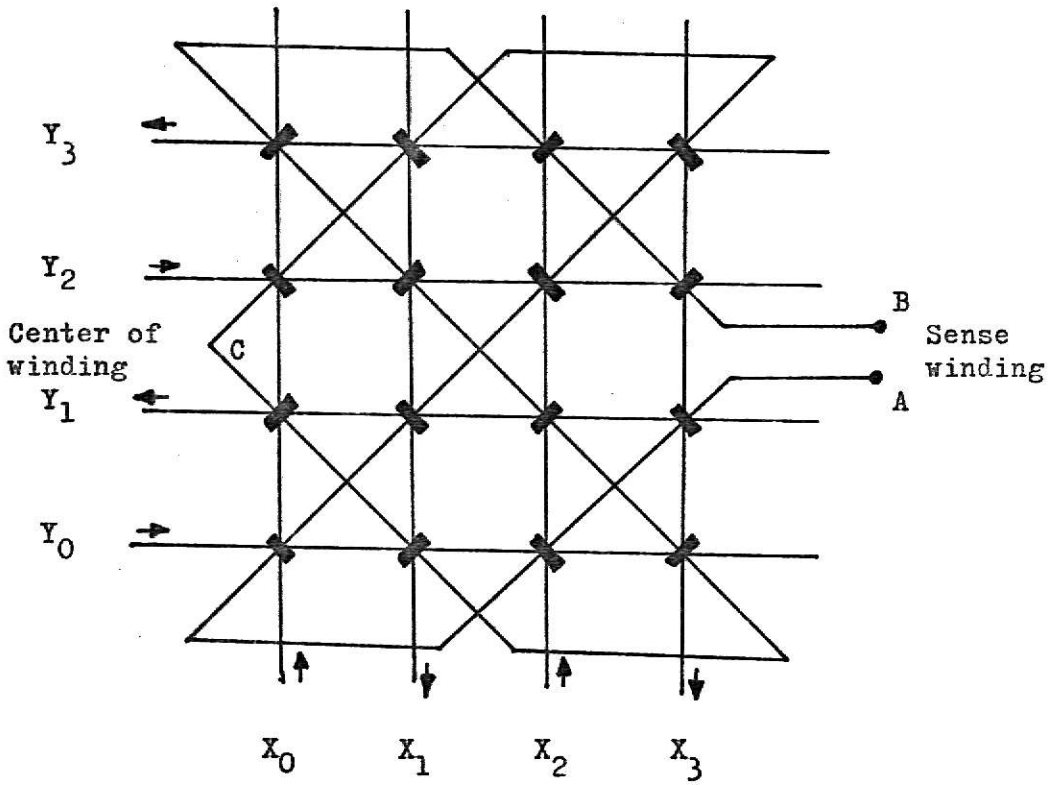


Figure 22. Bifilar Sense Winding of Cores.

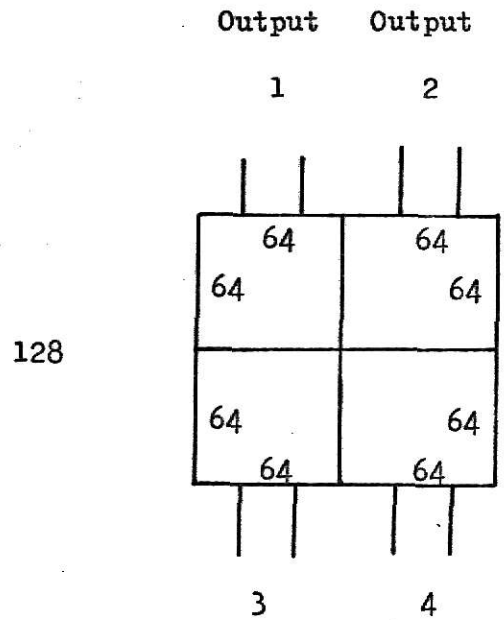


Figure 23. Blocks of four 64 x 64 sense windings of 128 x 128 core matrix.

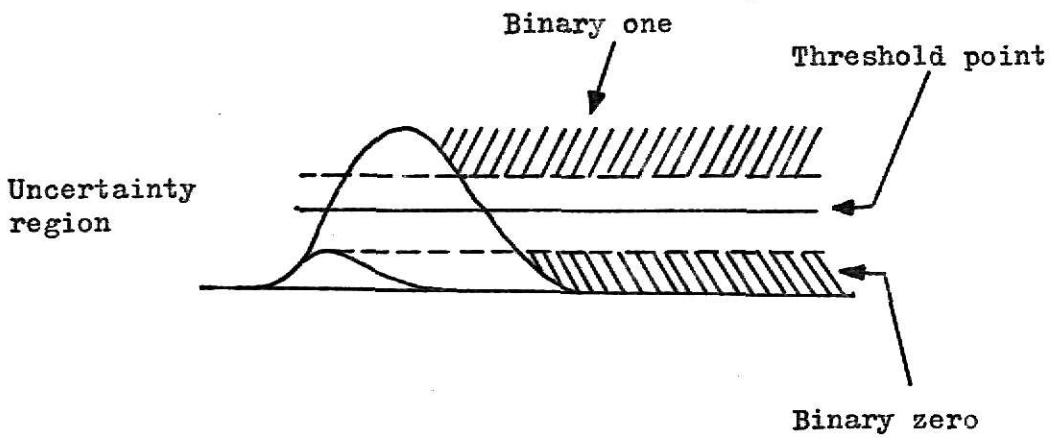


Figure 24. Typical sense amplifier input signals showing relationships between binary zero and binary one and the threshold point and uncertainty region.

Sense Amplifier Design Criteria

Many factors must be considered in the design of an integrated core memory sense amplifier.

(1) The design should be as versatile as possible.

(2) The design must meet a wide variety of speed requirements and should be suitable for low cost fabrication.

(3) The threshold should be adjustable in order to meet the maximum number of requirements with a single amplifier.

(4) The uncertainty region should be as small as possible.

(5) The power supply required should be commonly used value.

(6) Sense amplifier requires a strobe to " enable " the amplifier at the optimum point should be provided.

Typical Core Output Signal at Sense Amplifier

Figure 24 shows the typical signal as seen at the input to the sense amplifier. The amplitude of the " 1 " signal depends on the size of the core and the rise time and amplitude of the selected currents from the core drivers. The area between " minimum one signal " and " the maximum zero signal " is called the uncertainty region. This area should be ideally as large as possible, since it is very important in the overall performance of the memory subsystem. Normally, the threshold of the amplifier will be set in the middle of the uncertainty region.

Sense Amplifier Interfacing with Memory

Figure 25 shows one channel of the sense amplifier connected to the sense winding of the memory plane. R_1 and R_2 are the terminating resistors of a sense winding and a d. c. bias path to ground for the input of the amplifier. R is in the range of 2·5 ohms to 200 ohms depending on the characteristic impedance of the sense winding. Closely matched terminating resistors are desirable to keep input offset at a minimum, which helps to minimize the uncertainty region.

Inhibit Driver

The function of the inhibit driver is to drive cores with +I/2 current, at command. To write " 0 " it delivers +I/2 current. The inhibit driver is on, after the end of the Read cycl and the beginning of the Write cycle. At low level input, transistor Q_2 is turned off and transistor Q_1 is turned on due to its voltage difference between base and emitter. Figure 26 shows a typical inhibit driver. Figure 27 shows an inhibit driver control circuit. Inhibit winding with the direction of read current are shown in Figure 28.

Nondestructive Read-Out

One of the disadvantages of coincident current operation of a core storage unit is that information is destroyed during reading and must be rewritten. Reading time is long and loss of information during

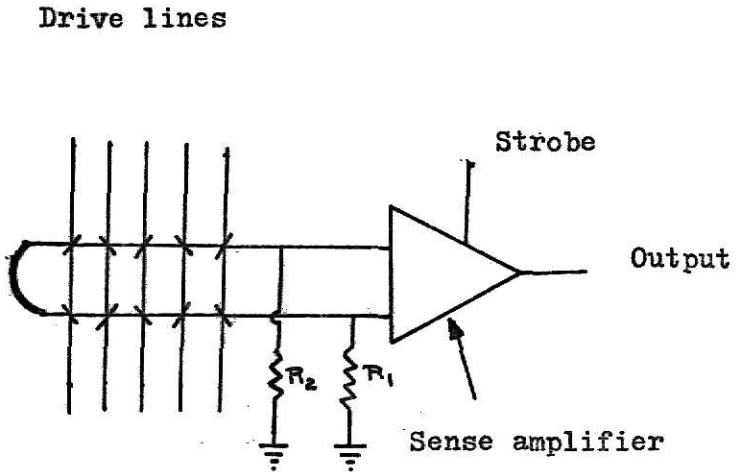


Figure 25. Sense Amplifier connection with drive lines.

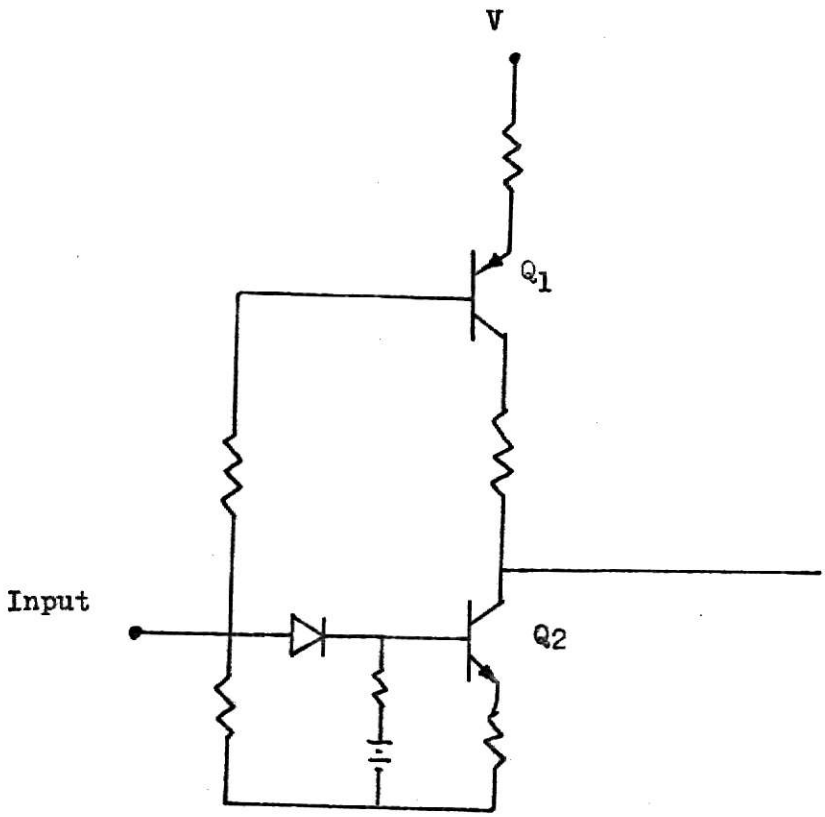


Figure 26. Inhibit Driver for a core memory.

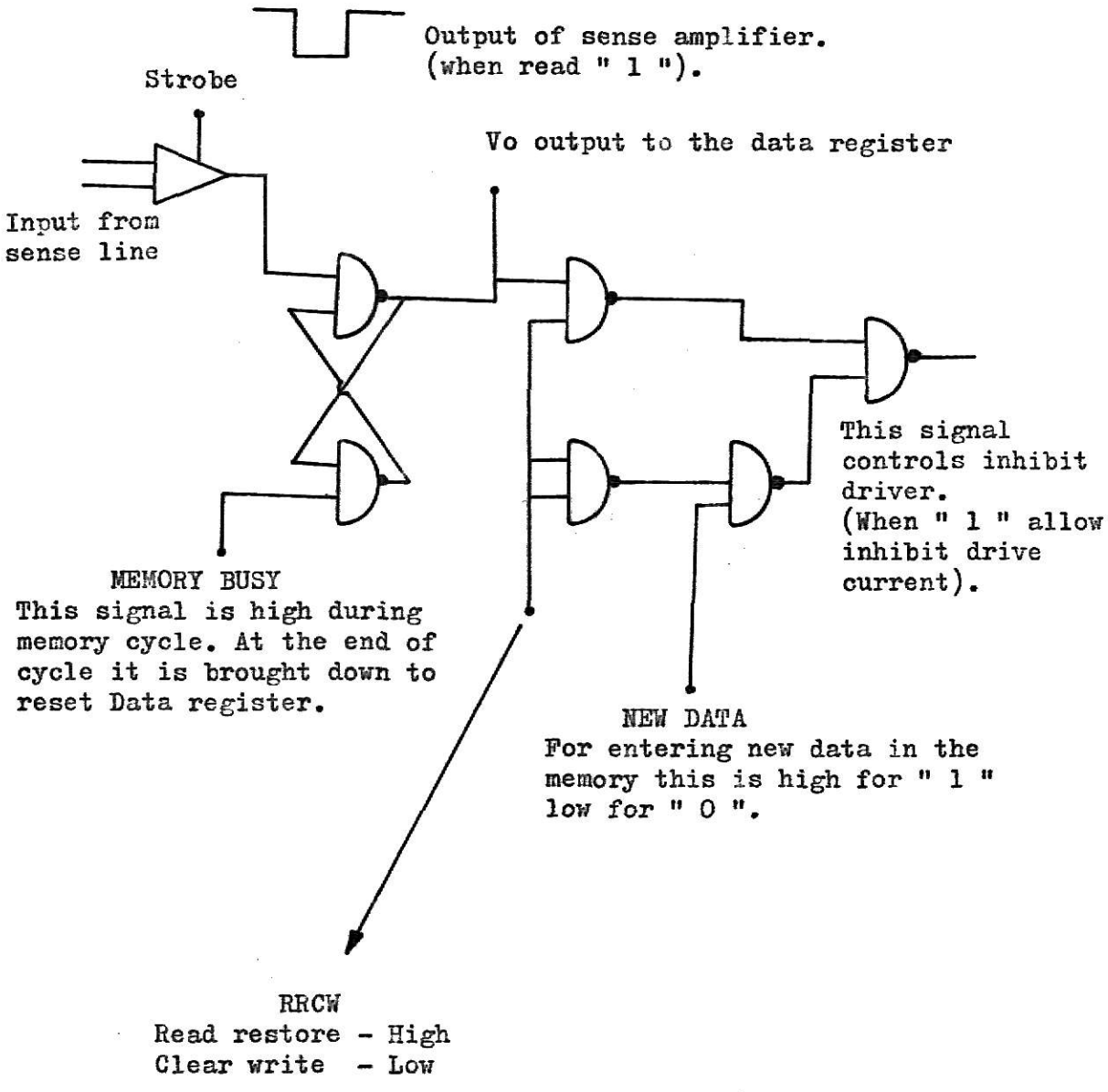


Figure 27. A typical control circuit for a core memory.

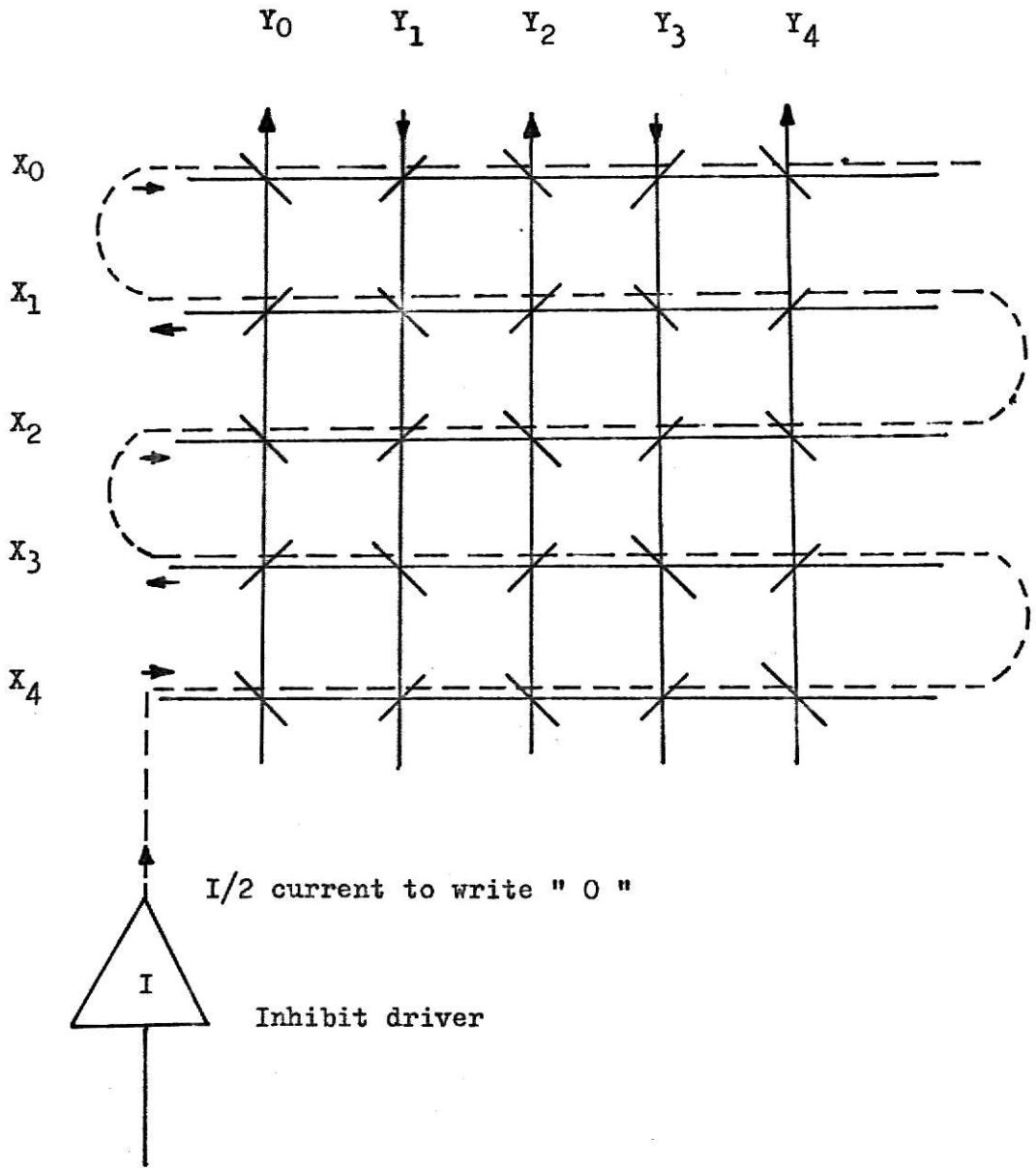


Figure 28. Inhibit Winding of Cores.

transfer from an electronic register and back to the core matrix may occur. In most computing applications, reading occurs more often than writing. Therefore, to shorten the reading time, nondestructive read-out might be used; this would greatly increase computational speeds.

If a nondestructive reading method is to replace the present destructive method, it should satisfy the following requirements.

(1) Reading time should be short.

(2) Writing time should not be much longer than that required by presently used methods.

(3) The method should be adaptable to storage units of large capacity.

(4) The fabrication cost of a nondestructive system should not be much greater than that of destructive systems.

CHAPTER V

CONCLUSION

The development of the magnetic core storeware has been in the direction of faster operation and larger capacity. It can be safely predicted that within the coming years storage devices will operate at a cycle time of much less than 1 microsecond. (Nowadays there are many with 700-900 nanosecond cycle time). These devices will find applications in current and future milli microsecond computers.

One of the disadvantages of coincident current operation of a core storage unit is that information is destroyed during reading and must be rewritten. The answer to that question is the nondestructive read out. Reducing the memory cycle time in half is another big step forward.

A continuous trend in design of core storage unit is the reduction of physical size. Initial units were excessively large and unsuitable for use in mobile equipment. By developing more closely packed matrices, designers have been able to produce very compact units. Considerably higher packing factor can be achieved in the future. Future core-storage units will fluxuate between fairly large, very high speed devices requiring many transistors and large-capacity, compact, slow, reliable units requiring few transistors. Undoubtedly there will be some intermediate units of medium capacity which will be highly reliable and compact for mobile use.

In addition to core memory there are other kinds of memories such as semiconductor, plated wire etc. Core memories have dominated the

market by sheer momentum. It is hard to believe that core memories can continue dominating the field in the future since the speeds already attained by semiconductor and plated wire memories are totally beyond the capabilities of core. Furthermore, there is greater difficulty in automating core, plated wire technologies are readily automated, and eventually this will force core out of its last stronghold-mass storage memories.

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GLOSSARY

ADDRESS - A number that designates a register, a memory location, or other source of information.

BIT - An abbreviation of binary digit, the smallest unit of information in the binary system.

BUFFER - A temporary storage site used to compensate for differences in data flow rates during data transfers.

CPU - An abbreviation for Central Processing Unit. The section of a computer that contains the arithmetic, logic, and control circuits. In some systems it may also include the storage unit.

CLEAR - To restore a storage device, or binary stage to a prescribed state, usually that denoting 0.

LOCATION - Storage position or register uniquely specified by an address.

MAT - More than one core and core winding on a plane.

MEMORY - The portion of a computer that stores information in a form that can be recalled by computer hardware.

PARITY BIT - A binary digit appended to an array of bits to make the sum of all the bits always odd or always even. A parity check tests whether the number of " 1 " in an array of bits is odd or even.

PROGRAM - Sequence of instructions to be used by a digital computer in solving a problem.

RANDOM ACCESS - Access to computer storage where the next location from which information is to be obtained may be chosen at random.

READ - To acquire and transmit information, from one form of storage to another.

REGISTER - The hardware for storing one machine word. The register length is equal to the number of bits it can store.

RESET - Clear.

RESTORE - To return a word to its initial state.

WORD - A set of bits that is treated, stored, and transported as a unit. This is the smallest addressable unit of information.

ACKNOWLEDGMENT

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FERRITE CORE MEMORY DESIGN

by

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AN ABSTRACT OF A MASTER'S REPORT

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MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY

Manhattan, Kansas

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The ever increasing demands for information processing have necessitated the making of computers in all sizes for big and small jobs. The heart of any computer, whether large or small is its memory.

The most common device used in high speed digital memories today is a ferrite core. In core memories there are three main types of organizations which may be traced back to two generic forms; bit organized and word organized. The 3 D (Bit organized), 2 D (Word organized) and $2\frac{1}{2}$ D (Hybrid of 3 D and 2 D) are the main core memory organizations in use today.

Drive and return wiring is also one of the basic factor to consider in a core memory design. Sources and Sinks take much of the room on a printed circuit board, so it is advantageous to look for some organization which reduces the number of sources and sinks.

The memory cycle time consists of two periods, the read time and the write time. In most computing applications, reading occurs more often than writing. Therefore to shorten the reading time nondestructive read out might be used; this would greatly increase computational speed.