TRANSISTOR CIRCUIT DESIGN

by

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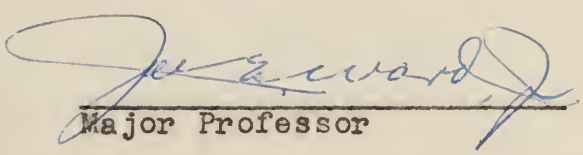

Major Professor

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INTRODUCTION

One problem that is prevalent in the design of any circuit that contains an active element is the proper representation of the active element by an equivalent circuit. The equivalent circuit for the electronic vacuum tube is well established and is the foundation for most beginning electronic textbooks. The parameters that make up the equivalent circuit can, in most cases, be taken directly from the manufacturer's data sheet, and the operation of the tube can be predicted quite accurately from the equivalent circuit.

There are special cases where the basic equivalent circuit is no longer an accurate representation of the tube. One such case is in the upper useful frequency range of the tube where phenomena such as transit time effects take place. In this frequency range the basic equivalent circuit is no longer accurate and must be revised to include the special effects.

In this report a basic equivalent circuit for the junction transistor is presented. The equivalent circuit is analogous to that of the vacuum tube in that it is relatively simple and the parameters can be taken directly from the manufacturer's data sheet or calculated using some simple relationships.

The transistor parameters specified by the manufacturer usually have a wide range in value, and in many cases the parameters are not adequately specified. It is up to the design engineer to approximate the parameter not adequately specified and to design the circuit to the specification at least to the first

approximation. It is in making these calculations that the equivalent circuit presented performs its most useful function. The equivalent circuit is useful as a first approximation to determine if the circuit meets the design specifications whether an upper or lower limit[1] transistor is used.

This report does not discuss the physical action that takes place in the transistor that determines the parameter. There are many sources available where the subject is developed thoroughly.[2,3,4]

This report deals only with small signal (linear) applications of the transistor. The equivalent circuit, and the equations derived from the circuit, are utilized to analyze certain specific transistor applications. The applications analyzed include: (a) negative feedback, (b) high-frequency considerations, including neutralization of the transistor, and (c) bias consideration.

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[1]The transistor parameters are usually specified by giving a maximum, minimum, and typical value. Upper and lower limits mean the maximum and minimum values of the parameter specified.

[2]W. Shockley, "The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors," Bell System Technical Journal, vol. 28, pp. 435-489, July, 1949.

[3]A. Lo, R. Endres, J. Zawels, F. Waldhauer, C. Cheng, Transistor Electronics, Prentice-Hall, Inc., Englewood Cliffs, N. J., pp. 272-309.

[4]L. Giacoletto, "Study of P-N-P Alloy Junction Transistor through Medium Frequencies," RCA Review, vol. 14, pp. 506-562, December, 1954.

EQUIVALENT CIRCUIT

There are two forms of the basic equivalent circuit discussed, the bridged-T and the hybrid-π. The low-frequency forms of the two are illustrated in Figs. 1 and 2.

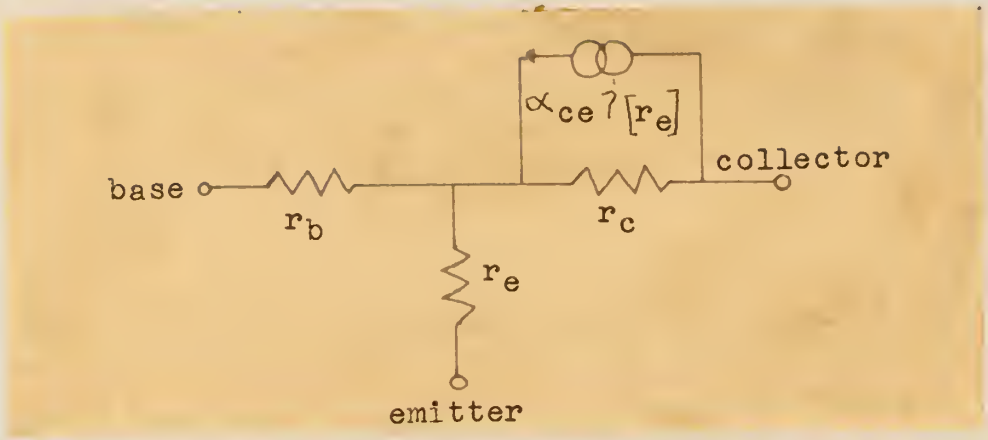

Fig. 1. Low-frequency bridged-T equivalent circuit.

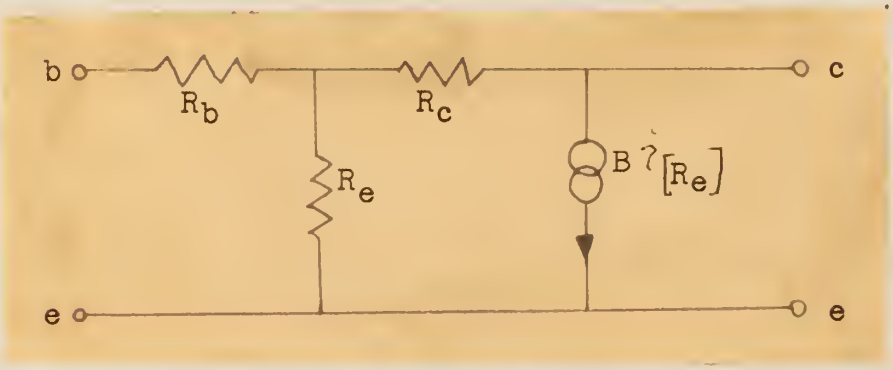

Fig. 2. Low-frequency hybrid-π equivalent circuit.

The T-equivalent circuit is the basic equivalent circuit used extensively in the literature (for example, see Lo, et al.)[1]. The notation, $\dot{?}[r_e]$, used in the equivalent circuit indicates the

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[1]A. Lo, R. Endres, J. Zawels, F. Waldhauer, C. Cheng, Transistor Electronics, Prentice-Hall, Inc., Englewood Cliffs, N. J., p. 43.

current flowing through the resistor in the brackets. To further clarify $B'[R_e]$ means B times the current flowing through R_e.

The definition of the parameter and their dependency (if any) on other parameters for the -T equivalent are as follows.

r_b - Base Spreading Resistance

This resistance represents the resistance of the material from which the base is made. r_b is sometimes referred to as the base connection resistance or the extrinsic base resistance. Typical values of r_b are from five ohms for a power transistor to several hundred ohms for small power units. This parameter is essentially independent of voltage and current but has a positive temperature coefficient of approximately 0.7 per cent per degree C.

r_e - Intrinsic Emitter Resistance

There is a direct relationship between the emitter resistance r_e and emitter current I_e. The relationship is given by $r_e = K/(I_e \text{ in } M_a)$, where K is a constant with the dimension of millivolts, and (I_e in M_a) is the emitter d-c bias current in milliamperes. For most transistors K = 26 is a good approximation.[1,2] Temperature, collector voltage, and collector current have little effect on this parameter.

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[1] Ibid., p. 288.

[2] P. Jochems, O. Memelink, L. Tummers, "Construction and Electrical Properties of a Germanium Alloy-diffused Transistor," Proceedings of the IRE, vol. 46, no. 6, p. 1162, June, 1958.

α_{ce} - Short-circuit Current Amplification Factor

α_{ce} is the short-circuit current amplification factor between collector and emitter. In practically all cases $.9 > \alpha_{ce} < 1$. The current amplification factor is a function of collector current, collector voltage, and temperature.

r_c - Collector Resistance

The value of r_c is primarily determined by the surface resistance across the base to collector junction. r_c can also be defined as the inverse slope of I'_{co} (leakage current) with collector voltage. Typical values of r_c are from a few thousand ohms to hundreds of megohms for low-power silicon devices.

The hybrid-π equivalent circuit can be derived from the T-equivalent circuit by writing equations for both and relating equivalent terms.

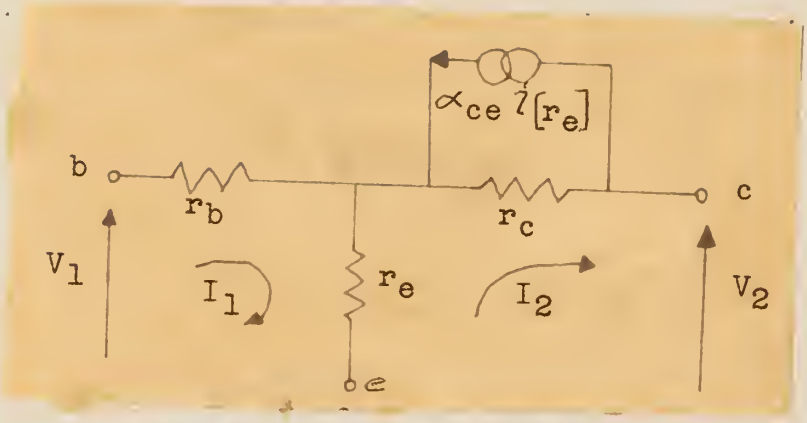

Fig. 3. T-equivalent circuit.

Using loop current analysis and writing equations for the input and output voltage for the T-equivalent circuit yields:

$$V_1 = I_1(r_b + r_e) - I_2 r_e \tag{1}$$

$$-V_2 = -I_1 r_e + I_2(r_e + r_c) + \alpha_{ce}\, i[r_e] r_c \tag{2}$$

The current through r_e is

$$i[r_e] = I_1 - I_2 \tag{3}$$

Substituting Eq. (3) into Eq. (2) yields

$$-V_2 = -I_1(r_e - \alpha_{ce} r_c) + I_2(r_e + r_c[1 - \alpha_{ce}]) \tag{4}$$

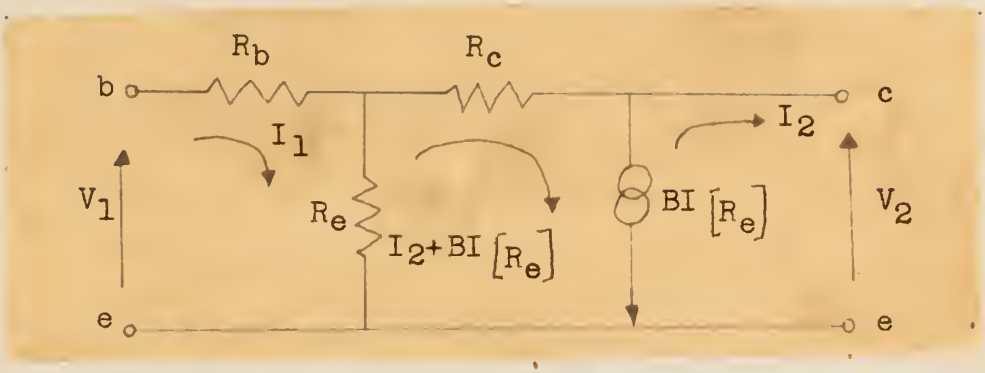

Fig. 4. π-equivalent circuit.

The expressions for the input and output voltages for the hybrid π-equivalent circuit are:

$$V_1 = I_1(R_b + R_e) - (I_2 + BI[R_e])R_e \tag{5}$$

$$-V_2 = -I_1(R_e) + (I_2 + BI[R_e])(R_e + R_c) \tag{6}$$

The current through R_e is

$$I[R_e] = \frac{I_1}{1 + B} - \frac{I_2}{1 + B} \tag{7}$$

Substituting Eq. (7) into Eqs. (5) and (6) yields

$$V_1 = I_1\left(R_b + \frac{R_e}{1 + B}\right) - I_2 \frac{R_e}{1 + B} \tag{8}$$

$$-V_2 = -I_1\left(\frac{R_e}{1 + B} - \frac{BR_c}{1 + B}\right) + I_2\left(\frac{R_e}{1 + B} + \frac{R_c}{1 + B}\right) \tag{9}$$

By comparing Eqs. (1) and (4) with Eqs. (8) and (9), the following relations are obtained.

$$r_b = R_b \tag{10}$$

$$r_e = \frac{R_e}{1 + B} \tag{11}$$

$$\alpha_{ce} = \frac{B}{1 + B} \tag{12}$$

From Eq. (12), B can be determined as

$$B = \frac{\alpha_{ce}}{1 - \alpha_{ce}} \tag{13}$$

and since $1 > \alpha_{ce} > .9$, $B >> 1$.

B is defined as the low-frequency, or d-c, short-circuit current gain between base and collector. The relationship between the low-frequency and d-c short-circuit current gain is discussed further in a later section.

From Eq. (10), R_e can be determined.

$$R_e = r_e(1 + B) \ , \ B >> 1 \tag{14}$$

$$R_e = Br_e \tag{15}$$

The definitions given previously for the T-equivalent circuit apply to the parameter for the π-equivalent circuit if the correct conversion factors stated above are used.

The hybrid π-equivalent circuit is the most useful of the two equivalent circuits presented, and will be used as the basis equivalent circuit for the remainder of this report.

The equivalent circuit thus far developed is useful only for low-frequency application. To extend the usefulness of the equivalent circuit to higher frequencies, reactive elements must be included to represent the variations of the transistor parameters with frequency. Figure 5 is the final equivalent circuit

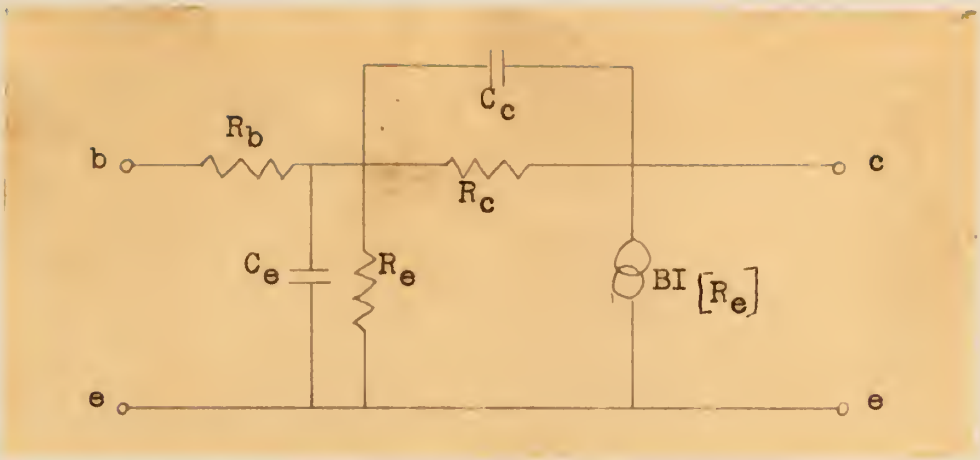

Fig. 5. Hybrid π-equivalent circuit.

which is useful to the first approximation over the major portion of the transistor frequency range. The equivalent circuit is similar to those developed in the literature[1,2,3], but with approximation made to eliminate the parameters which have little effect on the overall characteristics of the transistor. As is the case of the resistive components, the values of capacitances can be taken directly from the manufacturer's data sheet or calculated, as shown later under definitions of transistor parameters.

Before elaborating on the frequency dependent parameters, the transfer matrix shall be determined from the equivalent circuit for the three basic configurations: common emitter, common collector, and common base. Approximations will also be made to

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[1]E. Wolfendule, The Junction Transistor and Its Application, The Macmillan Company, New York, 1958, pp. 103-111.

[2]P. Jochems, O. Memelink, L. Tummers, "Construction and Electrical Properties of a Germanium Alloy-diffused Transistor," Proceedings of the IRE, vol. 46, no. 6, p. 1162, June, 1958.

[3]L. Giacoletto, "Study of P-N-P Alloy Junction Transistor from D-c Through Medium Frequencies," RCA Review, vol. 14, p. 561, December, 1954.

simplify the matrices for low and high frequencies. From the transfer matrix the voltage gain, current gain, input impedance, and output impedance will be determined.

Equivalent Circuit Analysis

To illustrate the method of analysis using the transfer matrix, a general case is given below.

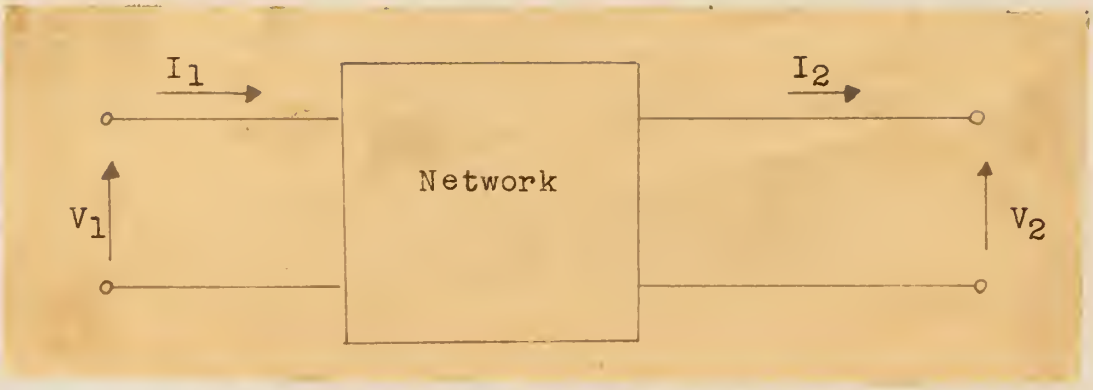

Fig. 6. General four-terminal network.

For any four-terminal network the following equations can be derived:

$$V_1 = AV_2 + BI_2 \tag{16}$$

$$I_1 = CV_2 + DI_2 \tag{17}$$

The transfer matrix can be written directly from Eqs. (16) and (17).

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{18}$$

For the purpose of deriving the voltage gain, current gain, input impedance, and output impedance, the general network shown in Fig. 6 is modified as shown in Fig. 7.

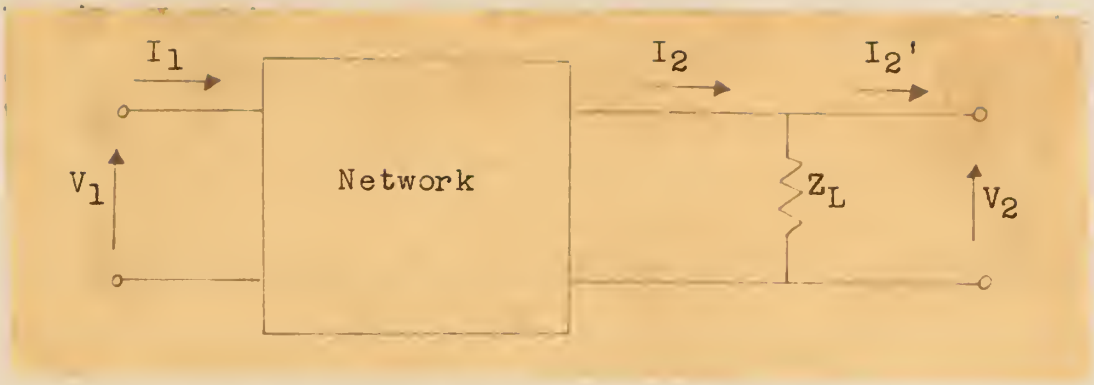

Fig. 7. General four-terminal network terminated by a load impedance.

Writing the transfer matrix for the two cascaded networks shown in Fig. 7 yields

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A & B \\ C & D \end{vmatrix} \begin{vmatrix} 1 & 0 \\ 1/Z_L & 1 \end{vmatrix} \begin{vmatrix} V_2 \\ I'_2 \end{vmatrix} \tag{19}$$

Carrying out the matrix multiplication and setting $I'_2 = 0$, since there is no load on terminal 3, yields

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A + B/Z_L & B \\ C + D/Z_L & D \end{vmatrix} \begin{vmatrix} V_2 \\ 0 \end{vmatrix} \tag{20}$$

Solving Eq. (20) for the voltage gain gives

$$K_v = \frac{V_2}{V_1} = \frac{1}{A + B/Z_L} \tag{21}$$

Letting $V_2 = I_2 Z_L$ in Eq. (20) and solving for the current gain gives

$$K_i = \frac{I_2}{I_1} = \frac{1}{CZ_L + D} \tag{22}$$

Again using the relationship that $V_2 = I_2 Z_L$ and using Eqs. (21) and (22), the input impedance can be determined.

$$Z_{in} = \frac{K_i Z_L}{K_v} = \frac{AZ_L + B}{CZ_L + D} \tag{23}$$

To determine the output impedance when the input is terminated by an impedance, the network shown in Fig. 8 is used.

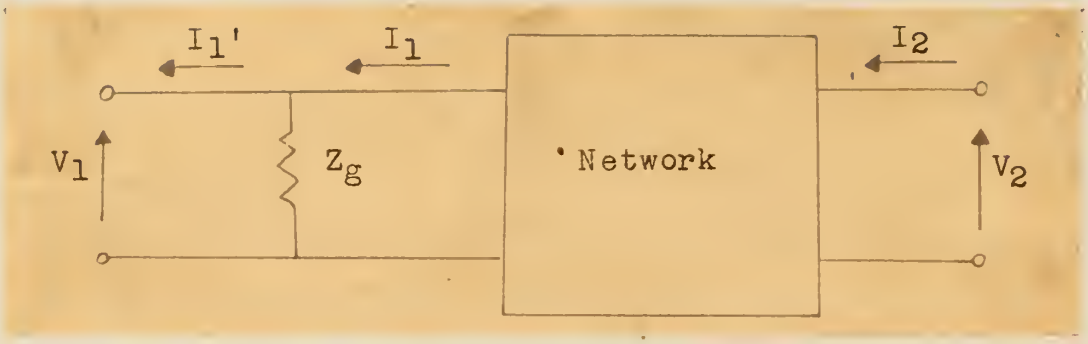

Fig. 8. General four-terminal network with the input terminated by an impedance.

The output impedance can be found by taking the inverse of the transfer matrix for the four-terminal network and applying the same rules that were applied for finding the input impedance. The output impedance is given by

$$Z_o = \frac{DZ_g + B}{CZ_g + A} \tag{24}$$

These relationships will be used to derive the pertinent design equations using the basic equivalent circuit (Fig. 5), arranged in the desired configuration. The equations describing the common emitter configuration are derived in detail to illustrate the method. The equations describing the common collector and common base configurations are stated without proof since the method of deriving them is identical to that of the common emitter case.

Common Emitter Configuration

The transfer matrices will be determined using the loop current method, starting with the common emitter configuration.

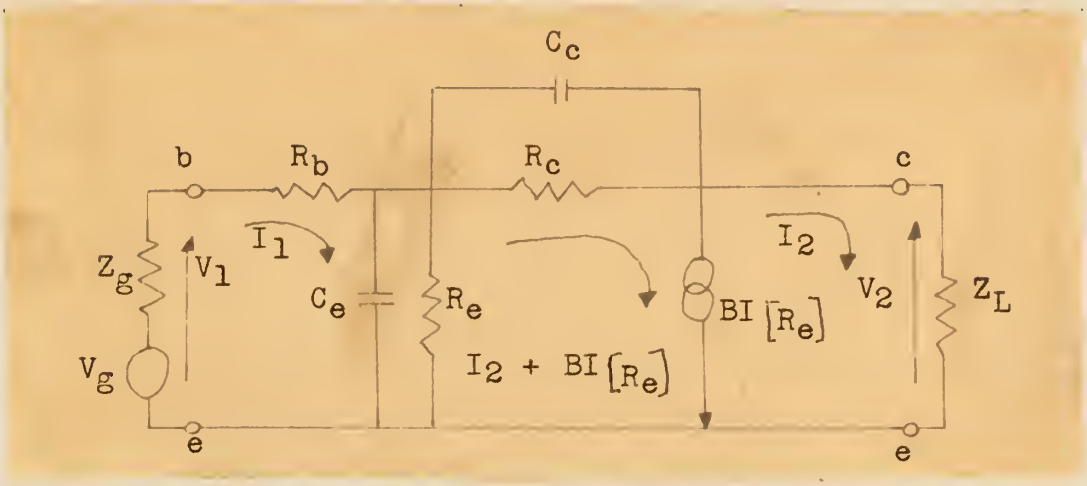

Fig. 9. Hybrid π-equivalent circuit for common emitter configuration.

Referring to Fig. 9 the equation for input voltage V_1 and output voltage V_2 can be written as:

$$V_1 = I_1(R_b + Z_e) - (I_2 + BI[R_e])Z_e \tag{25}$$

$$-V_2 = -I_1(Z_e) + (I_2 + BI[R_e])(Z_e + Z_c) \tag{26}$$

where

$$Z_e = \frac{R_e \frac{1}{PC_e}}{R_e + \frac{1}{PC_e}}, \quad Z_c = \frac{R_c \frac{1}{PC_c}}{R_c + \frac{1}{PC_c}} \tag{27}$$

and $P = jw$.

The current through the resistance R_e is:

$$I[R_e] = (I_1 - [I_2 + BI[R_e]]) \frac{Z_e}{R_e}$$

Solving for $I\left[R_e\right]$ yields

$$I\left[R_e\right] = \frac{Z_e}{R_e + BZ_e} I_1 - \frac{Z_e}{R_e + BZ_e} I_2 \qquad (28)$$

Substituting Eq. (28) into Eqs. (25) and (26) gives new expressions for V_1 and V_2.

$$V_1 = I_1 \left(\frac{R_eR_b + R_eZ_e + BZ_eR_b}{R_e + BZ_e}\right) - I_2 \frac{R_eZ_e}{R_e + BZ_e} \qquad (29)$$

$$-V_2 = I_1 \left(\frac{BZ_eZ_c - Z_eR_e}{R_e + BZ_e}\right) + I_2 \left(\frac{Z_eR_e + Z_cR_e}{BZ_eZ_c - Z_eR_e}\right) \qquad (30)$$

Solving for I_1 in Eq. (30) yields

$$I_1 = -V_2 \left(\frac{R_e + BZ_e}{BZ_eZ_c - Z_eR_e}\right) - I_2 \left(\frac{Z_eR_e + Z_cR_e}{BZ_eZ_c - Z_eR_e}\right) \qquad (31)$$

Substituting Eq. (31) in Eq. (29) and solving for V_1 yields,

$$V_1 = -V_2\left(\frac{R_eR_b+R_eZ_e+BZ_eR_b}{BZ_eZ_c - Z_eR_e}\right) - I_2\left(\frac{R_eZ_eZ_c+R_eZ_eR_b-R_bR_eZ_c}{BZ_eZ_c - Z_eR_e}\right) \qquad (32)$$

The transfer matrix can be written directly from Eqs. (31) and (32).

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} -\frac{R_eR_b+R_eZ_e+BZ_eR_b}{BZ_eZ_c - R_eZ_e} & -\frac{R_eZ_eZ_c+Z_eR_eR_b+Z_cR_bR_e}{BZ_eZ_c - Z_eR_e} \\ -\frac{R_e + BZ_e}{BZ_eZ_c - R_eZ_e} & -\frac{Z_eR_e + Z_cR_e}{BZ_eZ_c - Z_eR_e} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \qquad (33)$$

By comparing the transfer matrix of Eq. (24) with that of the general case given in Eq. (18), the following relationships are evident.

$$A = -\frac{R_eR_b + R_eZ_e + BZ_eR_b}{BZ_eZ_c - R_eZ_e} \qquad (34)$$

$$B = - \frac{R_e Z_e Z_c + Z_e R_e R_b + Z_c R_b R_e}{B Z_e Z_c - R_e Z_e} \tag{35}$$

$$C = - \frac{R_e + B Z_e}{B Z_e Z_c - R_e Z_e} \tag{36}$$

$$D = - \frac{Z_e R_e + Z_c R_e}{B Z_e Z_c - Z_e R_e} \tag{37}$$

The voltage gain for the common emitter configuration is determined by using the relationship given in Eq. (21).

$$K_{ve} = - \frac{Z_L Z_e (B Z_c - R_e)}{\begin{array}{l} R_e Z_e Z_c + R_e Z_e Z_L + B R_b Z_L Z_e + R_e Z_e R_b \\ + R_e R_b Z_c + R_b R_e Z_L \end{array}} \tag{38}$$

The current gain for the common emitter configuration is determined by using Eq. (22).

$$K_{ie} = - \frac{Z_e (B Z_c - R_e)}{R_e (Z_c + Z_L + Z_e) + B Z_L Z_e} \tag{39}$$

The input impedance for the common emitter configuration is determined by using Eq. (23).

$$Z_{in_e} = R_b + \frac{(Z_c + Z_L) Z_e R_e}{R_e Z_e + B Z_L Z_e + R_e Z_c + R_e Z_L} \tag{40}$$

The output impedance for the common emitter configuration is determined by using Eq. (24).

$$Z_{oe} = \frac{(Z_e R_e + Z_c R_e) Z_g + Z_e R_e Z_c + Z_e R_b R_e + Z_c R_b R_e}{Z_g (R_e + B Z_e) + R_e R_b + R_e Z_e + B Z_e R_b} \tag{41}$$

The low-frequency transfer matrix can be determined in a manner equivalent to that of the general case.

The low-frequency common emitter transfer matrix can be determined to be:

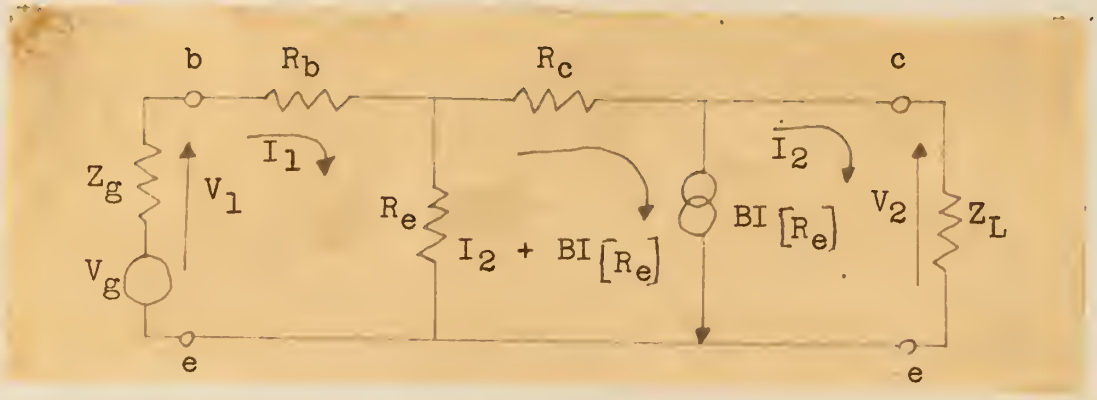

Fig. 10. Hybrid-π low-frequency common emitter equivalent circuit.

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} -\dfrac{(1+B)R_b + R_e}{BR_c - R_e} & -\dfrac{R_eR_b + R_cR_b + R_cR_e}{BR_c - R_e} \\ -\dfrac{1+B}{BR_c - R_e} & -\dfrac{R_e + R_c}{BR_c - R_e} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{42}$$

The voltage gain K_v can be calculated using the relationship given in Eq. (21).

$$K_{ve} = -\frac{R_L(BR_c - R_e)}{R_L([1+B]R_b + R_e) + R_eR_b + R_cR_b + R_cR_e} \tag{43}$$

In the general case $R_c >> R_e$, $B >> 1$.

$$K_{ve} \simeq -\frac{BR_L R_c}{R_L(BR_b + R_e) + R_c(R_e + R_b)}$$

In most practical cases $R_c >> R_L$.

$$K_{ve} \simeq -\frac{BR_L}{R_e + R_b} \tag{44}$$

The current gain K_i can be calculated using the relationship given in Eq. (22).

$$K_{ie} = - \frac{BR_c - R_e}{(1 + B)R_L + R_e + R_c} \tag{45}$$

In all cases $R_c >> R_e$, $B >> 1$. Therefore K_i reduces to

$$K_{ie} \simeq - \frac{BR_c}{BR_L + R_c} \tag{46}$$

The current gain with the output short circuited will be of interest later. Therefore setting R_L equal to zero, the short-circuit current gain can be found to be

$$K_{ie} \simeq -B \quad \text{short-circuit current gain} \tag{47}$$

The low-frequency common emitter input impedance for the equivalent circuit is

$$R_{in_e} = R_b \frac{(R_c + R_L)R_e}{R_e + BR_L + R_c + R_L} \tag{48}$$

As before, $R_c >> R_L$, $R_c >> R_e$.

$$R_{in_e} \simeq R_b + \frac{R_c R_e}{R_c + BR_L} \tag{49}$$

The input impedance with the output short circuited will be of interest later, so setting R_L equal to zero the short-circuit input impedance can be found to be

$$R_{in_e} \simeq R_b + R_e \quad \text{short-circuit input impedance} \tag{50}$$

The low-frequency common emitter output impedance for the equivalent circuit is

$$R_{out\ e} = \frac{(R_e+R_c)R_g+R_eR_c+R_eR_b+R_bR_c}{R_g(1 + B) + R_b(1 + B) + R_e} \tag{51}$$

The output impedance with the input open circuited is

$$R_{out\ e} \simeq \frac{R_e + R_c}{B} \quad \text{open-circuit output impedance} \tag{52}$$

The transfer matrix for the high-frequency common emitter equivalent circuit can be determined using the same method as that used in the general case.

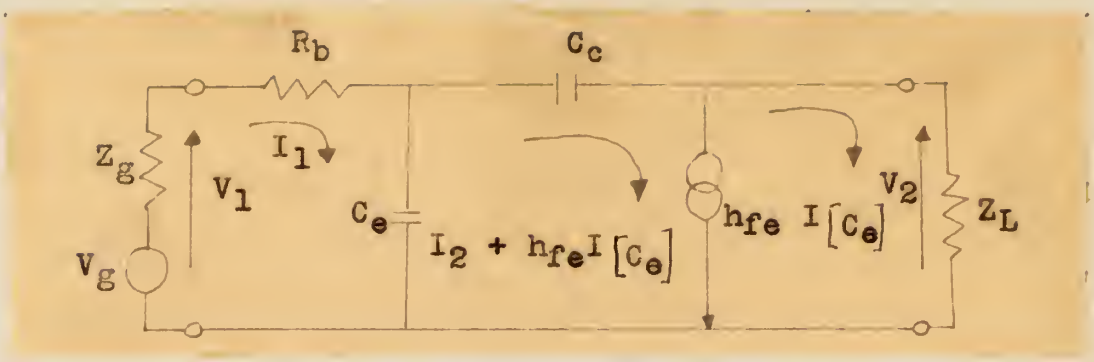

Fig. 11. Hybrid-π high-frequency common emitter equivalent circuit.

This equivalent circuit is useful in the frequency range where $\left|\frac{1}{PC_e}\right| << R_e$ and $\left|\frac{1}{PC_c}\right| << R_c$. Also the parameter, h_{fe}, introduced in Fig. 11 will be defined as $B\frac{Z_e}{R_e}$.

$$h_{fe} = B\frac{Z_e}{R_e} \quad \text{or} \quad B\frac{1}{1 + PC_e R_e} \tag{53}$$

The transfer matrix for the high-frequency equivalent circuit is

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} -\frac{(1+h_{fe})R_b+X_e}{h_{fe}X_c - X_e} & -\frac{X_eR_b+X_cR_b+X_cX_e}{h_{fe}X_c - X_e} \\ -\frac{h_{fe}}{h_{fe}X_c - X_e} & -\frac{X_e + Y_c}{h_{fe}X_c - X_e} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{54}$$

In practically all cases of interest $X_c >> X_e$, where $X_c = \frac{1}{PC_c}$ and $X_e = \frac{1}{PC_e}$. Using this approximation the voltage gain, K_v, current gain K , input impedance Z_{in}, and output impedance

Z_{out} are as follows:

$$K_{ve} = - \frac{h_{fe} X_c Z_L}{(\left[1 + h_{fe}\right]R_b + X_e)Z_L + (R_b + X_e)X_c} \tag{55}$$

$$K_{ie} = - \frac{h_{fe} X_c}{(1 + h_{fe})Z_L + X_c} \tag{56}$$

$$Z_{ine} = R_b + \frac{(X_c + Z_L)X_e}{X_c + Z_L(1 + h_{fe})} \tag{57}$$

$$Z_{out\ e} = \frac{X_c Z_g + X_c(X_e + R_b)}{(1 + h_{fe})Z_g + (1 + h_{fe})R_b + X_e} \tag{58}$$

The output impedance with the input open circuited will be of interest later.

$$Z_{out\ e} \simeq \frac{X_c}{1 + h_{fe}} \quad \text{output impedance with input open circuited} \tag{59}$$

Common Collector Configuration

Figure 12 is the equivalent circuit in the common collector configuration. The transfer matrix and the equations of interest will be stated without proof since the method of determining these is identical with that used for the common emitter case.

Common collector transfer matrix:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} \frac{R_b + Z_c}{Z_c} & \frac{R_e(Z_c + Z_e)}{Z_c(R_e + BZ_e)} \\ \frac{1}{Z_c} & \frac{R_e(Z_c + Z_e)(R_b + Z_e) - Z_c^2 R_e}{Z_c(R_e + BZ_e)} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{60}$$

Common collector voltage gain:

$$K_{vc} = \frac{Z_L Z_c (R_e + BZ_e)}{(R_b+Z_c)(R_e+BZ_e)Z_L + R_e(Z_c R_b + Z_e R_b + Z_c Z_e)} \tag{61}$$

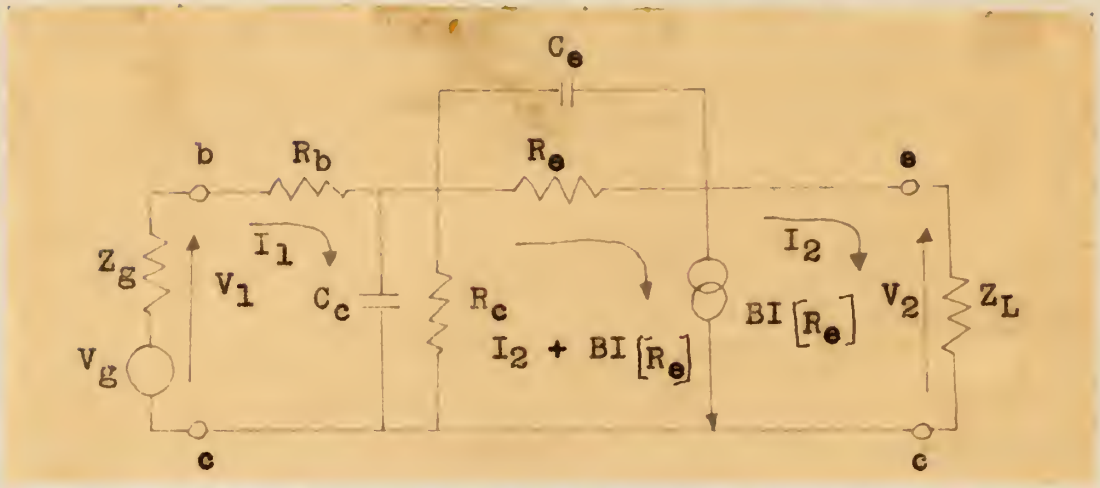

Fig. 12. Hybrid-π equivalent circuit for the common collector configuration.

Common collector current gain:

$$K_{ie} = \frac{Z_c(BZ_e + R_e)}{BZ_e Z_L + R_e(Z_c + Z_e + Z_L)} \tag{62}$$

Common collector input impedance:

$$Z_{in_c} = R_b + \frac{Z_L Z_c (R_e + BZ_e) + Z_c Z_e R_e}{Z_c R_e + Z_e R_e + Z_L(R_e + BZ_e)} \tag{63}$$

Common collector output impedance:

$$Z_{out_c} = \frac{(Z_c\left[Z_g + R_b\right] + Z_e\left[Z_g + Z_e + Z_c\right])R_e}{(Z_g + R_b + Z_e)(R_e + BZ_e)} \tag{64}$$

Low-frequency common collector transfer matrix:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} \frac{R_b + R_c}{R_c} & \frac{R_e(R_b + R_c) + R_c R_b}{R_c(1 + B)} \\ \frac{1}{R_c} & \frac{R_c + R_e}{R_c(1 + B)} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{65}$$

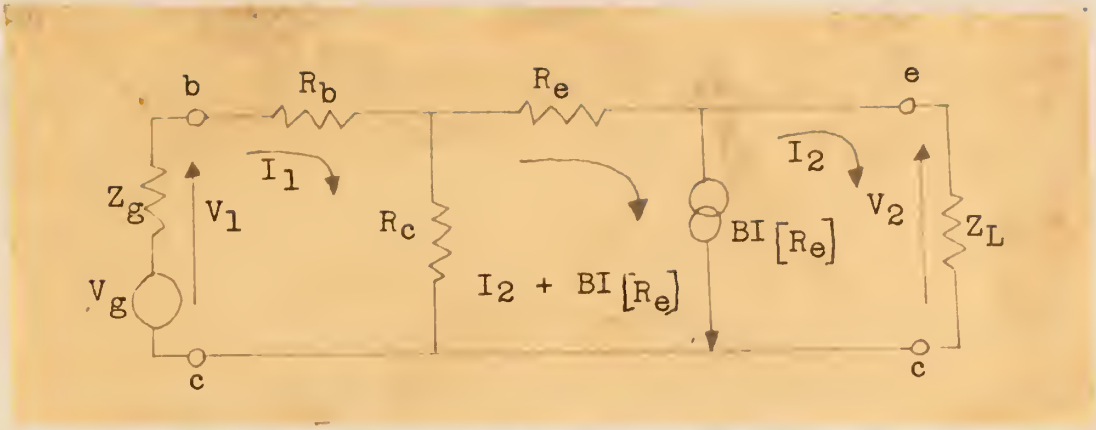

Fig. 13. Hybrid-π low-frequency common collector equivalent circuit.

Low-frequency common collector voltage gain:

$$K_{vc} = \frac{R_L R_c (1 + B)}{(R_b + R_c)(1 + B)R_L + R_c R_b + R_e R_b + R_c R_e} \tag{66}$$

Using the valid approximations that $R_c >> R_e$, $R_L >> R_e$ and $B >> 1$.

$$K_{vc} \simeq 1 \tag{67}$$

Low-frequency common collector current gain:

$$K_{ic} = \frac{R_c (1 + B)}{BR_L + R_c + R_e + R_L} \tag{68}$$

Using the approximations that $R_c >> R_e$ and $B >> 1$:

$$K_{ic} \simeq \frac{BR_c}{BR_L + R_c} \tag{69}$$

Low-frequency common collector input impedance:

$$R_{in_c} = R_b + \frac{R_L R_c (1 + B) + R_c R_e}{R_c + R_e + (1 + B)R_L} \tag{70}$$

Using the approximations that $B >> 1$, $R_L >> R_e$, and $R_c >> R_e$:

$$R_{in_c} \simeq R_b + \frac{(R_e + BR_L)R_c}{R_c + BR_L} \tag{71}$$

Low-frequency common collector output impedance:

$$R_{out_c} = \frac{R_c(R_g + R_b) + R_e(R_g + R_e + R_c)}{(R_g + R_b + R_c)(1 + B)} \tag{72}$$

Using the approximations that $R_c >> R_e$, $R_c >> R_b$, $R_c >> R_g$, $R_g >> R_b$, and $B >> 1$:

$$R_{out_c} \simeq \frac{R_g + R_2}{B} \tag{73}$$

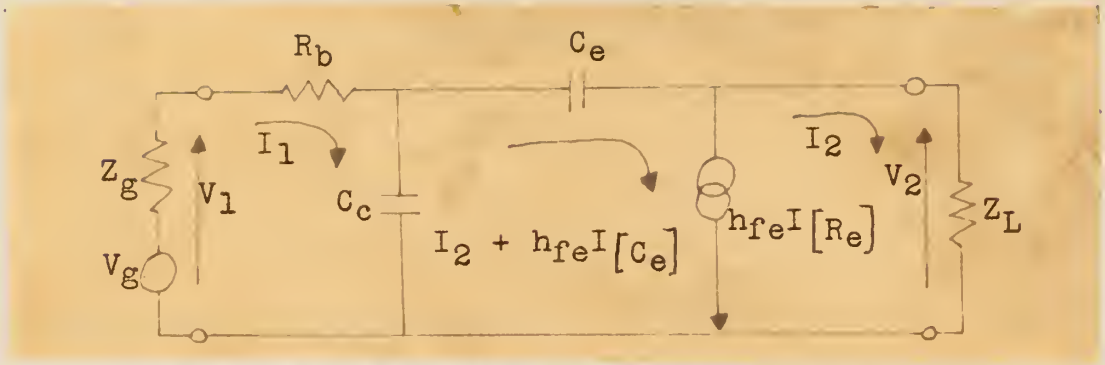

Fig. 14. Hybrid-π high-frequency common collector equivalent circuit.

High-frequency common collector transfer matrix:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} \frac{R_b + X_c}{X_c} & \frac{X_e(R_b + X_c) + X_cR_b}{X_c(1 + h_{fe})} \\ \frac{1}{X_c} & \frac{X_c + X_e}{X_c(1 + h_{fe})} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{74}$$

High-frequency common collector voltage gain:

$$K_{vc} = \frac{Z_LX_c(1 + h_{fe})}{(R_b+X_c)(1+h_{fe})Z_L + X_cR_b+X_eR_b+ X_cX_e} \tag{75}$$

using the approximations that $X_c >> R_b$, $X_c >> X_e$, and $(1 + h_{fe})Z_L >> (R_b + X_e)$.

$$K_{vc} \simeq 1 \tag{76}$$

High-frequency common collector current gain:

$$K_{ic} = \frac{X_c(1 + h_{fe})}{h_{fe}Z_L + X_c + X_e + Z_L} \tag{77}$$

Using the approximation that $X_c >> X_e$:

$$K_{ic} \simeq \frac{X_c(1 + h_{fe})}{X_c + Z_L(1 + h_{fe})} \tag{78}$$

High-frequency common collector input impedance:

$$Z_{in_c} = R_b + \frac{Z_L X_c(1 + h_{fe}) + X_c X_e}{X_c + X_e + Z_L(1 + h_{fe})} \tag{79}$$

Using the approximations that $X_c >> X_e$, $Z_L >> X_e$:

$$Z_{in_c} \simeq R_b + \frac{Z_L X_c(1 + h_{fe})}{X_c + Z_L(1 + h_{fe})} \tag{80}$$

High-frequency common collector output impedance:

$$Z_{out_c} = \frac{X_c(Z_g + R_b) + X_e(Z_g + X_e + X_c)}{(Z_g + R_b + X_c)(1 + h_{fe})} \tag{81}$$

Using the approximations that $X_c >> X_e$, $Z_g >> R_b$, and $X_c >> Z_g$.

$$Z_{out_c} \simeq \frac{Z_g + X_e}{1 + h_{fe}} \tag{82}$$

Common Base Configuration

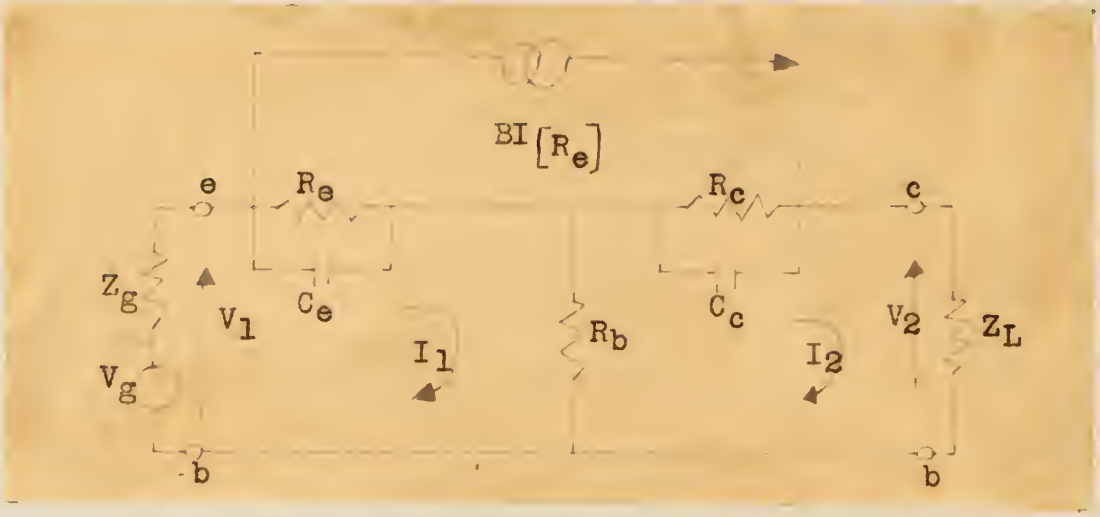

Fig. 15. Hybrid-π equivalent circuit for the common base configuration.

Transfer matrix for the common base configuration:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} \dfrac{R_e(Z_e+R_b)+BZ_eR_b}{BZ_eZ_c+R_b(R_e+BZ_e)} & \dfrac{R_bR_eZ_e+Z_cZ_eR_e+Z_cR_bR_e}{BZ_eZ_c+R_b(R_e+BZ_e)} \\ \dfrac{R_e+BZ_e}{BZ_eZ_c+R_b(R_e+BZ_e)} & \dfrac{(R_b+Z_c)(R_e+BZ_e)}{BZ_eZ_c+R_b(R_e+BZ_e)} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{83}$$

Common base voltage gain:

$$K_{vb} = \frac{Z_L(BZ_eZ_c + R_b[R_e + BZ_e])}{Z_L(R_e[Z_e+R_b]+BZ_eR_b)+R_bR_eZ_e+Z_cZ_eR_e+Z_cR_bR_e} \tag{84}$$

Common base current gain:

$$K_{ib} = \frac{B(Z_eZ_c + Z_eR_b) + R_bR_e}{(Z_L + Z_c + R_b)(BZ_e + R_e)} \tag{85}$$

Common base input impedance:

$$Z_{in_b} = \frac{R_b(Z_L R_e + Z_c R_e + BZ_e Z_L) + Z_e R_e (Z_L + Z_c + R_b)}{(Z_L + Z_c + R_b)(R_e + BZ_e)} \tag{86}$$

Common base output impedance:

$$Z_{out_b} = \frac{Z_c(BZ_e Z_g + Z_g R_e + Z_e R_e + R_b R_e) + BZ_e Z_g R_b + Z_g R_b R_e + Z_e R_b R_e}{BZ_e R_b + BZ_e Z_g + Z_g R_e + Z_e R_e + R_e R_b} \tag{87}$$

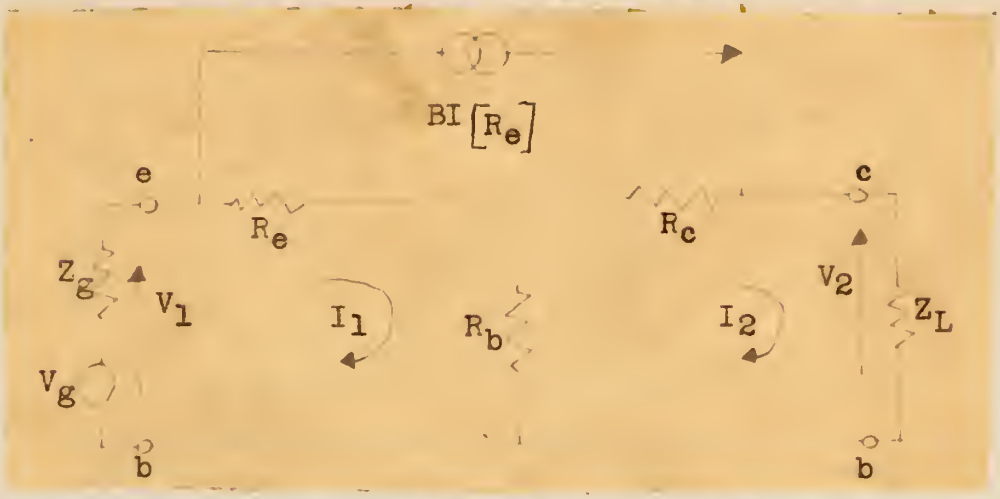

Fig. 16. Hybrid-π low-frequency common base equivalent circuit.

Low-frequency common base voltage gain:

$$K_{vb} = \frac{R_L(BR_c + R_b[1 + B])}{R_L([R_e + R_b] + BR_b) + R_b R_e + R_c R_e + R_c R_b} \tag{88}$$

Using the approximations that $R_c >> R_b$, $R_c >> R_L$

$$K_{vb} \simeq \frac{BR_L}{R_e + R_b} \tag{89}$$

Low-frequency common base current gain:

$$K_{ib} = \frac{B(R_c + R_b) + R_b}{(R_L + R_c + R_b)(1 + B)} \tag{90}$$

Using the approximations that $R_c >> R_b$, $R_c >> R_L$, and $B >> 1$:

$$K_{ib} \simeq 1 \tag{91}$$

The current gain with the output short circuited is:

$$K_{ib} = \frac{B}{1 + B} \quad \text{short-circuit current gain} \tag{92}$$

Low-frequency common base input impedance:

$$R_{in_b} = \frac{R_b(R_L+R_c+BR_L) + R_e(R_L+R_c+R_b)}{(R_L + R_c + R_b)(1 + B)} \tag{93}$$

Using the approximations that $R_c >> R_L$, $R_e >> R_b$, $R_L >> R_b$, and $B >> 1$:

$$R_{in_b} \simeq \frac{R_e + R_b}{B} \tag{94}$$

This is also the approximate input impedance with the output short circuited which will be of use later.

Low-frequency common base output impedance:

$$R_{out_b} = \frac{R_c(BR_g+R_g+ R_e+R_b)+BR_gR_b+R_gR_b+R_bR_e}{B(R_g + R_b) + R_g + R_e + R_b} \tag{95}$$

Using the approximations that $R_g >> R_b$, $R_c >> R_e$, $R_c >> R_b$, and $B >> 1$:

$$R_{out_b} = \frac{R_c(BR_g + R_e)}{BR_g + R_e} = R_c \tag{96}$$

The low-frequency output impedance with the input open-circuited will be of interest later; this is

$$R_{out_b} = R_c \quad \text{open-circuit current gain} \tag{97}$$

High-frequency common base transfer matrix:

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} \frac{X_e+(1+h_{fe})R_b}{h_{fe}X_c+(1+h_{fe})R_b} & \frac{X_eR_b+X_cX_e+X_cR_b}{h_{fe}X_c+(1+h_{fe})R_b} \\ \frac{1 + h_{fe}}{h_{fe}X_c+(1+h_{fe})R_b} & \frac{(R_b+X_c)(1+h_{fe})}{h_{fe}X_c+(1+h_{fe})R_b} \end{vmatrix} \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \tag{98}$$

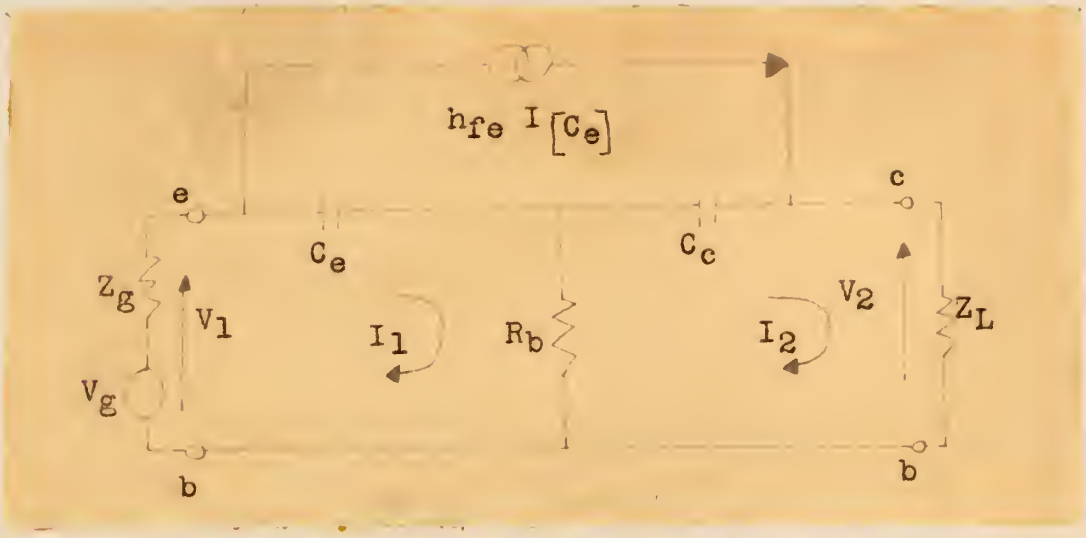

Fig. 17. Hybrid-π common base high-frequency equivalent circuit.

High-frequency common base voltage gain:

$$K_{vb} = \frac{Z_L(h_{fe}X_c+R_b[1+h_{fe}])}{Z_L(X_e+R_b+h_{fe}R_b)+R_bX_e+X_cX_e+X_cR_b} \tag{99}$$

Using the approximations that $X_c >> R_b$ and $X_c >> X_e$:

$$K_{vb} \simeq \frac{h_{fe}X_cZ_L}{Z_L(X_e + R_b[h_{fe} + 1]) + X_c(R_b + X_e)} \tag{100}$$

High-frequency common base current gain:

$$K_{ib} = \frac{h_{fe}(X_c + R_b) + R_b}{(Z_L + X_c + R_b)(1 + h_{fe})} \tag{101}$$

Using the approximation that $X_c >> R_b$:

$$K_{ib} \simeq \frac{h_{fe}X_c}{(Z_L + X_c)(1 + h_{fe})} \tag{102}$$

High-frequency common base input impedance:

$$Z_{in_b} = \frac{R_b(Z_L+X_c+h_{fe}Z_L) + X_e(Z_L+X_c+R_b)}{(Z_L + X_c)(1 + h_{fe})} \tag{103}$$

Using the approximation that $X_c >> R_b$:

$$Z_{in_b} \simeq \frac{R_b(Z_L[1 + h_{fe}] + X_c) + X_e(Z_L + X_c)}{(Z_L + X_c)(1 + h_{fe})} \qquad (104)$$

The input impedance at very high frequencies with the output short-circuited will be of interest later; this is

$$Z_{in_b} \simeq R_b \quad \text{short-circuit input impedance} \qquad (105)$$

High-frequency common base output impedance:

$$Z_{out_b} = \frac{Z_g(h_{fe}X_c+X_c+h_{fe}R_b+R_b)+X_cX_e+X_eR_b+X_cR_b}{Z_g(h_{fe} + 1) + X_eR_b(1 + h_{fe})} \qquad (106)$$

The output impedance with the input open-circuited will be of interest later; this is

$$Z_{out_b} \simeq X_c + R_b \quad \text{open-circuit output impedance} \qquad (107)$$

Definitions of Transistor Parameters

The equivalent circuits having been established, it is now necessary to determine the parameters from the manufacturer's data sheet. Listed below are the parameters usually given on a typical data sheet. In many cases some of the important parameters are missing but usually they can be estimated by utilizing some of the relationships thus far developed.

The configuration of the transistor that the parameter represents is denoted by subscripts. For example, h_{fe} is the common emitter forward current transfer ratio with the output ac short-circuited, while h_{fb} is the identical parameter for the common base configuration.

Small Signal and High-frequency Parameters

h_{ob} -- Common base - output admittance, input ac open-circuited.

h_{oe} -- Common emitter - output admittance, input ac open-circuited.

h_{ib} -- Common base - input impedance, output ac short-circuited.

h_{ie} -- Common emitter - input impedance, output ac short-circuited.

h_{rb} -- Common base - reverse voltage transfer ratio, input ac open-circuited.

h_{fb} -- Common base -forward current transfer ratio, output ac short-circuited.

h_{fe} -- Common emitter - forward current transfer ratio, output ac short-circuited.

h_{fc} -- Common collector - forward current transfer ratio, output ac short-circuited.

$f_{\alpha b}$ - Common base - the frequency at which the magnitude of the small signal short-circuit forward current transfer ratio is 0.707 of its low-frequency value.

$f_{\alpha e}$ - Common emitter - the frequency at which the magnitude of the small signal short-circuit forward current transfer ratio is 0.707 of its low-frequency value.

f_{max} - Maximum frequency of oscillation.

C_{ob} -- Collector to base - capacitance measured across

the output terminals with the input ac open-circuited.

C_{oe} -- Collector to emitter - capacitance measured across the output terminals with the input ac open-circuited.

r'_b -- Base spreading resistance.

NF -- Noise figure.

Z_1 -- Input impedance.

Z_o -- Output impedance.

T_q -- Operation temperature.

T_j -- Junction temperature.

T_{stg} - Storage temperature.

Direct-current Measurements

I_C, I_E, I_B - Direct currents into collector, emitter, or base terminal.

V_{CB}, V_{EB} - Voltage collector to base, or emitter to base.

V_{CE} -- Voltage collector to emitter.

V_{BE} -- Voltage base to emitter.

BV_{CBO} - Breakdown voltage, collector to base junction reverse biased, emitter open-circuited (value of I_c should be specified).

V_{CEO} - Voltage collector to emitter, at zero base current, with the collector junction reverse biased. Specify I_c.

BV_{CEO} - Breakdown voltage, collector to emitter, with base open-circuited. This may be a

function of both "m" (the charge carrier multiplication factor) and the h_{fb} of the transistor. Specify I_c.

I_{EO}, I_{EBO} - Emitter current when emitter junction is reverse biased and collector is dc open-circuited.

I_{CEO} - Collector current with collector junction reverse biased and base open-circuited.

I_{CES} - Collector current with collector junction reverse biased and base shorted to emitter.

I_{ECS} - Emitter current with emitter junction reverse biased and base shorted to collector.

R_{SC} -- Collector saturation resistance.

I_{CO}, I_{CBO} - Collector current when collector junction is reverse biased and emitter is dc open-circuited.

h_{FE} -- Common emitter direct-current transfer ratio, output short-circuited.

h_{FB} -- Common base direct-current transfer ratio, output short-circuited.

The methods of determining the equivalent circuit parameters from the data given on the manufacturer's data sheets are listed below.

Determination of B

Case 1. h_{fe} given. h_{fe} was defined as the forward current transfer ratio with the output ac short-circuited. This parameter

is usually specified by the manufacturer at a frequency well below the common emitter cut-off frequency. Referring to Eq. (47), it follows that $B \simeq h_{fe}$ if h_{fe} is specified as being measured below the common emitter cut-off frequency $f_{\alpha e}$. In terms of the static characteristics h_{fe} is defined as

$$h_{fe} = \left.\frac{\partial I_C}{\partial I_B}\right|_{V_c=C} = \underset{\Delta \to 0}{\text{limit}} \frac{\Delta I_C}{\Delta I_B}$$

where I_C, I_B, and V_c are the direct-current values of the collector current, base current, and collector voltage respectively.

Case 2. h_{FE} given. h_{FE} was defined as the direct-current transfer ratio with the output short-circuited. There is little difference between h_{fe} and h_{FE} if h_{fe} is specified at a frequency well below its cut-off frequency $f_{\alpha e}$. This can be substantiated by comparing the values of h_{fe} and h_{FE} on data sheets that give both parameters.[1] For making calculations to the first approximation, the following relationships are valid.

$$B \simeq h_{FE} \quad \text{and} \quad h_{FE} \simeq h_{fe}$$

Case 3. α_{ce} or h_{fb} given. Referring to Eqs.(12) and (92), B can be calculated using the relationship

$$B = \frac{\alpha_{ce}}{1 - \alpha_{ce}}$$

where $\alpha_{ce} = h_{fb}$. The above relationship is true if h_{fb} or α_{ce} is specified at a frequency well below the common base cut-off frequency $f_{\alpha b}$.

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[1] General Electric Transistor Manual, 3rd ed., General Electric Co., Semiconductor Products, 1224 W. Genesee St., Syracuse, New York, 1958.

Determination of R_e

R_e can be estimated using the relationship $R_e = \frac{B26}{I_E \text{ in ma}}$ in all practical cases of interest.

Determination of R_b

Case 1. R_b is approximately equal to r_b so if r_b is given, R_b can be taken directly from the data sheet.

Case 2. r_b not given, but h_{ie} given. In practically all cases the frequency at which h_{ie} is measured is so low that the low-frequency equivalent circuit applies. Referring to Eq. (50), the equation for determining R_b can be derived.

$$R_b \simeq h_{ie} - \frac{B26}{I_E \text{ in ma}}$$

where I_E in ma indicates the d-c emitter bias current in milliamperes. The value of the d-c bias conditions for which any parameter is specified is usually given on the manufacturer's data sheet, and is used in the calculation of R_b.

Case 3. r_b not given, but h_{ib} given. Referring to Eq. (94), the equation for determining R_b can be derived.

$$R_b \simeq B \left(h_{ib} - \frac{26}{I_E \text{ in ma}}\right)$$

Determination of C_e

This parameter can be determined knowing R_e and $f_{\alpha e}$ of $f_{\alpha b}$.

There is a fundamental relationship existing between $f_{\alpha e}$ and $f_{\alpha b}$, this being $f_{\alpha e} = \frac{f_{\alpha b}}{B + 1}$, or $f_{\alpha e} \simeq \frac{f_{\alpha b}}{B}$. This relationship can be derived from the equations for the common emitter current gain and the common base current gain. Equation (39) gives for the common emitter current gain

$$K_{ie} = - \frac{Z_e(BZ_c - R_e)}{R_e(Z_c + Z_L + Z_e) + BZ_LZ_e}$$

The expression with the output short circuited is of interest, and also at $f_{\alpha e}$ $Z_c >> Z_e$ and $Z_c >> R_e$; therefore $K_{ie} \simeq - \frac{BZ_e}{R_e}$. Similarly for the common base case, simplifying Eq. (85) for the output short circuited yields $K_{ib} \simeq \frac{BZ_e}{BZ_e + R_e}$. Rewriting these equations in an alternate form and using the equivalent parameters listed under Definitions of Transistor Parameters, it follows that $h_{fe} = \frac{B}{1 + j\omega C_eR_e}$. The frequency at which h_{fe} is 0.707 of its value at low frequencies is defined as $f_{\alpha e}$; therefore $\left|X_{ce}\right| = R_e$ at $f_{\alpha e}$ or $f_{\alpha e} = \frac{1}{2\pi C_eR_e}$. The equivalent expressions for the common base case are

$h_{fb} = \frac{1}{1 + B\ j\omega\ C_eR_e}$ and $f_{\alpha b} = \frac{1}{2\pi\ B\ C_eR_e}$. From this it is obvious that $f_{\alpha e} \simeq \frac{f_{\alpha b}}{B}$ for the equivalent circuits developed. The equations for finding C_e are therefore $C_e = \frac{1}{2\pi\ f_{\alpha e}R_e}$ or $C_e = \frac{B}{2\pi\ f_{\alpha b}R_e}$.

Determination of C_c

C_c can be estimated from the value given for C_{ob}. The data

given for C_{ob} on the manufacturer's data sheet is a direct indication of the value of C_c, (refer to Eq. (107)). C_{ob} is a measured parameter and it includes some extrinsic capacitance, so C_{ob} is always greater than C_c. As an approximation C_c can be estimated to be $1\mu\mu F_d$ less than the value given for C_{ob}.

Determination of R_c

R_c can be approximated when h_{oe} or h_{ob} is given on the data sheet.

Case 1. h_{oe} given. Referring to Eq. (52), the equation for the common emitter output impedance with the input open circuited was found to be $R_{out\ c} = \frac{R_e + R_c}{B}$ which is equal to $\frac{1}{h_{oe}}$ in this case. Using the relationships already developed, the equation for R_c can be determined to be

$$R_c = \frac{B}{h_{oe}} - \frac{B26}{I_E \text{ in ma}} \quad \text{or} \quad R_c \simeq \frac{B}{h_{oe}}$$

since $\frac{B}{h_{oe}} >> \frac{B26}{I_E \text{ in ma}}$ in all cases.

Case 2. h_{ob} given. Using the same procedure as used above with reference to Eq. (97), R_c can be found to be $R_c \simeq \frac{1}{h_{ob}}$.

Determination of h_{fe}

This parameter is equivalent to the one given on the data sheet. The problem is to determine its value at the frequency of interest. One method is to use the expression $h_{fe} \simeq B \frac{Z_e}{R_e}$

where Z_e can be determined at the frequency of interest. Another method of determining h_{fe} is to use the approximation that h_{fe} decreases at a rate of approximately 6 db per octave from its value at $f_{\alpha e}$.

Table of Equivalent Circuit Parameters

Table 1 is a tabulation of the parameters that constitute the equivalent circuit and formulas useful in approximating these parameters from the manufacturer's data sheet.

Table 1. Approximate relationships between equivalent circuit parameters and parameters on manufacturer's data sheet.

Equivalent circuit parameter	Equations for calculating			
	Direct equivalent	Common base	Common emitter	Direct calculation
B		$\alpha/1-\alpha$	h_{FE}	
R_b	r_b	$B(h_{ib} - \frac{26}{I_E(ma)})$	$h_{ie} - \frac{B26}{I_E(ma)}$	
R_e				$B26/I_E(ma)$
C_e		$\frac{B}{w_{\alpha b} R_e}$	$1/w_{\alpha e} R_e$	
C_c	C_{ob}	C_{ob}		
R_c		$1/h_{ob}$	B/h_{oe}	
h_{fe}				$B \frac{Z_e}{R_e}$

NEGATIVE FEEDBACK

Negative feedback is of use in the design of transistor amplifiers to improve the following characteristics:

1. Frequency response
    a. In the design of wide-band amplifiers negative feedback is of use in trading gain for bandwidth.
2. Variation in gain due to variation in transistor parameters.
3. Distortion.

There are two basic forms of feedback which will be discussed here--voltage (shunt) feedback and current (series) feedback.

Voltage Feedback

The method of analysis will be to determine a constant voltage form of an equivalent circuit for the amplifier without feedback and then to modify this equivalent circuit by adding the feedback circuit to determine the desired design equations. The common emitter amplifier configuration will be used as the basic circuit for the analysis.

Figure 18 shows the basic common emitter amplifier stage with the biasing network not shown.

Figure 19 shows the constant voltage form of equivalent circuit for the common emitter stage.

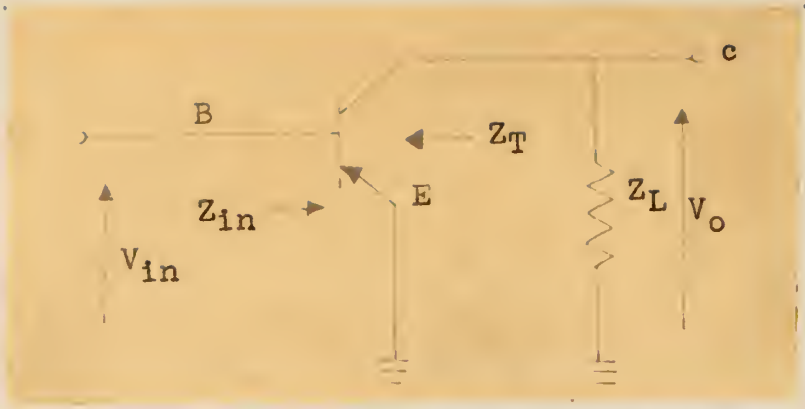

Fig. 18. Common emitter amplifier stage.

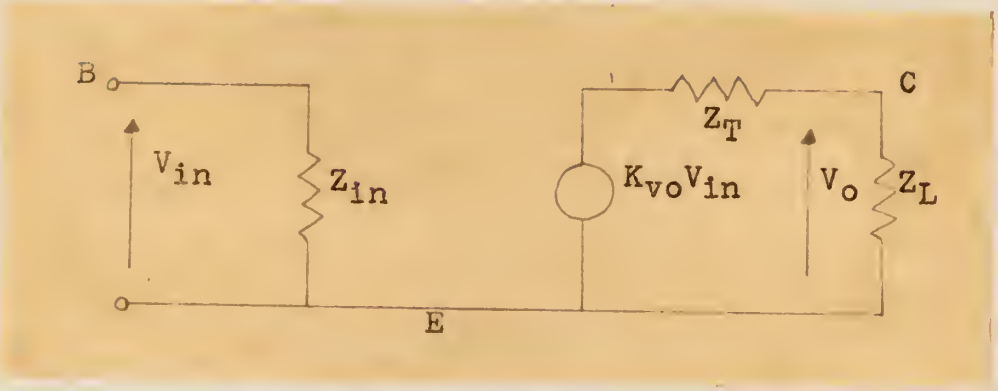

Fig. 19. Constant voltage form of equivalent circuit for the common emitter amplifier stage.

In Fig. 19:

K_{vo} = voltage gain with load open circuited

Z_T = output terminal impedance with input short circuited

Z_{in} = input impedance

B, C, E = the base, collector, and emitter terminals respectively.

The open-circuit voltage gain can be found for the general case by referring to Fig. 6 and Eq. (16), and letting $I_2 = 0$.

$$V_2/V_1 = 1/A \tag{108}$$

Therefore in Fig. 19

$$K_{vo} = 1/A \tag{109}$$

In terms of the common emitter equivalent circuit previously developed, Eq. (34), A is

$$A = - \frac{R_e R_b + R_e Z_e + B Z_e R_b}{B Z_e Z_c - R_e Z_e} \tag{110}$$

Therefore the open-circuit voltage gain is

$$K_{vo} = - \frac{B Z_e Z_c - R_e Z_e}{R_e R_b + R_e Z_e + B Z_e R_b} \tag{111}$$

Z_T can be found by using Eq. (24), by letting $Z_g = 0$ (input short circuited).

$$Z_T = \frac{B}{A} = \frac{Z_e R_e Z_c + Z_e R_b R_e + Z_c R_b R_e}{R_e R_b + R_e Z_e + B Z_e R_b} \tag{112}$$

From Fig. 19 the equation for the voltage gain can be written as

$$K_{ve} = - \frac{1}{A} \frac{Z_L}{Z_L + Z_T} \tag{113}$$

Substituting Eqs. (110) and (112) into Eq. (113) yields the previously derived Eq. (38) for the common emitter voltage gain.

From Eq. (40), the input impedance without feedback is

$$Z_{in_e} = R_b + \frac{(Z_c + Z_L) Z_e R_e}{R_e Z_e + B Z_L Z_e + R_e Z_c + R_e Z_L} \tag{114}$$

The voltage gain with feedback will now be determined. Figure 20 is the common emitter amplifier with voltage feedback.

From Fig. 21, using Millman's theorem and solving for V_{in}, yields

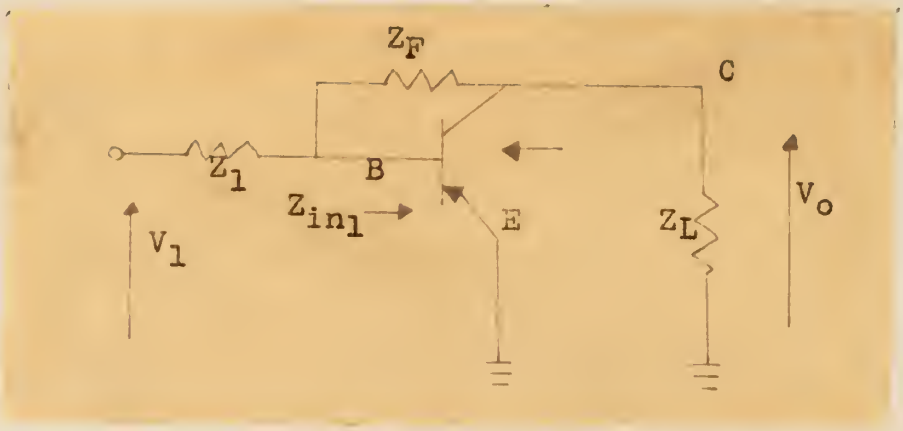

Fig. 20. Common emitter amplifier with voltage feedback.

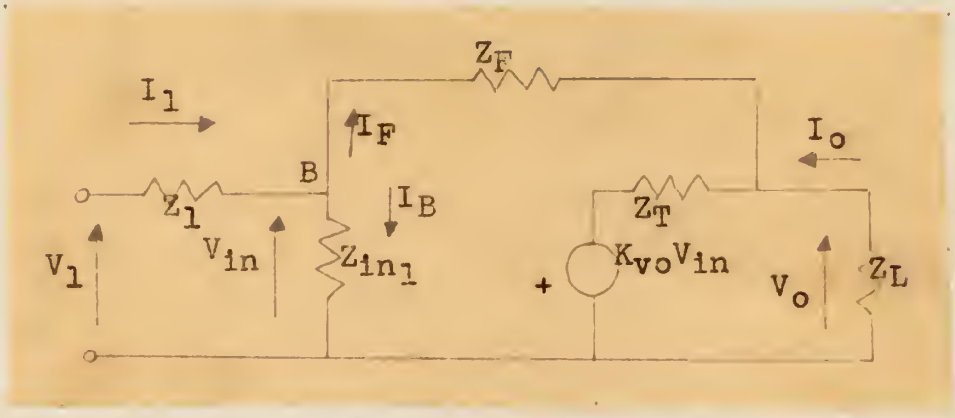

Fig. 21. Equivalent circuit of amplifier stage with feedback.

$$V_{in} = \frac{\frac{V_1}{Z_1} + \frac{V_o}{Z_F}}{\frac{1}{Z_{in_1}} + \frac{1}{Z_1} + \frac{1}{Z_F}} \qquad (115)$$

where Z_{in_1} is the modified input impedance as described in Eq. (121).

Using the approximation that $Z_F >> Z_{in_1}$, which is true in all practical cases, and solving for V_o in terms of $K_{vo}V_{in}$, yields

$$V_o \simeq - \frac{\dfrac{Z_L\, Z_F}{Z_L + Z_F}}{Z_o + \dfrac{Z_L Z_F}{Z_o + Z_F}} K_{vo}\, V_{in} \tag{116}$$

Letting

$$Z_x = \frac{Z_L\, Z_F}{Z_L + Z_F} \tag{117}$$

Eq. (116) can be written

$$V_o \simeq - \frac{Z_x}{Z_x + Z_o} K_{vo}\, V_{in} \tag{118}$$

Solving for $\frac{V_o}{V_{in}}$, replacing K_{vo} with $\frac{1}{A}$, yields

$$K_{ve_1} \simeq - \frac{V_o}{V_{in}} = - \frac{Z_x}{Z_x + Z_o} \frac{1}{A} \tag{119}$$

Equation (119) is approximately equal to Eq. (113) if Z_L is replaced by Z_x, so the voltage gain from base to collector with feedback is approximately given by Eq. (38) if Z_L is replaced by Z_x and $Z_F >> Z_{in_1}$.

$$K_{ve_1} \simeq - \frac{Z_x Z_e (BZ_c - R_e)}{R_e Z_e Z_c + R_e Z_e Z_x + BR_b Z_x Z_e + R_e Z_e R_b + R_e R_b Z_c + R_b R_e Z_x} \tag{120}$$

Using the same argument stated above, Z_{in_1} in Fig. 21 is approximately equal to Z_{in_E} defined by Eq. (40), if Z_L in Eq. (40) is replaced by Z_x defined in Eq. (117).

$$Z_{in_1} \simeq R_b + \frac{(Z_c + Z_x) Z_e R_e}{R_e Z_e + BZ_x Z_e + R_e Z_c + R_e Z_x} \tag{121}$$

From Eq. (119)

$$V_{in} \simeq - \frac{V_o}{K_{ve_1}} \quad \text{or} \quad V_o \simeq - V_{in} K_{ve_1} \tag{122}$$

Substituting Eq. (120) into Eq. (115) and solving for V_o/V_1, which is the voltage gain with feedback, yields:

$$K_{vF} = \frac{V_o}{V_1} \simeq - \frac{Z_F}{Z_g} \left(\frac{1}{\frac{1}{K_{ve_1}} \left(\frac{Z_F}{Z_g} + \frac{Z_F}{Z_{in_1}} + 1 \right) + 1} \right) \tag{123}$$

If K_{ve_1} is sufficiently large,

$$K_{vF} \simeq - \frac{Z_F}{Z_1} \tag{124}$$

Derivation of input impedance with feedback:

$$Z_{in_F} = Z_1 + \frac{V_{in}}{I_1} \tag{125}$$

$$I_1 = I_B + I_F \tag{126}$$

$$I_B = \frac{V_{in}}{Z_{in_1}} \tag{127}$$

$$I_F = \frac{V_{in} - V_o}{Z_F} \tag{128}$$

Substituting Eq. (122) into Eq. (128) gives

$$I_F \simeq \frac{V_{in} + K_{ve_1} V_{in}}{Z_F} \tag{129}$$

Substituting Eqs. (127) and (128) into Eq. (125) and solving for input impedance with feedback, yields:

$$Z_{inF} \simeq Z_1 + \frac{1}{\frac{1}{Z_{in_1}} + \frac{1}{Z_F} (1 + K_{ve_1})} \tag{130}$$

Derivation of current gain:

From Eqs. (126), (127), and (128) the input current is

$$I_1 = I_B + I_F \simeq V_{in} \left(\frac{1}{Z_{in_1}} + \frac{1}{Z_F}\left[1 + K_{ve_1}\right]\right) \qquad (131)$$

The output current is given by

$$I_o = \frac{V_o}{Z_L} \simeq - \frac{K_{ve_1} V_{in}}{Z_L} \qquad (132)$$

Solving for the current gain with feedback yields

$$K_{iF} = \frac{I_o}{I_1} \simeq -\left(\frac{K_{ve_1}}{Z_L}\right) \frac{1}{\frac{1}{Z_{in_1}} + \frac{1}{Z_F}\left(1 + K_{ve_1}\right)} \qquad (133)$$

Current Feedback

The method of analysis will be to determine a constant-current form of an equivalent circuit for the amplifier without feedback, and then to modify this equivalent circuit by adding the feedback circuit to determine the desired design equations. The common emitter amplifier configuration will be used as the basic circuit for the analysis.

Figure 18 is the common emitter amplifier stage with the biasing network not shown. Figure 22 is the constant-current form of equivalent circuit for the amplifier stage.

In Fig. 22

K_{iS} = current gain of the amplifier with the output short circuited

Z_T = output terminal impedance with the input open circuited

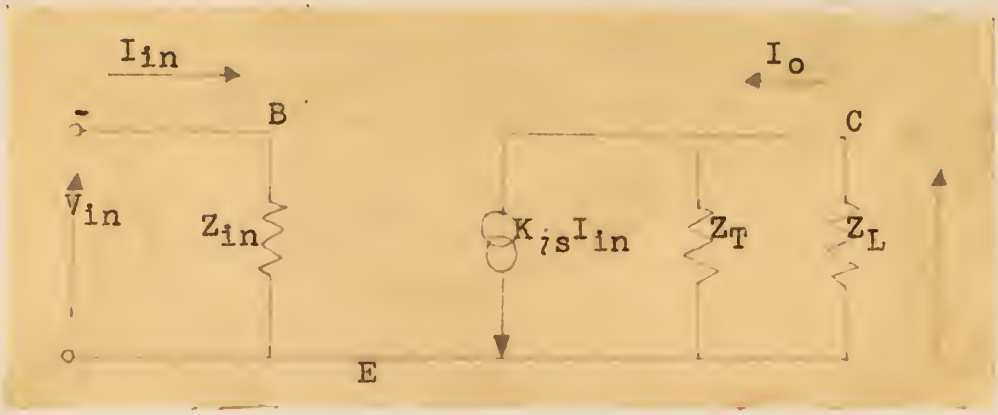

Fig. 22. Constant-current form of equivalent circuit for the common emitter amplifier stage.

Z_{in} = input impedance

B, C, E = the base, collector, and emitter terminals respectively.

The short-circuit current gain can be found for the general case by referring to Fig. 6, Eq. (16), and letting $V_2 = 0$.

$$I_2/I_1 = 1/D \tag{134}$$

Therefore in Fig. 22

$$K_{is} = 1/D \tag{135}$$

In terms of the common emitter equivalent circuit previously developed, Eq. (37), D is

$$D = - \frac{Z_e R_e + Z_c R_e}{BZ_e Z_c - Z_e R_e} \tag{136}$$

Therefore the short-circuit current gain is

$$K_{is} = - \frac{BZ_e Z_c - Z_e R_e}{Z_e R_e + Z_c R_e} \tag{137}$$

Z_T can be found by using Eq. (24) by letting $Z_g \longrightarrow \infty$ (input open circuited).

$$Z_T = \frac{D}{C} = \frac{Z_e R_e + Z_c R_e}{R_e + B Z_e} \tag{138}$$

From Fig. 22 the equation for the current gain can be written as

$$K_{ie} = \frac{1}{D} \frac{Z_T}{Z_T + Z_L} \tag{139}$$

Substituting Eqs. (136) and (138) into Eq. (139) yields the previously derived Eq. (39) for the common emitter current gain.

The input impedance is given by Eq. (40).

The equation describing the amplifier stage with feedback will now be determined. Figure 23 is the common emitter amplifier stage with current feedback.

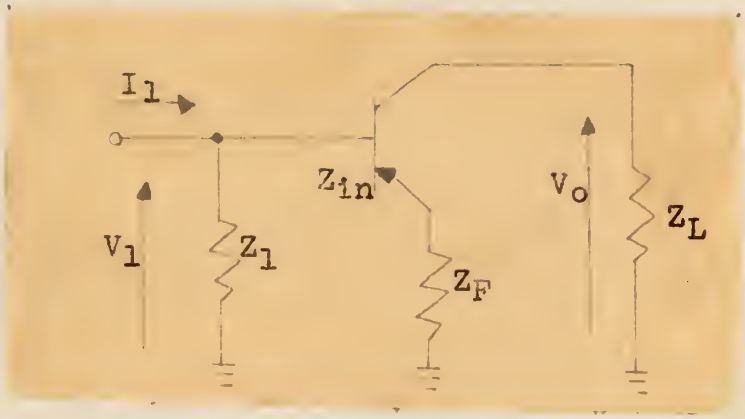

Fig. 23. Common emitter amplifier with current feedback.

Referring to Fig. 24 and writing the equation for E_{in} in terms of I_{in} (assuming $Z_T >> Z_F$ and $Z_L >> Z_F$), yields

$$V_{in} \simeq I_{in} (Z_{in} + Z_F) + K_{is} I_{in} \left(\frac{Z_T}{Z_T + Z_L}\right) Z_F \tag{140}$$

Solving Eq. (140) for V_{in}/I_{in} gives the input impedance with feedback when measured at the base terminal.

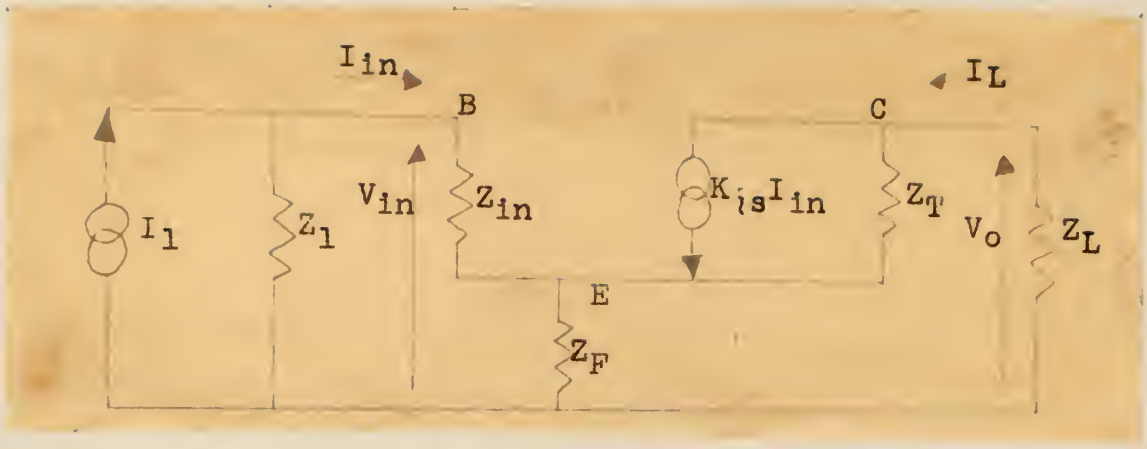

Fig. 24. Equivalent circuit of common emitter amplifier stage with current feedback.

$$Z_{inF_B} = \frac{V_{in}}{I_{in}} \simeq Z_{in} + Z_F \left[1 + K_{is} \left(\frac{Z_T}{Z_T + Z_L}\right)\right] \tag{141}$$

The input impedance with feedback taking into account Z_1 is

$$Z_{inF} = \frac{V_{in}}{I_1} \simeq \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_{in} + Z_F \left[1 + K_{is}\left(\frac{Z_T}{Z_T + Z_L}\right)\right]}} \tag{142}$$

Solving for V_o gives (assuming $Z_o >> Z_F$ and $Z_L >> Z_F$),

$$V_o \simeq - K_{is} I_{in} Z_L \frac{Z_T}{Z_T + Z_L} \tag{143}$$

The voltage gain with feedback is

$$K_{vF} = V_o / V_{in} \tag{144}$$

Substituting Eqs. (140) and (143) into Eq. (144) yields

$$K_{vF} \simeq - \frac{K_{is} \frac{Z_T}{Z_T + Z_L} Z_L}{Z_{in} + Z_F \left(1 + K_{is} \frac{Z_T}{Z_T + Z_L}\right)} \tag{145}$$

Derivation of current gain with feedback.

From Fig. 24

$$I_1 \simeq I_{in} \frac{Z_1 + Z_{inF_B}}{Z_1} \tag{146}$$

$$I_o \simeq - K_{is} I_{in} \frac{Z_o}{Z_o + Z_L} \tag{147}$$

Solving for current gain yields

$$I_{iF} \simeq \frac{I_o}{I_1} = - Z_1 \frac{K_s I_{in} \dfrac{Z_T}{Z_T + Z_L}}{I_{in}(Z_1 + Z_{inF_B})} \tag{148}$$

Substituting Eq. (141) into Eq. (148) and simplifying, yields

$$K_{iF} \simeq - \frac{Z_1}{Z_F} \frac{}{1 + \dfrac{1}{K_{is} \dfrac{Z_T}{Z_T + Z_L}} \left(\frac{Z_1}{Z_F} + \frac{Z_{in}}{Z_F} + 1\right)} \tag{149}$$

If $K_{is} \dfrac{Z_T}{Z_T + Z_L} \; Z_F >> Z_1 + Z_{in} + Z_F$,

$$K_{iF} \simeq - \frac{Z_1}{Z_F} \tag{150}$$

HIGH-FREQUENCY AMPLIFICATION

Undoubtedly the most important consideration in the design of a high-frequency amplifier is the proper choice of the transistor to be used. If signal power gain is used as a criterion for the usefulness of a given transistor at a given frequency, a figure of merit for the transistor can be developed

which is analogous to the well known gain bandwidth product for the vacuum tube. The figure of merit for the transistor is the frequency at which the signal power gain is unity. The figure of merit is often defined on data sheets as the maximum frequency of oscillation. Once the figure of merit for a transistor has been determined the signal power gain that is possible at frequencies below it can be estimated, using the approximation that signal power gain increases 6 db per octave below the figure of merit.

Derivation of Figure of Merit

The figure of merit[1] for transistors can be determined from the basic equivalent circuit.

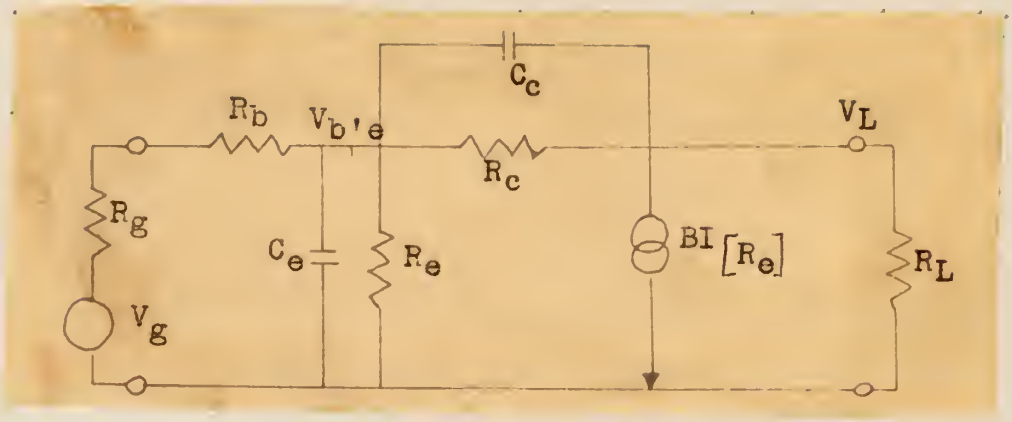

Fig. 25. Equivalent circuit for determining signal power gain.

Since the figure of merit is for optimum conditions, it will be derived assuming the input and output are conjugately

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[1]L. Giacoletto, "Study of P-N-P Alloy Junction Transistor from D-c through Medium Frequencies," RCA Review, vol. 14, December, 1954.

matched. The condition of unity power gain occurs at the upper useful frequency range of the transistor, so at high frequencies certain simplifying conditions hold. These are:

$$X_e >> X_c \qquad R_e >> X_e \qquad R_c >> X_c >> R_L$$

$$R_b >> X_e \qquad f >> f \propto b$$

The following equations are taken directly from the equivalent circuit.

Since as stated above $R_b >> X_e$ and $X_c >> R_b$, the input power under matched conditions ($R_b = R_g$) is

$$P_{in} \simeq \frac{|V_g|^2}{4R_b} \tag{151}$$

The output power is

$$P_o = \frac{|V_L|^2}{R_L} \tag{152}$$

since the output is matched $R_L = R_o$, where R_o is the output resistance of the transistor. The output impedance for the high-frequency case was derived as Eq. (58), and is

$$Z_{out_e} = \frac{X_c Z_g + X_c(X_e + R_b)}{(1 + h_{fe})Z_g + (1 + h_{fe})R_b + X_e} \tag{153}$$

Using the approximation that $h_{fe} >> 1$ and the simplifying relationships stated above, the output impedance is

$$Z_{out\ e} \simeq \frac{X_c}{h_{fe}} \tag{154}$$

Since $h_{fe} = \frac{BZ_e}{R_e}$, the output impedance can be written as

$$Z_{out\ e} = R_o = R_L \simeq \frac{C_e R_e}{C_c B} \tag{155}$$

Equation (155) indicates that the output impedance of the transistor is resistive at high frequencies.

Solving for the output voltage in terms of the current generator $BI_{[R_e]}$ yields

$$V_L \simeq BI_{[R_e]} R_L = h_{fe} I_{[C_e]} R_L \tag{156}$$

Since $X_e << R_e$, $X_c >> R_b$, and $X_c >> R_L$, solving for $I_{[C_e]}$ yields

$$I_{[C_e]} = \frac{V_g}{2 R_b} - h_{fe} I_{[C_e]} \frac{R_L}{X_c} \tag{157}$$

It has been established that $R_L = R_o$ and $R_o \simeq \frac{X_c}{h_{fe}}$. Using these relationships in Eq. (157), and solving for $I_{[C_e]}$ yields

$$I_{[C_e]} \simeq \frac{V_g}{4 R_b} \tag{158}$$

Combining Eqs. (156) and (158), and solving for V_L, yields

$$V_L \simeq h_{fe} \frac{V_g}{4 R_b} R_L \tag{159}$$

In terms of B

$$V_L \simeq \frac{BX_e}{R_e} \frac{V_g}{4 R_b} R_L \tag{160}$$

or

$$V_L \simeq \frac{B V_g R_L}{j\omega C_e R_e 4 R_b} \tag{161}$$

Combining Eqs. (152), (155), and (161) and solving for the output power, yields

$$P_o \simeq \frac{B|V_g|^2}{16 R_b^2 \omega^2 R_e C_e C_c} \tag{162}$$

The power gain is

$$P_G = \frac{P_o}{P_{in}} \simeq \frac{B}{(2\pi f)^2 \, 4 \, R_b R_e C_e C_c} \tag{163}$$

Setting the power gain equal to 1 and solving for f yields

$$f = \sqrt{\frac{B}{8 \pi R_b C_c} \; \frac{1}{2 \pi R_e C_e}} \tag{164}$$

but $f_{\alpha e} = \dfrac{1}{2 \pi C_e R_e}$ and $f_{\alpha b} = B \, f_{\alpha e}$. Therefore

$$f = \sqrt{\frac{f_{\alpha b}}{8 \pi R_b C_c}} \tag{165}$$

Equation (165) is the figure of merit for the transistor, or the frequency at which the power gain is equal to unity under matched conditions.

Alternate Equivalent Circuits

The parameters for the y-equivalent circuit, Fig. 27, and the π-equivalent circuit, Fig. 28, will now be determined in terms of the parameters of the basic equivalent circuit, Fig. 26. The π-equivalent circuit will be useful in determining the design equations for neutralizing a transistor amplifier stage, as will be shown later.

The transfer matrix parameters that describe Fig. 26 have been previously determined in Eqs. (34), (35), (36), and (37). In general the equations describing Fig. 26 in terms of the transfer matrix parameters are:

$$V_1 = A \, V_2 + B \, I_2 \tag{166}$$

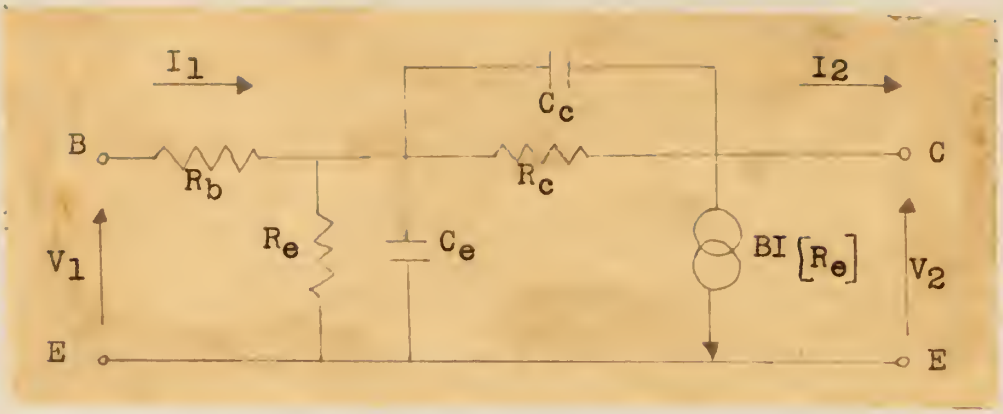


Fig. 26. Hybrid π-equivalent circuit.

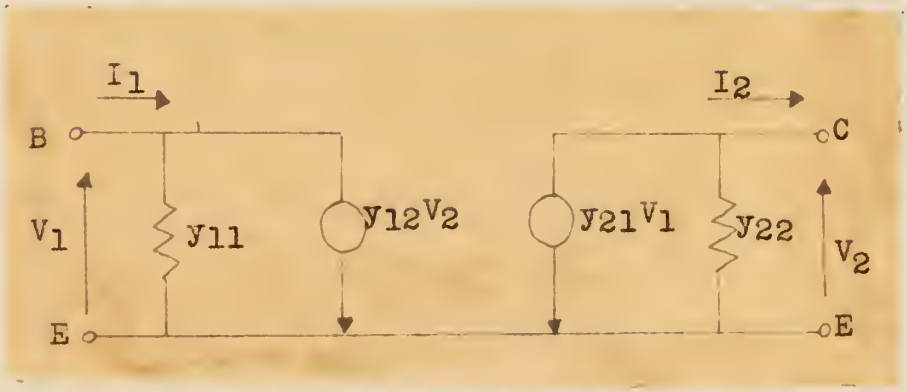


Fig. 27. Y-equivalent circuit.

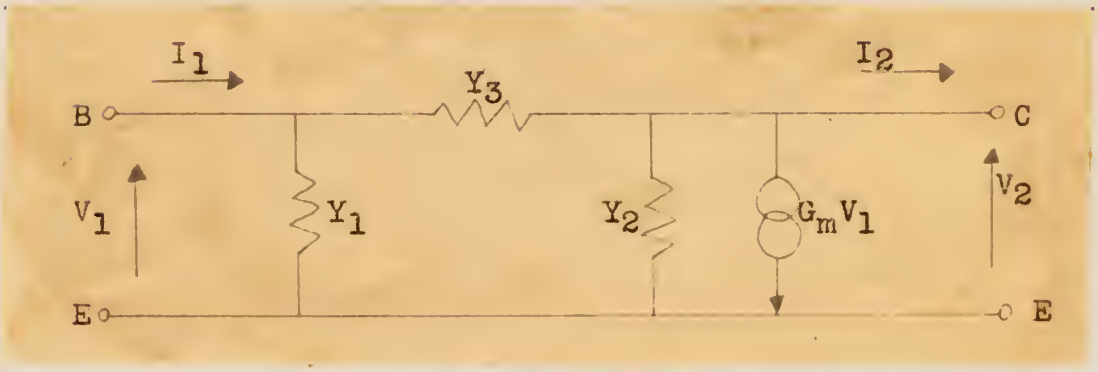


Fig. 28. π-equivalent circuit.

$$I_1 = C\ V_2 + D\ I_2 \qquad (167)$$

The equations describing Fig. 27 in terms of the y-parameters are:

$$I_1 = y_{11}\ V_1 + y_{12}\ V_2 \qquad (168)$$

$$-I_2 = y_{21} V_1 + y_{22} V_2 \tag{169}$$

Solving Eq. (166) for I_2 yields

$$I_2 = V_1 \frac{1}{B} - V_2 \frac{A}{B} \tag{170}$$

or

$$-I_2 = -\frac{1}{B} V_1 + \frac{A}{B} V_2 \tag{171}$$

Substituting Eq. (170) into Eq. (167) yields

$$I_1 = \frac{D}{B} V_1 - \left(\frac{DA - BC}{B}\right) V_2 \tag{172}$$

Comparing Eqs. (171) and (172) with Eqs.(168) and (169), the following relationships are evident.

$$y_{11} = \frac{D}{B} \tag{173}$$

$$y_{12} = \frac{BC - DA}{B} \tag{174}$$

$$y_{21} = -\frac{1}{B} \tag{175}$$

$$y_{22} = \frac{A}{B} \tag{176}$$

From Eqs. (34), (35), (36), and (37), the transfer matrix parameters for the hybrid π-equivalent circuits are:

$$A = -\frac{R_e R_b + R_e Z_e + B Z_e R_b}{B Z_e Z_c - R_e Z_e} \tag{177}$$

$$B = -\frac{R_e Z_e Z_c + Z_e R_e R_b + Z_c R_b R_e}{B Z_e Z_c - Z_e R_e} \tag{178}$$

$$C = -\frac{R_e + B Z_e}{B Z_e Z_c - Z_e R_e} \tag{179}$$

$$D = - \frac{Z_e R_e + Z_c R_e}{B Z_e Z_c - Z_e R_e} \tag{180}$$

Substituting Eqs. (177) through (180) into Eqs. (173) through (176) yields

$$y_{11} = \frac{Z_e R_e + Z_c R_e}{R_e Z_e Z_c + Z_e R_e R_b + Z_c R_b R_e} \tag{181}$$

$$y_{12} = \frac{- Z_e}{Z_e Z_c + Z_e R_b + Z_c R_b} \tag{182}$$

$$y_{21} = \frac{B Z_e Z_c - Z_e R_e}{R_e Z_e Z_c + Z_e R_b R_e + Z_c R_b R_e} \tag{183}$$

$$y_{22} = \frac{R_e R_b + R_e Z_e + B Z_e R_b}{R_e Z_e Z_c + Z_e R_b R_e + Z_c R_b R_e} \tag{184}$$

Equations (181) through (184) above give the y-parameters of Fig. 27 in terms of the hybrid π-parameters of Fig. 26.

The following relationships between the parameters of Figs. 27 and 28 are evident.

$$y_{11} = Y_1 + Y_3 = \frac{I_1}{V_1} \quad (V_2 = 0) \tag{185}$$

$$y_{22} = Y_2 + Y_3 = \frac{I_2}{V_2} \quad (V_1 = 0) \tag{186}$$

$$y_{21} = G_m - Y_3 = \frac{I_2}{V_1} \quad (V_2 = 0) \tag{187}$$

$$y_{12} = -Y_3 = \frac{I_1}{V_2} \quad (V_1 = 0) \tag{188}$$

Solving for the π equivalent circuit parameters in terms of the hybrid π equivalent circuit parameters yields

$$Y_3 = -y_{12} = \frac{Z_e}{Z_eZ_c + Z_eR_b + Z_cR_b} \tag{189}$$

$$G_m = y_{21} + Y_3 = \frac{BZ_eZ_c}{R_eZ_eZ_c + Z_eR_bR_e + Z_cR_bR_e} \tag{190}$$

$$Y_2 = y_{22} - Y_3 = \frac{R_eR_b + BZ_eR_b}{R_eZ_eZ_c + Z_eR_bR_e + Z_cR_bR_e} \tag{191}$$

$$Y_1 = y_{11} - Y_3 = \frac{Z_c}{Z_eZ_c + Z_eR_b + Z_cR_b} \tag{192}$$

Equations (189) through (192) give the π equivalent circuit parameters of Fig. 28 in terms of the hybrid-π parameters of Fig. 26.

The equivalent circuit of Fig. 28 is more useful if the Y-parameters are divided into their real and imaginary components as shown in Fig. 29.

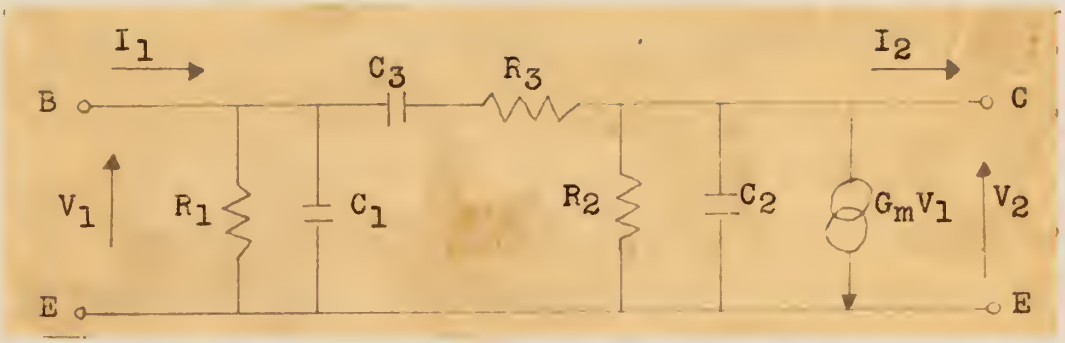


Fig. 29. π-equivalent circuit showing real and imaginary components.

Comparing Figs. 28 and 29, the following relationships are evident.

$$Y_1 = \frac{1}{R_1} + j\omega c_1 \tag{193}$$

$$Y_2 = \frac{1}{R_2} + j\omega c_2 \tag{194}$$

$$Y_3 = \frac{1}{R_3 + \dfrac{1}{j\omega c_3}} \tag{195}$$

$$G_m = g_{mR} + jg_{mI} \tag{196}$$

The following results are obtained by solving Eqs. (189) through (192) for their real and imaginary components as indicated in Eqs. (193) through (196).

$$R_1 \simeq R_b + R_e \frac{R_e + R_b}{R_e + R_b + \omega^2 C_e{}^2 R_e{}^2 R_b} \tag{197}$$

$$C_1 \simeq C_e \frac{1}{(1 + \frac{R_b}{R_e})^2 + \omega^2 C_e{}^2 R_b{}^2} \tag{198}$$

$$R_2 = \frac{R_c}{1 + BR_b \dfrac{R_e+R_b+\omega^2 C_e C_c R_e R_b R_c}{(R_b+R_e)^2 + \omega^2 C_e{}^2 R_e{}^2 R_b{}^2}} \tag{199}$$

For low power transistor $R_e >> R_b$, since $R_e \simeq \dfrac{B26}{I_E(ma)}$, $B \simeq R_b$, and $I_E < 5$ ma.

Simplifying Eq. (199) yields

$$R_2 \simeq \frac{R_c}{1 + B\dfrac{R_b}{R_e}\dfrac{1 + \omega^2 C_e C_c R_b R_c}{1 + \omega^2 C_e{}^2 R_b{}^2}} \tag{200}$$

At sufficiently high frequencies

$$R_2 \simeq \frac{C_e R_e}{B C_c} \tag{201}$$

and since $\omega_{\alpha b} = B/R_e C_c$

$$R_2 \simeq \frac{1}{\omega \alpha_b C_e} \tag{202}$$

$$C_2 \simeq C_c \left(1 + B \frac{R_b(R_b + R_e)}{(R_b+R_e)^2 + \omega^2 C_e^2 R_b^2 R_e^2}\right) \tag{203}$$

Solving for the real and imaginary parts of Y_3 yields

$$R_3 = R_b \left(\frac{C_e}{C_c}\right) + \frac{R_b + R_e}{R_e R_c \omega^2 C_c^2} \tag{204}$$

$$C_3 = \frac{C_c}{\frac{R_e + R_b}{R_e} - \frac{C_e R_b}{C_c R_c}} \tag{205}$$

$$g_{mR} \simeq \frac{B(R_b + R_e)}{(R_b + R_e)^2 + \omega^2 C_e^2 R_b^2 R_e^2} \tag{206}$$

$$g_{mI} \simeq -\frac{\omega C_e R_b R_e B}{(R_b + R_e)^2 + \omega C_e^2 R_b^2 R_e^2} \tag{207}$$

Equations (201) through (207) give the parameters of the equivalent circuit shown in Fig. 29 in terms of the parameters of the hybrid π-equivalent circuit shown in Fig. 26. Due to the complexity involved in calculating these equations, the following simplifying assumptions were made.

$$R_c >> R_b \qquad R_c >> R_e \qquad R_c >> B \qquad C_e >> C_c$$

NEUTRALIZATION

The basic limitation imposed by the transistor on its application in its upper useful frequency range is its inherent bilateral nature. As the operating frequency of the transistor is increased the internal feedback impedance between its output

and input becomes smaller, and instability due to positive feedback results. There are two basic methods of reducing the effects of the internal feedback and extending the useful frequency range of the transistor. The two methods discussed are: (1) Isolation by neutralization, and (2) isolation by mismatch.

Isolation by Neutralization

The principle involved in neutralization is simply to sample the output voltage of the stage to be isolated and feed back this voltage to the input with the correct phase and amplitude to cancel the internal feedback voltage. Figure 30 is an example of a neutralized transistor stage.

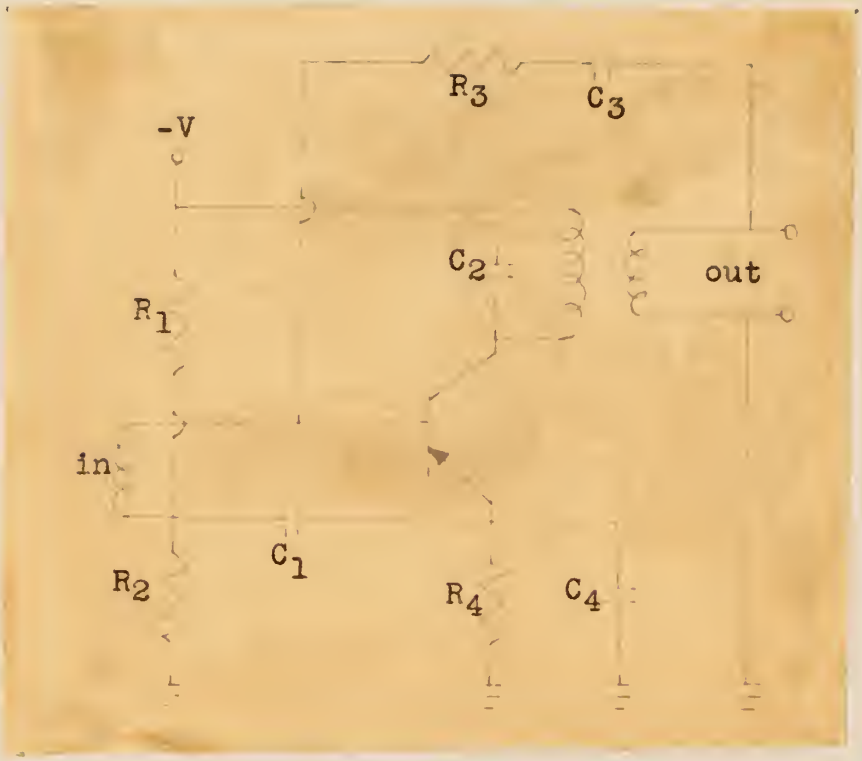
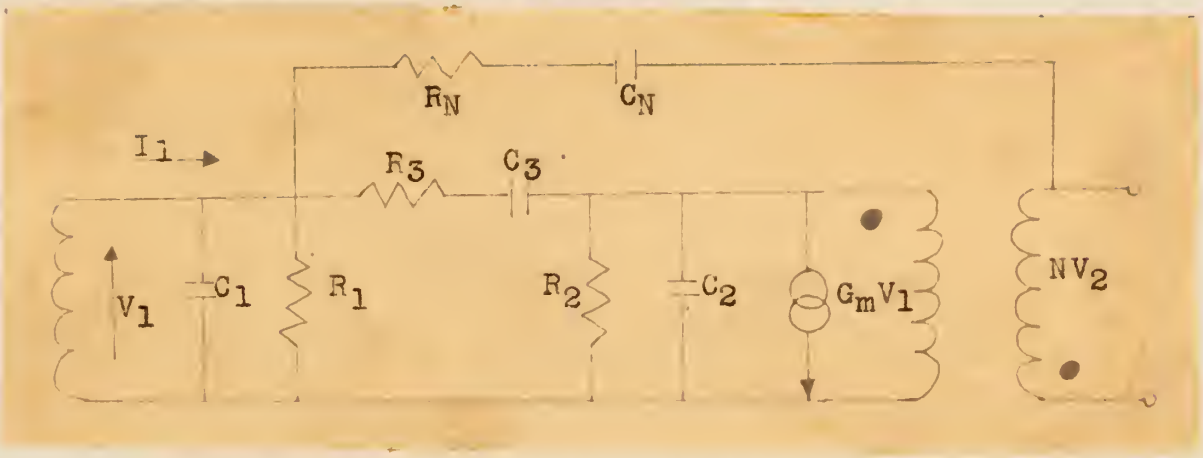


Fig. 30. Example of neutralized amplifier.

The problem the designer is faced with is to determine the correct value for the components that make up the neutralizing network and develop an equivalent circuit to represent the neutralized stage. The method employed in this report to determine the required design equations is to use the π equivalent circuit previously developed (see Fig. 28). The desired values of the feedback components are determined with only minor calculations from this equivalent circuit. Figure 31 is the a-c equivalent circuit of the neutralized amplifier.



N = transformer turns ratio

N > 1 = for step-up transformer

N < 1 = for step-down transformer

Fig. 31. Equivalent circuit of neutralized amplifier.

From Fig. 31 it is evident that for proper neutralization (assuming an ideal transformer)

$$R_N = N R_3 \tag{208}$$

$$C_N = C_3/N \tag{209}$$

where R_3 and C_3 are given by Eqs. (204) and (205). Therefore

$$R_N = N \left(\frac{R_b C_e}{C_c} + \frac{R_b + R_e}{R_e R_c \omega^2 C_c^2} \right) \tag{210}$$

and

$$C_N = \frac{1}{N} \left(\frac{C_c}{\frac{R_e + R_b}{R_e} - \frac{C_e R_b}{C_c R_c}} \right) \tag{211}$$

Equations (210) and (211) are the desired values of the neutralizing components in terms of the hybrid equivalent circuit parameters.

Since neutralizing the amplifier eliminates the internal feedback, the neutralized transistor can be represented by the equivalent circuit of Fig. 32.

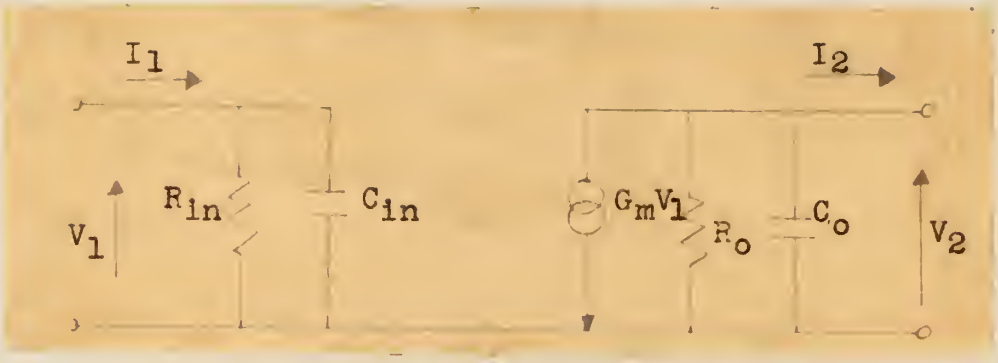


Fig. 32. Equivalent circuit of neutralized amplifier stage.

In Fig. 32

$$R_{in} = R_1 \quad \text{(see Eq. (197))} \tag{212}$$

$$C_{in} = C_1 \quad \text{(see Eq. (198))} \tag{213}$$

$$R_o = R_2 \quad \text{(see Eq. (199))} \tag{214}$$

$$C_o = C_2 \quad \text{(see Eq. (203))} \tag{215}$$

$$G_m = g_{mR} + j g_{m_1} \quad \text{(see Eqs. (206) and (207))} \tag{216}$$

assuming

$$R_N + j\omega C_N >> \frac{1}{\frac{1}{R_1} + j\omega C_1} \quad \text{and} \quad R_N + j\omega C_N >> \frac{1}{\frac{1}{R_2} + j\omega C_2} .$$

The common emitter configuration was used as the basis of analysis in the previous example. The common base configuration can be neutralized in a similar manner, the requirement being that

$$Y_N = - y_{12} \tag{217}$$

where Y_N = the effective neutralizing admittance

y_{12} = the reverse transfer admittance of the transistor.

In terms of the common base transfer matrix parameters (Eq. 83),

$$y_{12} = \frac{BC - DA}{B} \simeq - \frac{R_b(R_e + BZ_e)}{Z_c R_e (Z_e + R_b)} \tag{218}$$

assuming $Z_c >> R_b$.

Figure 33 shows a typical neutralized common base stage with the biasing network not shown.

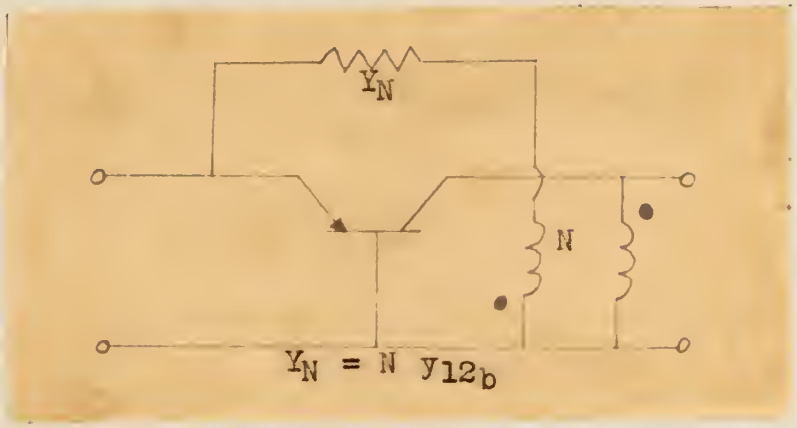


Fig. 33. Neutralized common base stage.

Isolation by Mismatch

Theoretically, isolation by neutralization is the optimum method of stabilizing a transistor at high frequencies, but it soon becomes apparent to the design engineer that though neutralization is the optimum method it has certain troublesome limitations. Transistor parameters vary from unit to unit and since the neutralizing network must be identical to the internal feedback network, considerable adjustment time is required for each unit under production conditions. Wide-band amplifiers also present problems when neutralization is attempted, since the neutralizing network can be made optimum for only one set of parameters and one frequency. It is possible to reduce the effects of the bilateral nature of the transistor without resorting to the complication of a neutralizing network by sacrificing gain in the interstage network. Isolation by this method will be termed isolation by mismatch since the method requires a deliberate mismatch between transistor output impedance and load impedance.

The problem is to determine the maximum load impedance that will assure stable operation. Or, after the design of the stage has been completed, meeting the design specifications, the stage should be reevaluated to see if it is stable using limit transistors and components.

The equivalent circuit shown in Fig. 34 will be used to derive the equation for the maximum stable load impedance. The

equivalent circuit is identical with the basic equivalent circuit (Fig. 5) with

$$Z_e = \frac{R_e}{1 + j\omega C_e R_e}, \quad Z_c = \frac{R_c}{1 + j\omega C_c R_c},$$

and

$$h_{fe} = \frac{BZ_e}{R_e} = \frac{B}{1 + j\omega C_e R_e}$$

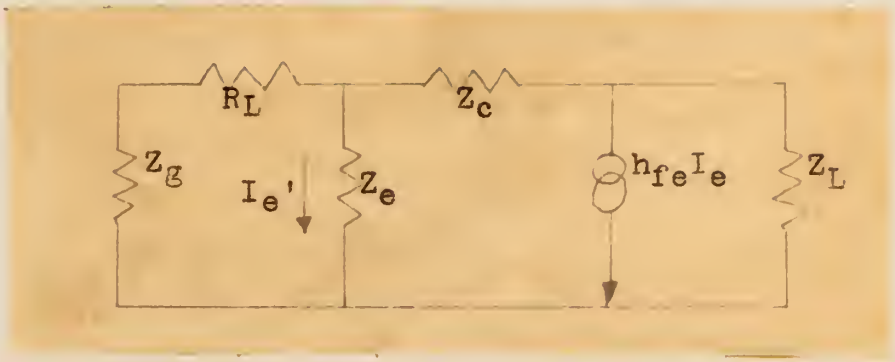


Fig. 34. Transistor equivalent circuit, terminated by load and generator impedances.

Assuming no externally applied signals, instability occurs when $I_e' = I_e$.

Solving for I_e' in terms of the current generator $h_{fe}I_e$ yields

$$I_e' = -h_{fe}I_e \frac{Z_L(R_b + Z_g)}{(Z_c + \frac{Z_e(R_b+Z_g)}{Z_e+R_b+Z_g} + Z_L)(R_b + Z_g + Z_e)} \tag{219}$$

Since $Z_c >> Z_e$, Eq. (219) can be simplified.

$$I_e' = -h_{fe}I_e \frac{Z_L}{Z_c + Z_L} \frac{R_b + Z_g}{R_b + Z_g + Z_e} \tag{220}$$

Instability occurs when $I_e' = I_e$, or when

$$h_{fe} \frac{Z_L}{Z_c + Z_L} \frac{R_b + Z_g}{R_b + Z_g + Z_e} + 1 = 0 \tag{221}$$

Rearranging Eq. (220), to separate the terms $1/Z_g$ and $1/Z_L$, and using the approximation that in the frequency range of interest $h_{fe} >> 1$, yields

$$\left(\frac{1}{Z_e + R_b} + \frac{1}{Z_g}\right)\left(\frac{h_{fe} R_b + Z_e}{Z_c(Z_e + R_b)} + \frac{1}{Z_L}\right) + \frac{h_{fe} Z_e}{Z_c(Z_e + R_b)^2} \simeq 0 \qquad (222)$$

In general, Eq. (222) can be written in terms of real and imaginary components.

$$(re(a) + j\, im(a))(re(b) + j\, im(b)) = -re(c) - j\, im(c) \qquad (223)$$

where re = real term

im = imaginary term

$$a = \frac{1}{Z_e + R_b} + \frac{1}{Z_g}$$

$$b = \frac{h_{fe} R_b + Z_e}{Z_c(Z_e + R_b)} + \frac{1}{Z_L}$$

$$c = \frac{h_{fe} Z_e}{Z_c(Z_e + Z_b)^2}$$

Equation (223) can be written as two real equations.[1]

$$re(a)\, re(b) - im(a)\, im(b) = -re(c) \qquad (224)$$

$$im(b)\, re(a) + im(a)\, re(b) = -im(c) \qquad (225)$$

Solving Eq. (224) for im(a) and im(b) yields

$$im(a) = \frac{re(a)\, re(b) + re(c)}{im(b)} \qquad (226)$$

$$im(b) = \frac{re(a)\, re(b) + re(c)}{im(a)} \qquad (227)$$

---

[1] W. Gartner, Transistors Principles, Design, and Applications, D. Van Nostrand Company, Inc., Princeton, New Jersey, p. 370.

Substituting Eqs. (226) and (227) into Eq. (225) and solving for im(a) and im(b), yields

$$\text{im(a)} = \frac{-\text{im(c)} \pm \sqrt{(\text{im(c)})^2 - 4\ \text{re(b)}\ \text{re(c)}\ \text{re(a)} + \text{re(a)}^2\ \text{re(b)}}}{2\ \text{re(b)}} \tag{228}$$

$$\text{im(b)} = \frac{-\text{im(c)} \pm \sqrt{\text{im(c)}^2 - 4\ \text{re(b)}\ \text{re(c)}\ \text{re(a)} + \text{re(a)}^2\ \text{re(b)}}}{2\ \text{re(a)}} \tag{229}$$

For possible instability, Eqs. (228) and (229) must be real to satisfy Eqs. (224) and (225). If

$$0 < \text{re(a)}^2\ \text{re(b)}^2 + \text{re(a)}\ \text{re(b)}\ \text{re(c)} - \frac{\text{im(c)}^2}{4}$$

Eqs. (224) and (225) will be imaginary and stability will be assured independent of load and generator susceptances. In a tuned amplifier it is necessary to determine the maximum values of the real parts of the terminating impedances independent of the imaginary parts, since in the "tuning up" process the imaginary parts may assume a wide range of values. If the real part of Eq. (222) is satisfied, then it is possible that during "tune up" the imaginary part will be satisfied and instability will result.

Setting Eq. (230) equal to zero (limit of assured stability) and solving for re(a) re(b), yields

$$2\ \text{re(a)}\ \text{re(b)} = -\text{re(c)} + |\,\text{c}\,| \tag{231}$$

$$2\ \text{re(a)}\ \text{re(b)} = -\text{re(c)} - |\,\text{c}\,| \tag{232}$$

where $|\,\text{c}\,|$ indicates the magnitude of c.

Equations (231) and (232) describe two equilateral[1] hyperbolas illustrated in Fig. 35.

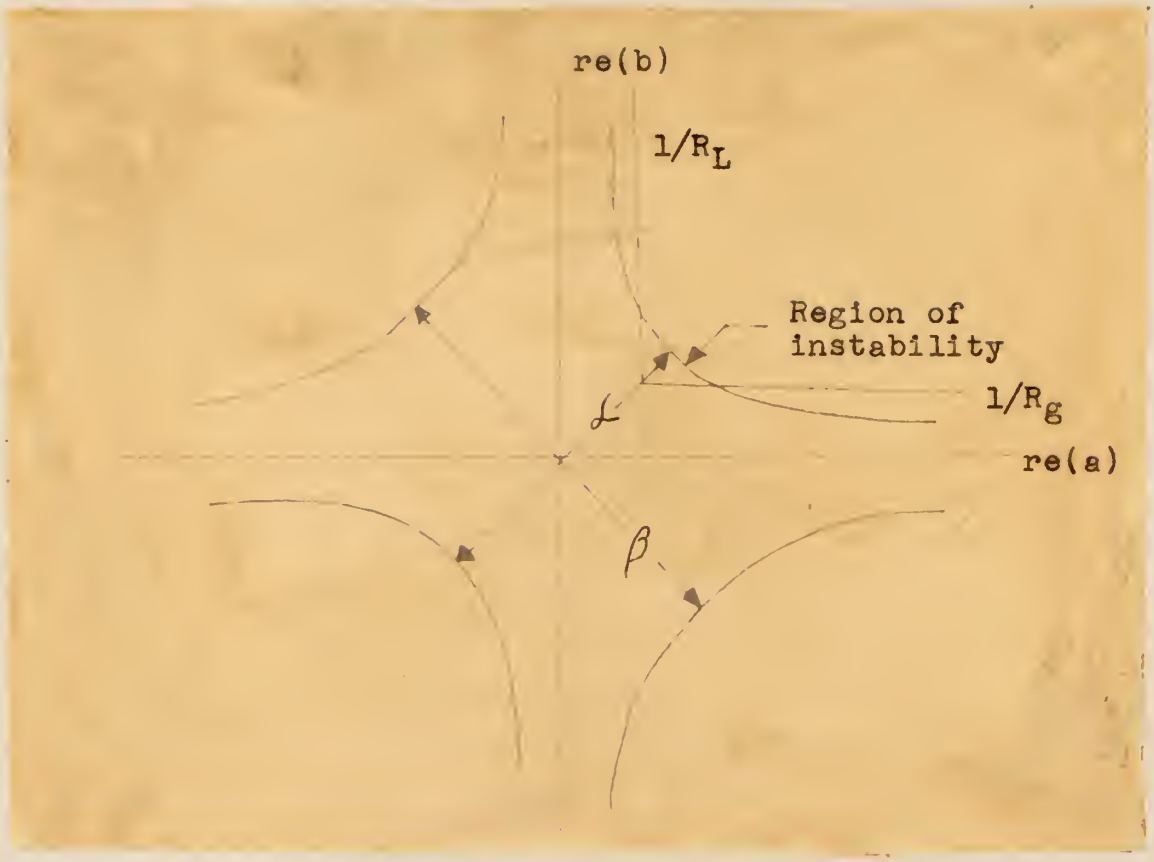


Fig. 35. Graphical presentation of Eqs. (231) and (232).

In Fig. 35

$$\alpha = 2\left[-re\left(\frac{h_{fe}\,Z_e}{Z_c(Z_e + R_b)^2}\right) + \left|\frac{h_{fe}\,Z_e}{Z_c(Z_e + R_b)^2}\right|\right] \qquad (233)$$

$$\beta = 2\left[-re\left(\frac{h_{fe}\,Z_e}{Z_c(Z_e + R_b)^2}\right) - \left|\frac{h_{fe}\,Z_e}{Z_c(Z_e + R_b)^2}\right|\right] \qquad (234)$$

where

---

[1]Ibid., page 371.

$$re\left(\frac{1}{Z_e + R_b}\right) \simeq \frac{R_e + \frac{\omega^2}{\omega_{\alpha e}^2} R_b}{R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2} \tag{235}$$

$$re\left(\frac{h_{fe} R_b + Z_e}{Z_c(Z_e + R_b)}\right) \simeq \frac{\frac{\omega^2}{\omega_{\alpha e}} C_c R_b(BR_b + R_e)}{R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2} \tag{236}$$

$$re\left(\frac{h_{fe} Z_e}{Z_c(Z_e + R_b)^2}\right) \simeq \frac{2\frac{\omega}{\omega_{\alpha e}} C_c B R_e^2 R_b}{(R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2)^2} \tag{237}$$

$$\left|\frac{h_{fe} Z_e}{Z_c(Z_e + R_b)^2}\right| \simeq \frac{\omega C_c B R_e}{R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2} \tag{238}$$

Equations (235) through (238) were derived assuming $Z_c \simeq \frac{1}{j\omega C_c}$, $R_e >> R_b$, $h_{fe} >> 1$, and $\omega_{\alpha e} \simeq \frac{1}{R_e C_e}$. $\omega_{\alpha e}$ is the common emitter angular cut-off frequency described previously.

Assuming $1/R_g$ and $1/R_L$ are positive values, Eq. (231) is the one of interest. Substituting Eqs. (235) through (238) into Eq. (231), and simplifying, yields the equation for absolute stability.

$$\left(\frac{R_e + \frac{\omega^2}{\omega_{\alpha e}^2} R_b}{R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2} + \frac{1}{R_g}\right)\left(\frac{\frac{\omega^2}{\omega_{\alpha e}^2} C_c R_b(BR_b + R_e)}{R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2} + \frac{1}{R_L}\right) >$$

$$\frac{B\,\omega\,C_c R_e\,(\frac{\omega}{\omega_{\alpha e}} R_b - R_e)^2}{(R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2)^2} \tag{239}$$

Solving Eq. (239) for $1/R_L$ yields

$$\frac{1}{R_L} > \frac{\omega C_c B R_e (R_e - \frac{\omega}{\omega_{\alpha e}} R_b)^2 R_g}{2(R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2)\left(\left[R_e + \frac{\omega^2}{\omega_{\alpha e}^2} R_b\right] R_g + R_e^2 + \frac{\omega^2}{\omega_{\alpha e}^2} R_b^2\right)}$$

$$- \frac{\omega^2 C_c R_b(BR_b + R_e)}{\omega_{\alpha e}(R_e^2 + \frac{\omega}{\omega_{\alpha e}^2} R_b^2)} \tag{240}$$

When ω is of the same order of magnitude of $\omega_{\alpha e}$ (mid-frequency range), Eq. (240) can be further simplified to yield

$$R_L < \frac{2\,|X_c|}{B} \cdot \frac{R_g + R_e}{R_g} \quad \text{where } |X_c| = \frac{1}{\omega C_c} \tag{241}$$

If Eq. (240) or (241) is satisfied (depending on the frequency range of interest), the transistor will be unconditionally stable.

Conversely, the maximum stable value of R_g could have been determined for a given R_L.

Above a certain frequency the transistor will be unconditionally stable regardless of the terminating impedances. If the transistor parameters are such that the $1/R_g$, $1/R_L$ plane never overlaps the parabola in the first quadrant of Fig. 35, the transistor will be unconditionally stable regardless of the values of $1/R_L$ or $1/R_g$ (assuming positive values). When this occurs may be determined from Eq. (239) as follows.[1]

$$2\left(R_e + \frac{\omega^2}{\omega_{\alpha e}^2} R_b\right)\left(\frac{\omega^2}{\omega_{\alpha e}} C_c R_b \left[BR_b + R_e\right]\right) > \omega\, C_c B R_e \left(\frac{\omega}{\omega_{\alpha e}} R_b - R_e\right)^2 \qquad (242)$$

Solving Eq. (239) for the smallest frequency that will insure the inequality yields[2]

$$\omega_c > \frac{R_e}{2\,R_b}\,\omega_{\alpha e} \quad \text{(approximately)} \qquad (243)$$

If Eq. (243) is satisfied at the frequency of operation, stability is assured regardless of the terminating impedances. Equation (243) is for the common emitter configuration. The analagous equations[3] for the common base and common collector configuration are approximately

$$\omega_b > .7\sqrt[4]{\omega_{\alpha b}^3/C_c R_b} \qquad (244)$$

$$\omega_c > \tfrac{1}{2}\sqrt{\omega_{\alpha b}/C_c R_b} \qquad (245)$$

---

[1] A. P. Stern, "Considerations on the Stability of Active Elements and Applications to Transistors," IRE Convention Record, vol. 4, part 2, p. 46, 1956.

[2] Ibid., page 46.

[3] Ibid., page 46.

Equations (244) and (245) indicate that these two configurations are potentially unstable up to much higher frequencies than the common emitter configuration.

Another method that can be used to determine the maximum load impedance when mismatch is used is to use the criterion that the forward power gain should always be greater by a predetermined number of dbs than the reverse power attenuation. One criterion that has been suggested is that the forward power gain shall be 10 db greater than the reverse power attenuation for absolute stability.[1] The reverse power attenuation is calculated assuming the output load is such that the transistor's output is conjugate matched. Then the forward power gain is calculated for the same conditions. If the reverse power attenuation is 10 db less than the forward power gain, the transistor is stable. The problem is to determine the required reduction in load impedance if the matched condition produces a reverse power attenuation which is not at least 10 db less than the forward power gain.

Calculation of reverse power attenuation:

Solving for I under the conditions previously discussed yields

$$I \simeq V/X_c \qquad (246)$$

The current through Z_g is

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[1]Donald G. Paterson, Circuit Design Consideration Using the Mesa Transistor, "Application Note Number 14," Motorola, Inc., Semiconductor Products Division, May 1, 1959.

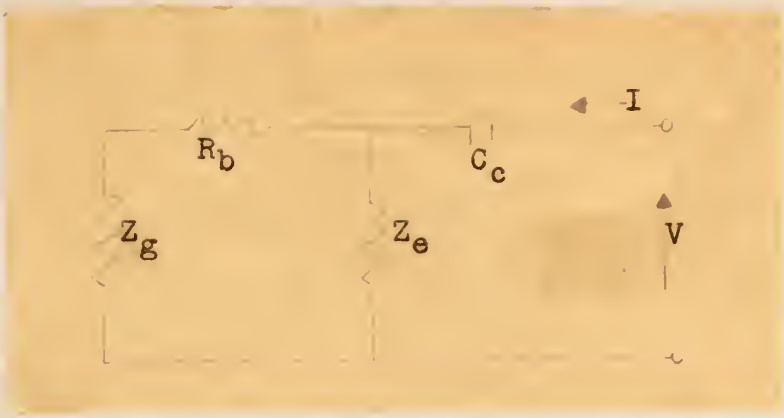

Fig. 36. Equivalent circuit for calculating reverse power gain.

$$I_g = I \frac{Z_e}{R_b + Z_g + Z_e} \tag{247}$$

The voltage developed by the feedback current through Z_g is

$$V_g \simeq \frac{V}{X_c} \frac{Z_e Z_g}{(R_b + Z_g + Z_e)} \tag{248}$$

The reverse power developed is

$$= \frac{|V_g|^2}{re(Z_g)} = \frac{|V_g|^2}{R_g} = \left|\frac{V}{X_c}\right|^2 \left|\frac{Z_g Z_e}{R_b+Z_g+Z_e}\right|^2 \frac{1}{R_g} \tag{249}$$

The power at the load is

$$P_L = \frac{|V|^2}{re(Z_L)} = \frac{|V|^2}{R_L} \tag{250}$$

where $R_L = R_o$ for matched condition.

The reverse power attenuation is

$$P_R = \frac{P_L}{P_g} = \left|X_c\right|^2 \left|\frac{R_b + Z_g + Z_e}{Z_e + Z_e}\right|^2 \frac{R_g}{R_L} \tag{251}$$

R_o can be calculated by finding the real part of Eq. (41).

The forward power gain is defined as the ratio of the power delivered to the load over the power into the transistor.

$$P_F = \left| K_{ie} \right|^2 \frac{R_L}{re(Z_{in_e})} \tag{252}$$

where K_{ie} is given by Eq. (39) and

Z_{in_e} is given by Eq. (40).

$$P_F \simeq \left| \frac{BZ_eZ_c}{R_e(Z_c+Z_L)+BZ_LZ_e} \right|^2 \frac{R_L}{re\left(R_b + \frac{(Z_c + Z_L)Z_eR_e}{R_e(Z_c+Z_L) + BZ_cZ_e}\right)} \tag{253}$$

Equation (253) is the forward power gain, assuming $Z_c >> Z_e$ and $Z_c >> R_e$.

For stability

$$P_F = 10\ P_R \tag{254}$$

Once the two power gains are calculated, the value of load resistance to achieve stable operation can be determined. Assume that $P_F < 10\ P_R$. This means that the forward power gain must be reduced by some factor.

The new output power should be

$$P_o = \frac{1}{K} \frac{|I|^2 R_L}{4} \tag{255}$$

where $R_L = R_o$

K = necessary reduction factor so that $P_F = 10\ P_R$.

Once K is known, the load resistance R_x placed in parallel with the output resistance that gives stable operation can be calculated. Figure 37 is a simplified version of the output circuit of the transistor used in calculating the necessary value of R_x for stable operation.

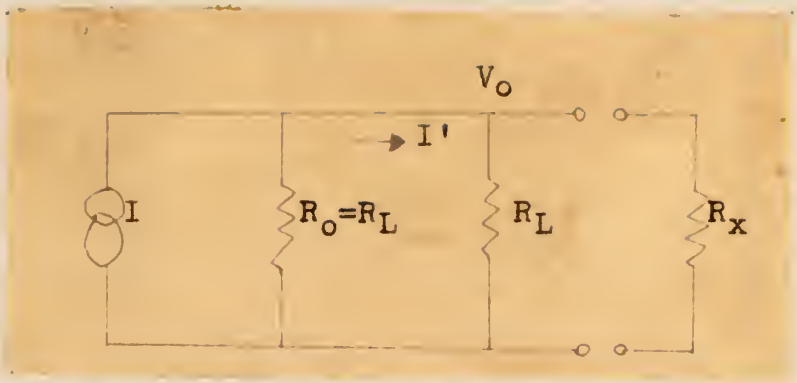

Fig. 37. Simplified circuit for calculation of R_x.

The current through R_L in parallel with R_x is

$$I' = I \frac{R_L + R_x}{2 R_x + R_L} \tag{256}$$

The new output power is given by

$$P_o = (I')^2 \frac{R_L R_x}{R_L + R_x} = I^2 \frac{(R_L + R_x)^2 (R_L R_x)}{(2 R_x + R_L)^2 (R_L + R_x)} \tag{257}$$

Setting Eq. (253) equal to Eq. (255)

$$\frac{(R_L + R_x) R_x R_L}{(2 R_x + R_L)^2} I^2 = \frac{I^2 R_L}{4K} \tag{258}$$

Solving Eq. (256) for R_x yields

$$R_x = \frac{R_L}{2} \left(-1 \pm \sqrt{\frac{K}{K - 1}}\right) \tag{259}$$

Since $K > 1$, $\sqrt{\frac{K}{K - 1}} > 1$ and the R_x of interest is positive, the value of R_x is given in Eq. (260).

$$R_x = \frac{R_L}{2} \left(\sqrt{\frac{K}{K - 1}} - 1\right) \tag{260}$$

BIAS CONSIDERATIONS AND TEMPERATURE EFFECTS

The choice of a proper biasing method to stabilize the operating point of the particular transistor circuit being designed is of paramount importance. An adequate biasing arrangement should serve the following purposes.

1. Minimize the spread in the input and output impedances due to the different d-c characteristics of individual transistors.
2. Prevent the danger of overloading the transistor at higher temperature due to increased collector current, resulting from the changes in transistor characteristics with increased temperature.
3. Prevent the possibility of thermal runaway, where internal dissipation causes an increase in junction temperature, followed by an increase in collector current, and therefore a further increase in dissipation.

Leakage Current Evaluation

The most detrimental cause of biasing instability is the various leakage currents that are inherent in every transistor. Listed below are the three pertinent leakage currents and their definitions.[1] Knowing the function of the circuit being designed

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[1]General Electric Transistor Manual, 6th ed., General Electric Company, p. 33, 1962.

and the definition of the leakage currents of the one this is applicable to, the design problem can be determined.

1. I_{CBO}. The collector current that will flow when the emitter is open-circuited and the collector-to-base diode is back-biased.
2. I_{EBO}. The emitter current that will flow when the collector is open-circuited and the base-to-emitter diode is back-biased.
3. I_{CEO}. The collector current that will flow from the collector to the emitter when the base is open-circuited and normal bias is applied to the collector.

Further elaboration will now be given to each individual leakage current.

1. I_{CBO}. I_{CBO} is the total leakage current that will flow between the collector and base and is composed of two leakage components.
   a. An internal thermal leakage component due to diode action which varies exponentially with temperature, and is relatively independent of collector voltage.
   b. A surface leakage component which is directly proportional to collector voltage and slightly affected by increased temperature.

Since the leakage current I_{CBO} flows when the collector-to-base diode is back-biased, this leakage current is applicable to circuits where this condition exists, such as for normal small signal application where the transistor is not in a

"cut-off" or "saturated" state.

2. I_{EBO}. This leakage current is similar to I_{CBO} in that it has a thermal and leakage component. I_{EBO} is often of the same magnitude as I_{CBO}, and is applicable where the base-to-emitter diode is back-biased, such as in switching circuits.

3. I_{CEO}. This leakage current does not have a straightforward explanation as in the case of I_{CBO} and I_{EBO}. One explanation is to postulate that I_{CBO} will flow as if the emitter were open-circuited instead of the base, but since the base is open-circuited the I_{CBO} that would normally flow must come from the emitter. The emitter current referred to the base is $I_E = \frac{1}{1 - \alpha} I_B$ where $I_B = I_{CBO}$ in this case. The collector current referred to the emitter is $I_c = \alpha I_E$ where $I_c = I_{CEO}$ in this case. Therefore $I_{CEO} = \frac{\alpha}{1 - \alpha} I_{CBO}$, or $I_{CEO} = BI_{CBO}$. This current is a major cause of thermal runaway when the transistor is operated with the base open or with a large value of resistance between base and emitter.

Since this report deals only with small signal applications, the leakage current of interest is I_{CBO}.

For predictable operation of any transistor circuit it is necessary to insure the bias stability of the circuit when limit transistors are used and the transistor is subjected to environmental extremes. Stating this problem as it applies to I_{CBO}

means that the "worst-case" I_{CBO} must be determined. Since in many cases I_{CBO} is specified only at 25 degrees C on the manufacturer's data sheet, it is necessary to determine the maximum value of I_{CBO} at elevated temperatures.

Below is a method of calculating the "worst-case" leakage current with the minimum data available.[1] The method makes several assumptions.

1. The thermal component of I_{CBO} doubles for approximately every 10 degrees C rise in junction temperature. This is a well established "rule of thumb" that is used in the transistor industry.
2. The leakage component varies linearly with voltage.
3. The leakage component increases with temperature at a rate one-half that of the thermal leakage component. This is a pessimistic figure but adds a safety margin to the evaluation.

The transistor junction temperature is

$$(1) \quad T_J = T_A + \triangle T_{PD}$$

where T_J = temperature of collector junction

T_A = ambient temperature

$\triangle T_{PD}$ = increase in junction temperature due to power dissipated in the device

Therefore $$\triangle T_{PD} = K \times P D$$

where K = thermal resistance in degrees C per milliwatt.

K should be given on all data sheets. If it is not given

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[1] P. G. Thomas, "Determining I_{CO} at Elevated Temperatures and Power Dissipations," Electronic Design News, January, 1960.

temperature (T_s). Therefore

$$K = \frac{T_{J\ max} - T_s}{PD \text{ at } T_s}$$

Also PD = total power dissipated in the transistor

$$PD = I_c(V_{cE} + \frac{V_{BE}}{B})$$

After determining the junction temperature that the transistor will be subjected to, it is now necessary to determine the leakage current I_{CBO} that will occur at this temperature. From the data sheet the maximum value of I_{CBO} can be determined at 25 degrees C. I_{CBO} should be specified at two values of collector voltage so that the surface leakage component can be calculated. If I_{CBO} is not specified at two separate collector voltages, a measurement should be made so the leakage component and thermal component can be separated.

An example for determining "worst-case" I_{CBO} at a given junction temperature T_J follows.

$$I_{CBO}\ (25°C) = x_{\mu a\ max} \text{ when } V_{CB} = z_{vdc}$$

$$I_{CBO}\ (25°C) = y_{\mu a\ max} \text{ when } V_{CB} = kz_{vdc}$$

It is now necessary to separate the surface leakage component from the thermal leakage component.

I_s = surface leakage component

I_T = thermal leakage component

$$I_{CBO} = I_s + I_T$$

Assuming that the surface leakage component varies linearly with collector voltage, the two components can be separated for a temperature of 25 degrees C.

$$I_S + I_T = x\,\mu a \qquad I_S = \frac{y - x}{K - 1}\,\mu a$$

$$KI_S + I_T = y\,\mu a \qquad I_T = \frac{Kx - y}{K - 1}\,\mu a$$

$$(K - 1)I_S = (y-x)\,\mu a \qquad A_T\, V_{CB} = Z_{vdc}$$

At the voltage of operation the surface leakage can be determined using the following relationships.

V_{CB1} = voltage of operation

V_{CB2} = voltage at which I_S is specified

$$I_{s1} = \frac{V_{CB1}}{V_{CB2}}\, I_S\,\mu a$$ surface leakage component at voltage of operation

The conversion factor to determine I_{CBO} at elevated temperatures using the rule of thumb is

$$\text{Letting } \beta = \frac{T_J - 25^\circ C}{10}$$

$$\text{Conversion factor } \phi = 2^{\beta}$$

The total I_{CBO_1} at an elevated junction temperature T_J and voltage V_{CB_1} is therefore

$$I_{CBO_1\ max} = I_{s1}\,\frac{\phi}{2} + I_T\,\phi$$

To insure reliable operation of the circuit, an additional safety factor should be included to account for aging effects on the transistor. An increase in the calculated value of 40 per cent should insure reliable operation.

Bias Stabilization Techniques

The usual method for expressing the stability of the biasing method chosen is in terms of a current stability factor S_I, and a voltage stability factor S_V.[1] The definitions of the two stability factors are as follows.

$$S_I = \frac{\Delta I_E}{\Delta I_{CBO}} \qquad \text{current stability factor} \qquad (261)$$

$$S_V = \frac{\Delta V_{CB}}{\Delta I_{CBO}} \qquad \text{voltage stability factor} \qquad (262)$$

Figure 38 gives the basic stabilization circuit and the current and voltage stability factors pertaining to the circuit.

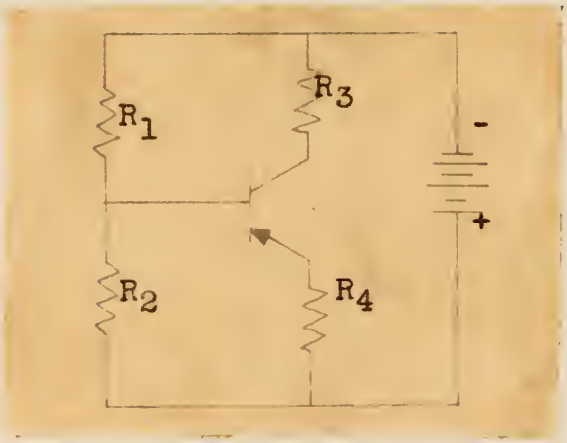


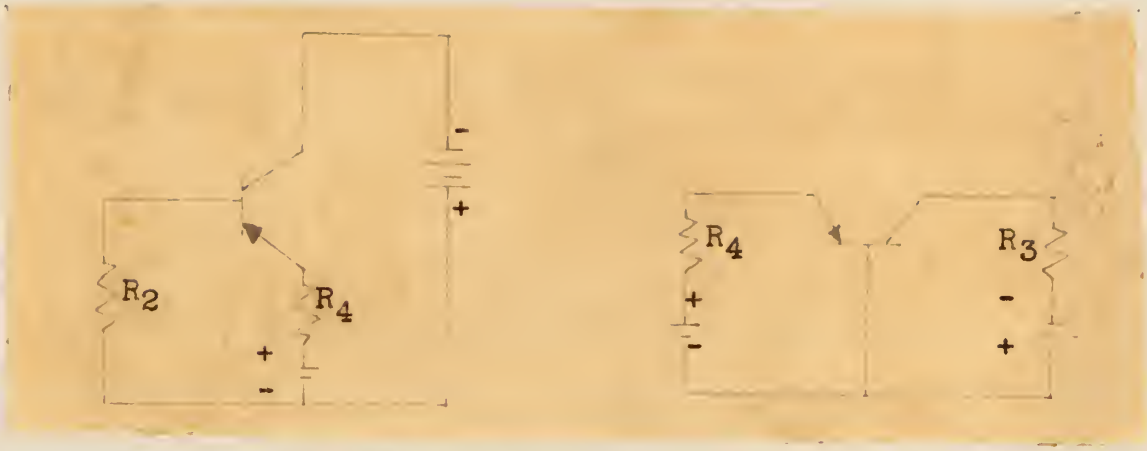
Fig. 38. General transistor circuit with current and voltage stability factors.

$$S_I = \frac{1/R_4}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1/(1+B)}{R_4}\right)} \qquad (263)$$

$$S_V = -\left(S_I R_4 + R_3 \left[1 + \frac{B}{1+B} S_I\right]\right) \qquad (264)$$

[1] TM 11-690, Department of the Army Technical Manual, "Basic Theory and Application of Transistors," March, 1959.

The stability factors given in Fig. 38 are applicable to any bias configuration that can be derived from Fig. 38, the requirement being that any resistor deleted or shorted must be replaced by a zero or infinity, respectively, in the stability equation. As an example, consider the common collector (emitter follower) amplifier and the common base amplifier shown in Fig. 39.



(a) Common collector (b) Common base

Fig. 39. Common collector and common base configuration.

For the common collector configuration $R_1 = \infty$ and $R_3 = 0$, so the stability equations are

$$S_I = \frac{1/R_4}{\left(\frac{1}{R_2} + \frac{1/(1+B)}{R_4}\right)} \tag{265}$$

$$S_V = -S_I \, R_4 \tag{266}$$

For the common base configuration $R_1 = 0$ and $R_2 = 0$, so the stability equations are

$$S_I = 0 \tag{267}$$

$$S_V = -R_3 \tag{268}$$

It is obvious from Fig. 38 that to obtain good stability the emitter resistor (R_4) should be large compared to the effective base resistance (parallel combination of R_1 and R_2). Also, as is illustrated by the common base example, the optimum method of bias would be to bias the transistor in such a manner that the d-c resistance to ground is zero in the base current path. This can be accomplished for the common emitter case by using a transformer input illustrated in Fig. 40.

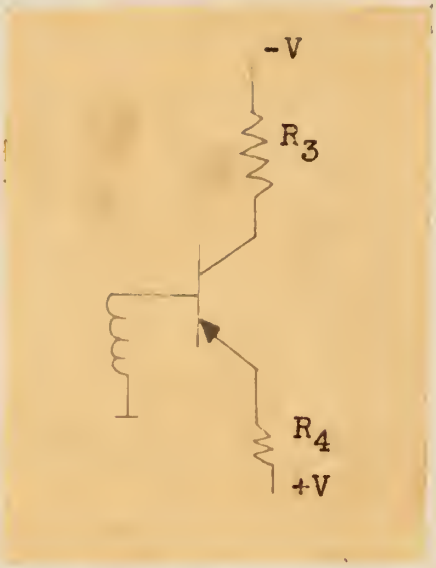


Fig. 40. Bias arrangement using a transformer input.

Since the stability factors are inversely proportional to a parameter that varies in a nonlinear fashion with temperature (I_{CBO}), it follows that compensation could be achieved by using biasing parameters that vary in a similar manner. Figures 41 and 42 illustrate the use of two elements that are nonlinear with temperature which can be used to bias stabilize a transistor circuit.

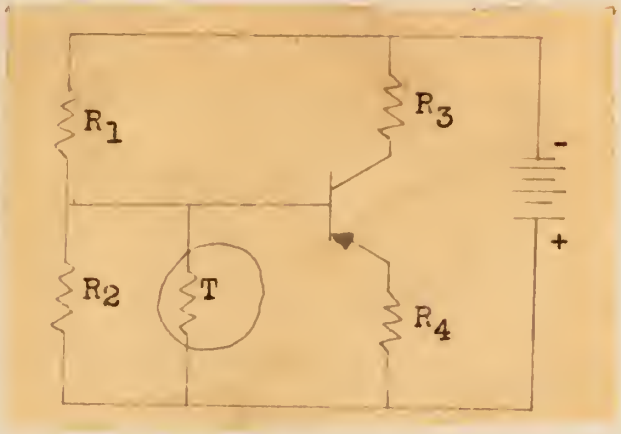


Fig. 41. Thermistor control of base bias voltage to compensate for deviation in bias voltage due to I_{CBO}.

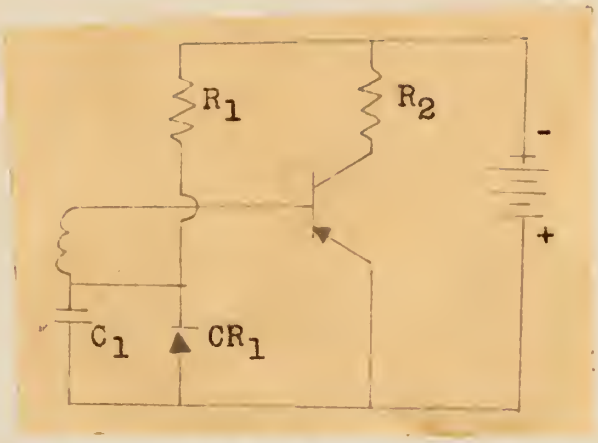


Fig. 42. Forward biased junction diode for compensation of variations of emitter-base junction resistance.

Since the emitter-resistor-base potentiometer bias method is used more extensively than the other methods discussed, it will be given further consideration. Figure 43 shows the emitter-resistor-base potentiometer bias method for the three basic amplifier configurations.

Usually the criterion for adequate d-c stability is the spread in emitter bias current that can be tolerated consistent with the design requirements of the circuit. For example, R_e in

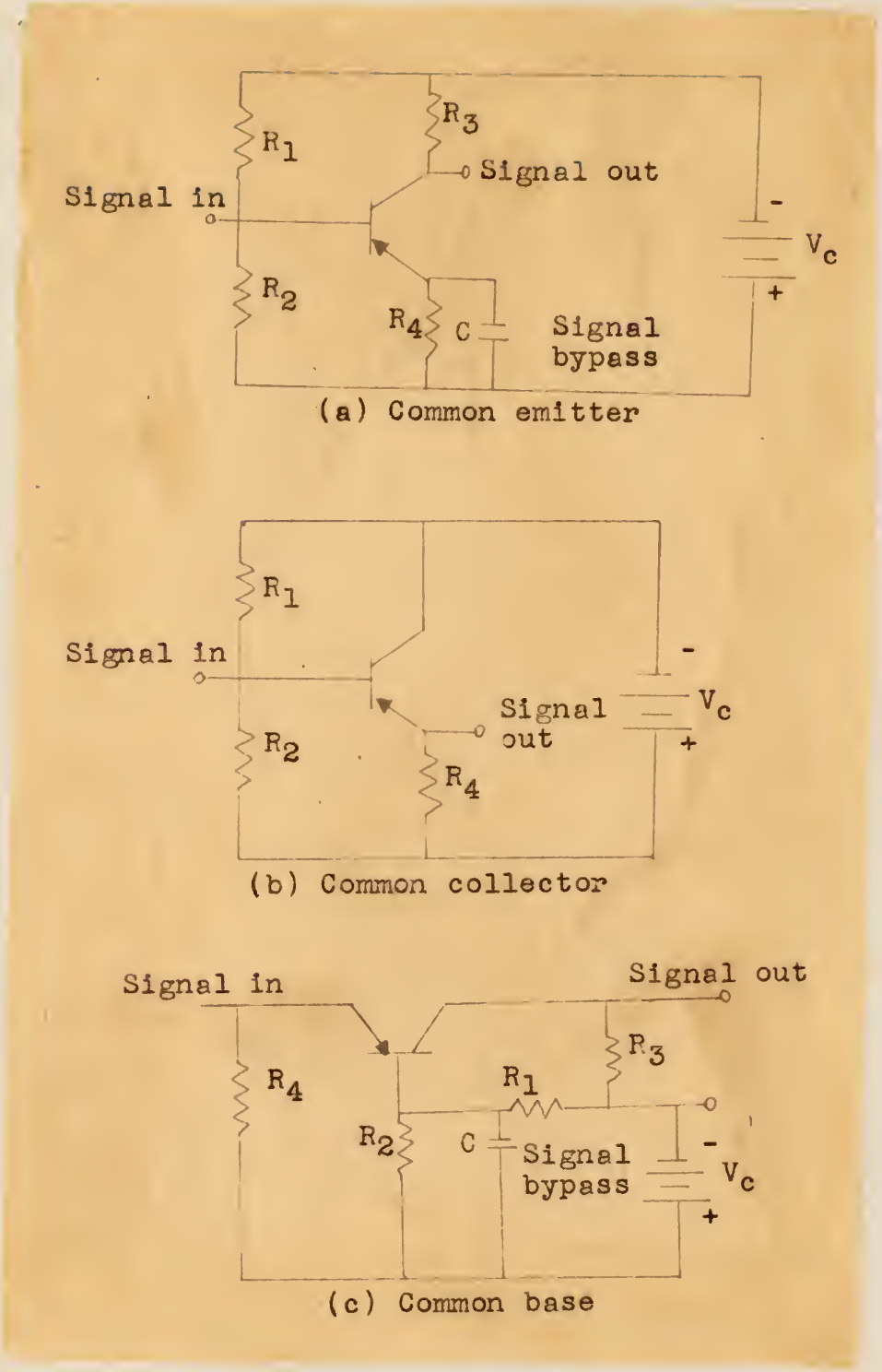


Fig. 3. Emitter-resistor-base potentiometer bias circuits for the three transistor amplifier configurations.

all the equivalent circuits discussed is inversely proportional to the emitter bias current. If R_e varies due to a variation of emitter bias current over a certain temperature range, the input impedance, voltage gain, etc., also vary. (For example, see Eqs. (38), (39), (40), and (41)).

In the usual case it is base bleeder resistances R_1 and R_2, of Fig. 43, that must be determined for the desired degree of emitter current stabilization. This is true since the values of R_3 and R_4 are usually dictated by circuit consideration such as the available bias supply voltage and the desired operating point. In the common emitter and common collector configuration the parallel combination of R_1 and R_2, $\left(\frac{R_1R_2}{R_1 + R_2}\right)$, represents an equivalent resistance to ground that a signal input sees, so it should be large compared to the input impedance of the transistor. Conversely, $\left(\frac{R_1R_2}{R_1 + R_2}\right)$ should be small compared to R_4 for good stability. In view of the above considerations it is desirable to determine the optimum relationship between R_1, R_2, and R_4 for adequate emitter current stability.

For the common base configuration it is R_4 that represents a shunt to the signal input.

Figure 44 will be used to determine the proper values of R_1 and R_2 for a given tolerance of I_e over the temperature range. It is assumed that V_c, R_3, and R_4 have been predetermined.

The symbols used in Fig. 44 are defined as follows.

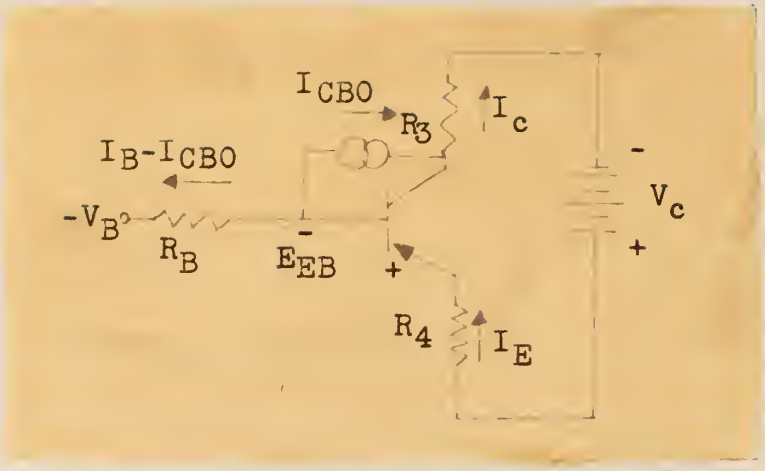


Fig. 44. Circuit for determining R_B.

V_B = The d-c base bias voltage which is negative with respect to the emitter and positive with respect to the collector for the PNP transistor illustrated. In terms of the parameters of Fig. 43, $V_B = \frac{V_c R_2}{R_1 + R_2}$.

V_C = The d-c collector bias voltage which is negative with respect to the emitter for the PNP transistor illustrated.

I_B = The d-c base bias current.

I_{CBO} = The base to collector leakage current.

I_E = The d-c emitter bias current.

I_C = The d-c collector bias current.

R_3 = The collector bias and/or load resistance.

R_4 = The emitter bias resistor.

R_B = Parallel equivalent of R_1 and R_2 of Fig. 43

$$(R_B = \frac{R_1 R_2}{R_1 + R_2}).$$

It has been previously shown that

$$I_B = \frac{I_E}{1 + B} \tag{269}$$

From Fig. 44

$$(I_B - I_{CBO})\, R_B + E_{EB} + I_E R_E = V_B \tag{270}$$

$$\frac{I_E}{1 + B} R_B - I_{CBO}\, R_B + E_{EB} + I_E R_E = V_B \tag{271}$$

$$I_E = \frac{I_{CBO}\, R_B - E_{EB} + V_B}{\frac{R_B}{1 + B} + R_E} \tag{272}$$

The maximum emitter current will occur when I_{CBO} is maximum, B is maximum, and E_{EB} is minimum.

$$I_E \text{ max} = \frac{I_{CBO}\,(\text{max})\, R_B - E_{EB}\,(\text{min}) + V_B}{\frac{R_B}{1 + B\,(\text{max})} + R_E} \tag{273}$$

Therefore

$$I_E \text{ min} = \frac{R_B I_{CBO}\,(\text{min}) - E_{EB}\,(\text{max}) + V_B}{\frac{R_B}{1 + B\,(\text{min})} + R_E} \tag{274}$$

$$V_B = I_E\,(\text{min}) \left(\frac{R_B}{1 + B\,(\text{min})} + R_E \right) - I_{CBO}\,(\text{min})\, R_B + E_{EB}\,(\text{min}) \tag{275}$$

$$V_B = I_E\,(\text{max}) \left(\frac{R_B}{1 + B\,(\text{max})} + R_E \right) - I_{CBO}\,(\text{max})\, R_B + E_{EB}\,(\text{min}) \tag{276}$$

$$R_B \left(- \frac{I_E\,(\text{max})}{1 + B\,(\text{max})} + \frac{I_E\,(\text{min})}{1 + B\,(\text{min})} + I_{CBO}\,(\text{max}) - I_{CBO}\,(\text{min}) \right)$$

$$= I_E\,(\text{max})\, R_E - I_E\,(\text{min})\, R_E + E_{EB}\,(\text{min}) - E_{EB}\,(\text{max}) \tag{277}$$

Assuming $I_{CBO}\,(\text{min}) = 0$ and solving for R_B yields

$$R_B = \frac{\left(I_E\ (max) - I_E\ (min)\right)R_E + E_{EB}\ (min) - E_{EB}\ (max)}{I_{CBO}\ (max) - \frac{I_E\ (max)}{1 + B\ (max)} + \frac{I_E\ (min)}{1 + B\ (min)}} \tag{278}$$

Solving for R_1 and R_2 yields

$$R_1 = R_B \frac{V_C}{V_B} \tag{279}$$

$$R_2 = \frac{R_1 V_B}{V_C - V_B} \tag{280}$$

Thus for a given tolerable variation of emitter current and worst-case variations of B, I_{CBO}, and E_{EB}, the values of the bleeder resistors R_1 and R_2 can be determined.

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TRANSISTOR CIRCUIT DESIGN

by

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This report presents a simplified equivalent circuit for the transistor which is useful at least as a first approximation for deriving the pertinent equations which describe the transistor. The equivalent circuit developed is presented in the hybrid π form since it is analogous to the familiar conventional equivalent circuit for the vacuum tube. The hybrid π circuit is derived directly from the bridged-T equivalent circuit which is described extensively in the literature on transistors. This report is limited to the discussion of small signal (linear) applications of the transistor.

Equations are derived which relate the equivalent circuit elements to the data presented on most commercial transistor data sheets. By utilizing these relationships it is possible to approximate the values of the equivalent circuit parameters from a minimum amount of data. Once the equivalent circuit is developed the operation of the transistor can be approximately predicted over its useful frequency range.

Transistor matrices for the transistor in the three basic amplifier configurations are derived from the equivalent circuit. The basic configurations are the common emitter, common base, and common collector configurations. The transfer matrices are used to derive the equations which describe the transistor when used as an amplifier in the three basic configurations. The descriptive equations include the input impedance, output impedance, current gain, and voltage gain. The equivalent circuit is simplified for both low and high frequencies and the transfer matrix and equations are presented for these conditions.

Equations are derived describing the transistor amplifier when voltage or current feedback is employed. For sufficiently high gain units the amplifier can be made independent of parameter variations by using feedback.

The figure of merit for a transistor is derived from the equivalent circuit. The figure of merit is analogous to the gain bandwidth product for a vacuum tube. The frequency at which the power gain of a matched transistor amplifier is unity is defined as the figure of merit.

Since the transistor is a bilateral device possible instability occurs over a relatively wide frequency range. Two methods of stabilization are discussed. The transistor amplifier can be stabilized by neutralizing techniques. Using the equivalent circuit the necessary values of the neutralizing components are derived. Neutralization is the optimum method since the amplifier can be conjugately matched at the input and output for maximum power gain.

The second method of stabilizing a transistor amplifier is to deliberately mismatch the input and/or output resistances. This method results in a loss of power gain, but is simpler and more predictable than the neutralizing technique. The equation for the maximum value of load resistance which will insure absolute stability is derived. The equation specifies the maximum value of load resistance in terms of the equivalent circuit parameters.

Above a certain frequency the transistor will be unconditionally stable regardless of the terminating impedances. The

approximate value of this frequency is derived in terms of the parameters of the basic equivalent circuit.

The report is concluded with a brief discussion of conventional biasing techniques. The various forms of leakage currents are discussed, including a method of determining I_{CBO} at elevated temperatures. Since the emitter-base-potentiometer method of biasing a transistor is the most common method used, it is discussed in detail.