THE APPLICATION OF LOCALLY OPTIMAL CONTROL WITH DIGITAL COMPENSATION TO A NATURALLY UNSTABLE SYSTEM

by

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CHAPTER I

INTRODUCTION

The problem of balancing a pencil on the end of one's finger is not unlike the problem of controlling the attitude of a missile during the initial stage of launch. This problem is the classic and intriguing problem of the inverted pendulum mounted on a cart. The cart must be moved so that the pendulum is always maintained in an upright position.

In order to make the inverted pendulum remain in the upright position, extremely accurate control is needed. Digital control provides a high degree of accuracy in sensing, computation, and control, and is used in this study. It has been thirty-one years since the first commercial electronic digital computer was built (Univac I, 1951) (1)*. The increase in usage of the digital computer has had an important impact in the whole society, especially in the field of engineering. The latest computer revolution has been the result of very large scale integration techniques (VLSI), in which more than ten thousand electronic elements are put into a single chip. The microprocessor or microcomputer, which was invented eleven years ago, is now finding new applications everyday, and the control engineer has been challenged to utilize these software programmable devices for controlling systems.

The objective of this research is to apply the digital control method to generate a real-time control program for controlling a naturally unstable system. An inverted pendulum mounted on a movable cart is chosen as the naturally unstable system.

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*Number in parentheses refers to reference in part X.

A four wheeled, light weight aluminum cart (size 24 inch by 8 inch) was available for this project. An inverted pendulum was mounted to the top of the cart by a pair of ball bearings which constrained the motion of the pendulum to one vertical plane. The 8.25 inch diameter wheels of the cart may be driven by an armature controlled dc servo motor through a 19.7 to 1 speed reducing belt drive system. The motion of the cart is in the plane of the pendulum motion. A micro torque potentiometer is used to measure the angular position of the pendulum and a dc tachometer measures the speed of the servo motor (and hence the speed of the cart). An operational amplifier connected as an integrator provides a signal proportional to the displacement of the cart from the tachometer signal. A dc power amplifier is used to provide power to the control signal to drive the armature of the servo motor. The photograph of the cart-pendulum system used in this research is presented in Figure 1-1, as shown in the next page.

A microprocessor was programmed to control the motion of the cart. Signals proportional to the angular displacement of the pendulum and a weighted sum of the velocity and displacement of the cart are sampled periodically and provided the basis for computing the control signal to drive the motor. The program stores the data of the pendulum position in specific memory locations, and displays the speed of the cart and the pendulum position on a CRT.

Objective

The objective of the work present in this thesis is to investigate problems associated with the implementation of a microcomputer based real-time controller of an inverted pendulum on a motor driven cart.

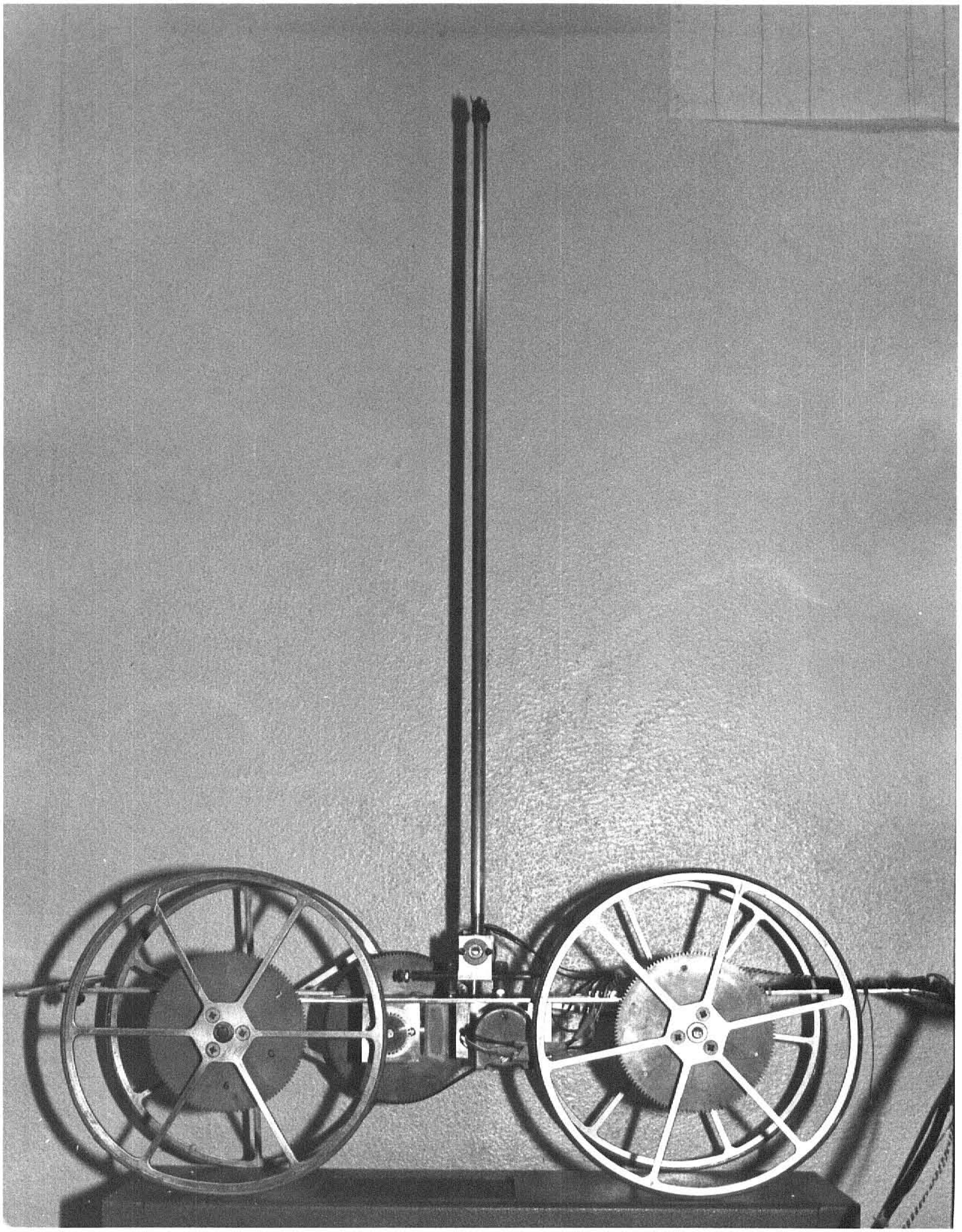


Figure 1-1, The Cart Pendulum System

The study investigates the application of a locally optimal control technique with digital compensation. Furthermore, observations are made on the effect of the digital computer time lag on the stability of the system.

The sampling period of 10 milli-second was chosen, and a programmable timer is used to time the sampling process.

Introduction to Sampled-data Systems

Sampled-data, or discrete-time systems are dynamic systems in which one or more variables can change only at discrete instants of time. Sampled-data systems arise in practice whenever the measurements necessary for control are obtained in an intermittent fashion, or when a controller or computer is time shared by several processes so that a control signal is sent out to each process only periodically or whenever a digital computer is used to perform computation necessary for control.

The sampled instant is the time at which some physical measurements are performed. The time interval between sampled instants must be short compared to the speed of response of the system and usually is set to be at least 10 times less than the natural period of the system that is controlled.

A sampled-data system may consist of a digital computer, analog to digital converters, digital to analog converters, sensors, actuators and the system being controlled. The analog signals are converted into digital signals by the analog to digital converters. The digital computer receives the digital values, performs specified computations, and produces digital control signals. The digital control signals are converted to analog signals by digital to analog converters.

The system is controlled by driving the actuators with the analog control signals.

Preview

Analysis begins by developing mathematical models (in Laplace form) that describe the actual system as presented in Chapter II. Digital models are then obtained from these Laplace equations by using Z-transform techniques as detailed in Chapter III. Based on these digital models, an optimal control law is formulated. The optimal control law and an analysis of the stability of the system are presented in Chapter IV. A computer simulation, using the equations of the digital models and the optimal controller, is discussed in Chapter V. The software logic of the real-time control program is presented in Chapter VI, and the experimental procedures are detailed in Chapter VII. The results of the experiment are presented in Chapter VIII, and conclusion and recommendation are presented in Chapter IX.

CHAPTER II

MATHEMATICAL MODELING

An important part of control system analysis is mathematical modeling. During the modeling process, equations are developed which describe the behaviour of each system element and also equations which describe the interconnections of these elements. For complex systems, the development of these equations may be tedious. Although assumptions may be thought of as leading to less accurate results, with properly made assumptions one can still predict the performance of the system with little loss in accuracy. The objective of mathematical modeling is to obtain the simplest mathematical description that adequately predicts the response of the system to all anticipated inputs.

Modeling

The system consisting of an inverted pendulum on a motor driven cart was divided into three models. These models are shown in Figure 2-1. The first model, $G_1(s)$, is the transfer function of the motor and cart with a feedback signal from the tachometer. $G_2(s)$ is the transfer function that describes the behaviour of the inverted pendulum mounted on the moving cart. The third model, $G_3(s)$, is the transfer function of the integrator. H(S) is the transfer function of a zero-order-hold which represents the action of the latch and the digital to analog converter. The value which results from the computation, U*, is periodically placed in a latch which drives a digital to analog converter. Each time the computation is performed, a new value is placed in the latch. U represents the analog signal which is output by the digital to analog converter. The signals V_t, V_x, and V_p are the

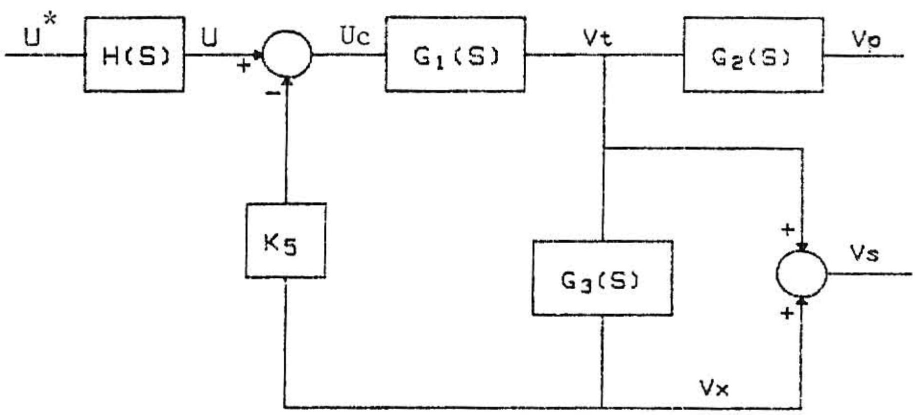
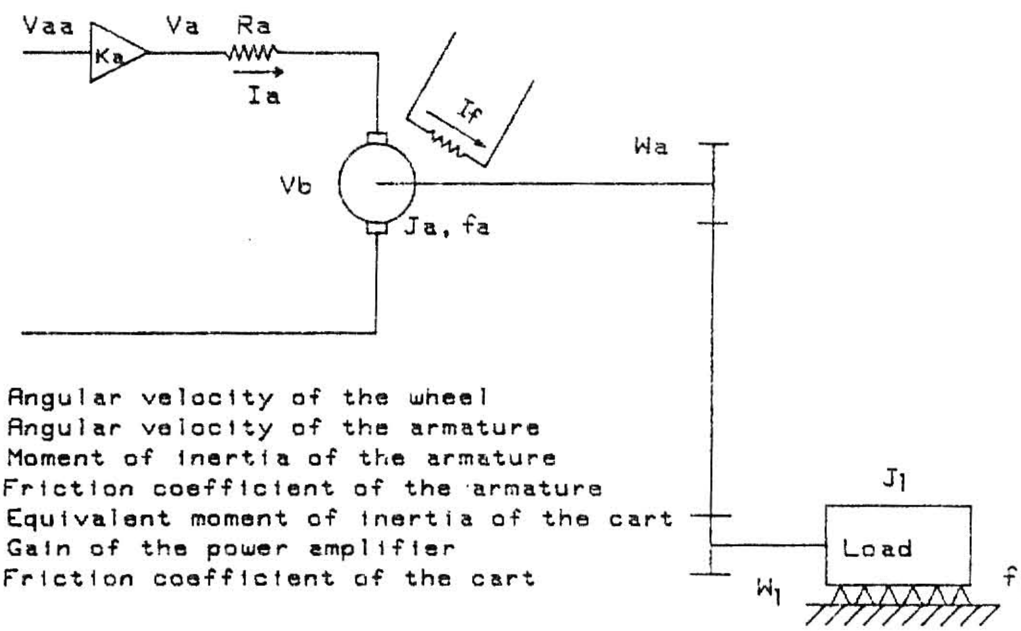


Figure 2-1, The Physical System



W_1 = Angular velocity of the wheel
Wa = Angular velocity of the armature
Ja = Moment of inertia of the armature
fa = Friction coefficient of the armature
J_1 = Equivalent moment of inertia of the cart
Ka = Gain of the power amplifier
f_1 = Friction coefficient of the cart

Figure 2-2, The Model of DC Motor with Load signals out of the tachometer, integrator and potentiometer respectively. The symbol V_s represents the sum of the signals V_t and V_x. K_5 represents a gain which produces a feedback signal that is proportional to the signal V_x.

Modeling of a Motor

Figure 2-2 shows a simple model of an armature controlled dc motor and the transmission system of the cart. The second-order effects of the motor, such as hystersis and the voltage drop across the brushes, are neglected.

By applying Kirchhoff's voltage law,

$$V_a - V_b = I_a R_a \tag{2-1}$$

The torque developed by the motor, T_m, was assumed to be proportional to the armature current, I_a, as follows:

$$T_m = K_m I_a \tag{2-2}$$

The back electromotive force voltage, V_b, is proportional to the motor speed, W_a, therefore:

$$V_b = K_b W_a \tag{2-3}$$

The effects due to the elasticity of the transmission is small and negligible. The relation between the load torque and motor torque may be expressed as follows:

$$J_a \dot{W}_a + f_a W_a = T_m - T_{ga} \tag{2-4}$$

$$J_1 \dot{W}_1 + f_1 W_1 = T_{g1} \tag{2-5}$$

where T_{ga} is the torque that applies to the armature and T_{g1} is the torque that applies to the load.

The T_{gl} is proportional to the T_{ga}, and may be expressed as:

$$T_{gl} = K_k T_{ga} \tag{2-6}$$

where K_k is the gear ratio of the transmission.

The angular velocity of the cart's wheel, W_l, is proportional to the angular velocity of the armature, W_a.

$$W_l = W_a / K_k \tag{2-7}$$

In order to improve the performance of the motor drive system the tachometer signal is amplified and feed-back to the input of the power amplifier. $G_0(s)$ is the transfer function that describes the motor without the feedback from tachometer. Figure 2-3 shows the block diagram of the model of $G_1(s)$. The relationship between $G_1(s)$ and $G_0(s)$ may be expressed as:

$$G_1(s) = \frac{V_t(s)}{Uc(s)} = \frac{K_{aa} K_a K_t\ G_0(s)}{1 + K_{aa} K_{bb} K_a K_t G_0(s)} \tag{2-8}$$

where K_{aa} and K_{bb} are the gains of the operational amplifiers, and K_t is the gain of the tachometer.

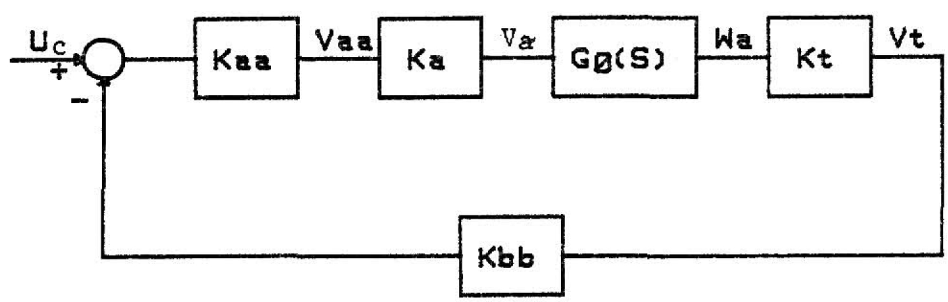


Figure 2-3, The Model of $G_1(s)$

Taking the Laplace transformation of the above equations, substituting Equations (2-1), (2-2), (2-3), (2-6), and (2-7) into and combining Equations(2-4) and (2-5), yields the transfer function of $G_0(s)$

$$G_0(s) = \frac{W_a(s)}{V_a(s)} = \frac{K_j}{(s + K_h)} \qquad (2\text{-}9)$$

where

$$K_j = K_m/[R_a(J_a + J_1/K_k^2)]$$

$$K_h = (f_a + f_1/K_k^2 + K_m K_b/R_a)/(J_a + J_1/K_k^2)$$

Substituting Equation (2-9) into (2-8), yields

$$G_1(s) = \frac{V_t(s)}{Uc(s)} = \frac{K_g}{s + (K_h + K_{bb}K_g)} \qquad (2\text{-}10)$$

where

$$K_g = K_{aa}K_aK_tK_j$$

The gains of the operational amplifiers K_{aa}, and K_{bb} were set to 2 and 4.7. The gain of the power amplifier, K_a, is 5. The gear ratio of the transmission K_k is 19.7 revolutions of the motor/revolution of the wheels. The gain of the tachometer, K_t, is 0.45 volts/revolution of the motor/second. Based on the above information, the root of the Equation (2-10) is at the location far away to the left of the imaginary axis. Hence, the transfer function, $G_1(s)$, may be expressed in the simpler form:

$$G_1(s) = K_g/(K_h + K_{bb}K_g) = K_1 \qquad (2\text{-}11)$$

An experiment was conducted to obtain the value of the gain, K_1. This value is the ratio of the output voltage of the tachometer, V_t, to the input voltage, Uc. Based on this experiment, the gain, K_1, was obtained

$$G_1(s) = K_1 = 0.89$$

Modeling of an Inverted Pendulum Mounted on a Moving Cart

Figure 2-4 shows an inverted pendulum mounted on a cart. The pendulum has length "d" and mass "m". The cart, of mass M, moves with a velocity V. The mass of the cart is much greater than that of the pendulum.

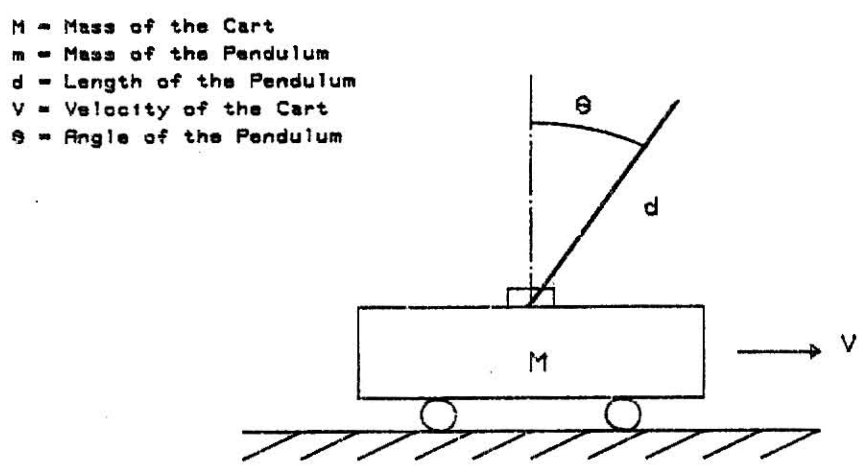


Figure 2-4
Schematic Representation of an Inverted Pendulum on the Cart

The Lagrange method is used to obtain the equation of motion. The total kinetic energy, KE, is

$$KE = \tfrac{1}{2}MV^2 + \tfrac{1}{2}I_g\dot{\theta}^2 + \tfrac{1}{2}mV_c^2 \qquad (2\text{-}12)$$

where $V_c^2 = V^2 + d^2\dot{\theta}^2/4 + dV\dot{\theta}\ \mathrm{Cos}\ \theta$, and $I_g = md^2/12$.

The total potential energy, PE, is

$$PE = \tfrac{1}{2} mdg \cos\theta \tag{2-13}$$

The Lagrange equation is

$$\frac{d}{dt}\left(\frac{\partial L}{\partial \dot{\theta}}\right) - \frac{\partial L}{\partial \theta} = 0 \tag{2-14}$$

where L = KE - PE

Substituting KE and PE into Equation (2-14), assuming small θ, and linearizing, yields

$$\dot{V} + 2d\ddot{\theta}/3 - g\theta = 0 \tag{2-15}$$

Rearranging Equation (2-15) and taking the Laplace transformation, yields,

$$\frac{\theta(s)}{V(s)} = \frac{-s}{(2ds^2/3 - g)} = \frac{K_f s}{s^2 - b^2} \tag{2-16}$$

where $K_f = -3/(2d)$, and $b^2 = (3g)/(2d)$.

The voltage out of the potentiometer, V_p, is proportional to the angular displacement of the pendulum, θ.

$$V_p(s) = K_p \theta(s) \tag{2-17}$$

where K_p is the gain of the potentiometer.

The output voltage of the tachometer, V_t, is proportional to the velocity of the cart, V.

$$V_t(s) = (K_t K_k / 2\pi r) V(s) \tag{2-18}$$

where r is the radius of the cart's wheel.

Substituting Equations (2-17) and (2-18) into (2-16), yields the transfer function of the second model, $G_2(s)$, as shown below.

$$G_2(s) = \frac{V_p(s)}{V_t(s)} = \frac{K_2 s}{s^2 - b^2} \tag{2-19}$$

where $K_2 = K_p K_f r/(K_t K_k)$.

The length of the pendulum, d, is 2 feet, the gain of the potentiometer is 5.76 volt/radian, hence

$$K_2 = 1.04.$$

The transfer function of the integrator, $G_3(s)$, may be expressed as:

$$G_3(s) = \frac{K_3}{s} \tag{2-20}$$

where K_3 is the gain of the integrator.

CHAPTER III

DIGITAL MODELING

Digital models are employed for the purpose of developing the control equations. In order to obtain the digital models, the Z-transform technique is used. The introduction of the Z-transform technique is provided in the next section, and the development of the digital models is presented afterwards.

Z-Transform

The analysis of sampled-data systems can be carried out by using the Z-transform approach. The Z-transform approach has the same relationship to linear time-invariant sampled-data systems as the Laplace transform approach bears to linear time-invariant continuous time systems (2). The Z-transform technique has become the most widely used method for the analysis and synthesis of sampled-data systems.

To analyze sampled-data systems by the transfer function method, it is essential to know how to derive Z-transforms from time functions and Laplace functions for the building blocks or the components of a system.

The equations of the Z-transform can be obtained from Laplace equations by using the definition or a table of Z-transforms. From the Z-transform equations, recurrence equations can be found. In this research, these recurrence equations were used in the computer simulation and the real time control program.

Digital Modeling

Figure 3-1 shows the block diagram of the system. The blocks within the dashed-line represent the physical elements of the inverted

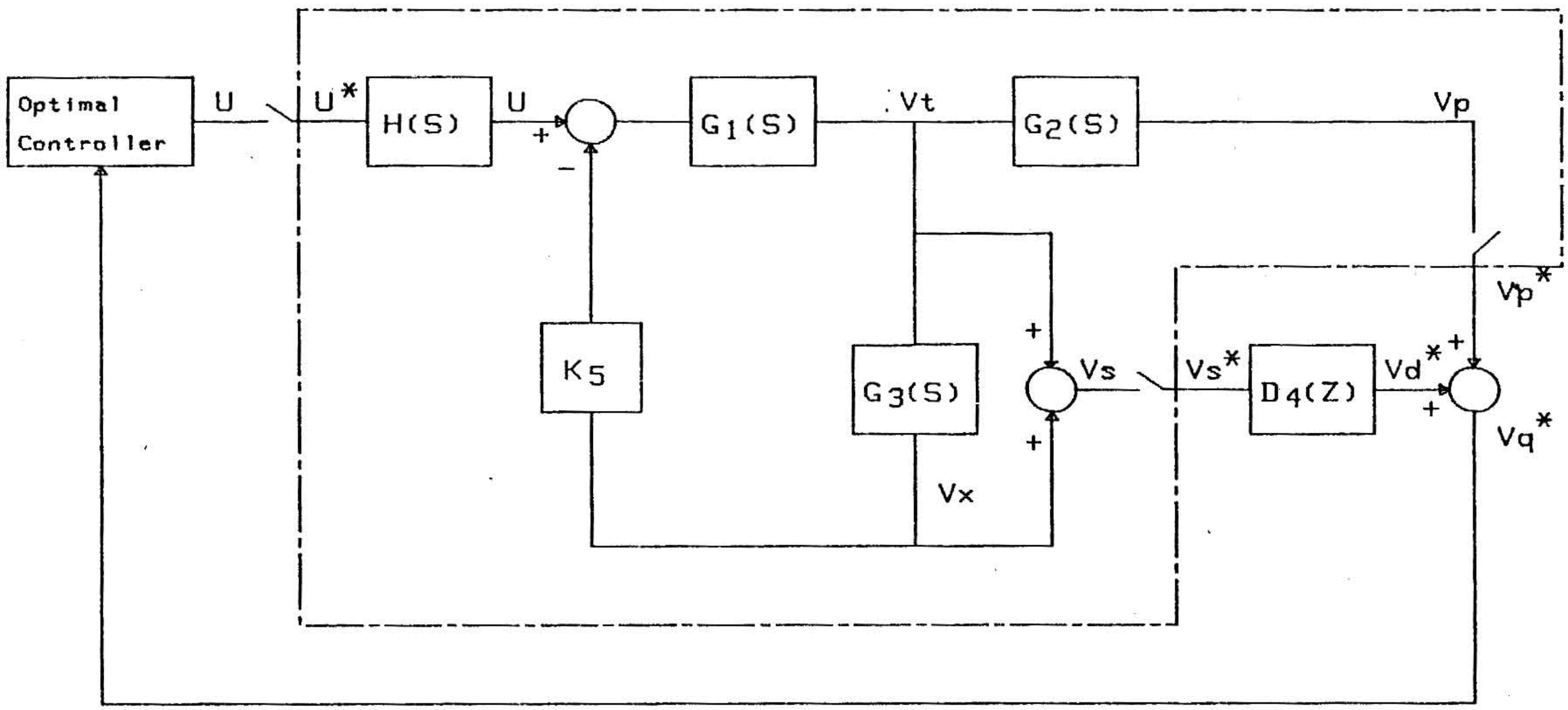


Figure 3-1, The Optimal Control System

pendulum system. The rest of the blocks represent computations carried out in the microprocessor. The analog signals V_s and V_p are sampled by the computer and provided the signals upon which the digital computations are performed. The two digital values, V_s^* and V_p^*, are produced by the analog to digital converter, and correspond to the signals V_s and V_p. $D_4(z)$ is the model of the digital compensator, which transfers the digital values V_s^* to V_d^*. The symbol V_q^* represents the sum of the digital values V_p^* and V_d^*. This digital value is fed to the optimal controller. Based on this value, the optimal controller produces a new control value, U^*, and places this control value in a latch in the digital to analog converter. The value U is the output of the digital to analog converter which controls the motion of the cart to balance the pendulum.

In order to develop the computer algorithms for the compensator D_4 and the optimal controller it is necessary to convert the Laplace models shown in Figure 3-1 to Z-transform models. Figure 3-2 shows the digital models $D_1(z)$, $D_2(z)$, $D_4(z)$, and the optimal controller. The digital model, $D_1(z)$, describes the relationship between the output signal from the potentiometer, V_p, and the control signal U.

$D_1(z)$ may be derived as follows:

$$\frac{V_p(s)}{U^*(s)} = \frac{H(s)G_1(s)G_2(s)}{1 + K_5G_1(s)G_3(s)} = \frac{K_1K_2s(1 - e^{-sT})}{(s + K_1K_3K_5)(s + b)(s - b)} \tag{3-1}$$

where

$$H(s) = \frac{1 - e^{-sT}}{s} \tag{3-2}$$

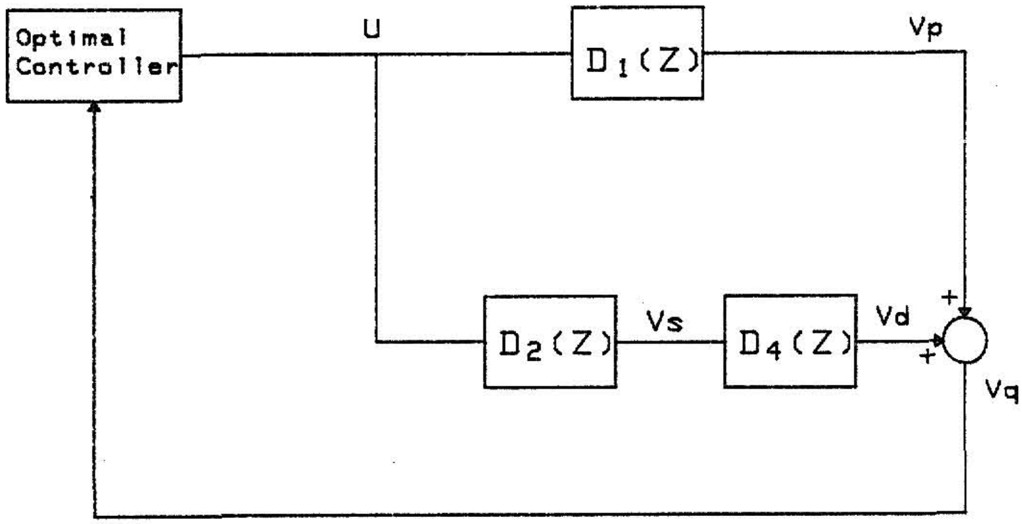


Figure 3-2

The Digital Models

Performing the Z-transform on Equation (3-1) results in

$$D_1(z) = \frac{V_p(z)}{U(z)} = K_{10} \left[\frac{(z + C_3)(z - 1)}{(z - e^{-aT})(z - e^{-bT})(z - e^{bT})} \right] \qquad (3\text{-}3)$$

$$K_{10} = K_1K_2A_3/2(a^2 - b^2)$$

$$a = K_1K_3K_5$$

$$b = 4.91$$

$$A_3 = (a + b)e^{-bT} + (a - b)e^{bT} - 2ae^{-aT}$$

$$B_3 = -2a + (a + b)e^{(b-a)T} + (a - b)e^{-(a+b)T}$$

$$C_3 = B_3/A_3$$

The relationship between the signal V_s and the control signal, U, is described by the digital model $D_2(z)$. The derivation of the digital model $D_2(z)$ is as follows:

$$\frac{V_s(s)}{V_t(s)} = 1 + G_3(s) = \frac{s + K_3}{s} \qquad (3\text{-}4)$$

$$\frac{V_t(s)}{U^*(s)} = \frac{K_1(1 - e^{-Ts})}{s + a} \qquad (3\text{-}5)$$

The product of Equations (3-4) and (3-5), yields

$$\frac{V_s(s)}{U^*(s)} = \frac{K_1(1 - e^{-Ts})(s + K_3)}{s(s + a)} \qquad (3\text{-}6)$$

Hence,

$$D_2(z) = \frac{V_s(z)}{U(z)} = \frac{K_1(z + D_3)}{z - e^{-aT}} \qquad (3\text{-}7)$$

where

$$D_3 = K_3(1 - e^{-aT})/a - 1$$

The digital model, $D_4(z)$, serves as a digital compensator. In order to derive the digital model, $D_4(z)$, the relationship between V_q and U is first developed.

The signal V_q^* is the sum of the signals V_d^* and V_p^*, hence

$$\frac{V_q(z)}{U(z)} = \frac{V_p(z)}{U(z)} + \frac{V_d(z)}{U(z)} \quad . \qquad (3\text{-}8)$$

Substituting Equations (3-7), and (3-3) into (3-8), yields

$$\frac{V_q(z)}{U(z)} = \frac{K_{10}(z + C_3)(z - 1)}{(z - e^{-aT})(z - e^{-bT})(z - e^{bT})} + \frac{K_1(z + D_3)}{z - e^{-aT}} D_4(z) \, . \qquad (3\text{-}9)$$

To simplify the Equation (3-9), the digital compensator, $D_4(z)$, is decided to have the form as shown below.

$$D_4(z) = \frac{V_d(z)}{V_s(z)} = \frac{K_{11}z + K_{12}}{(z - e^{-bT})(z - e^{bT})} \qquad (3\text{-}10)$$

The values of K_{11} and K_{12} may be adjusted in order to obtain stability. Substituting Equation (3-9) into (3-10), yields

$$\frac{V_q(z)}{U(z)} = \frac{P_1 z^2 + P_2 z + P_3}{(z - e^{-aT})(z - e^{-bT})(z - e^{bT})} \qquad (3\text{-}11)$$

where

$$P_1 = K_{10} + K_i K_{11}$$

$$P_2 = K_{10}(C_3 - 1) + K_i(D_3 K_{11} + K_{12})$$

$$P_3 = K_1 D_3 K_{12} - K_{10} C_3$$

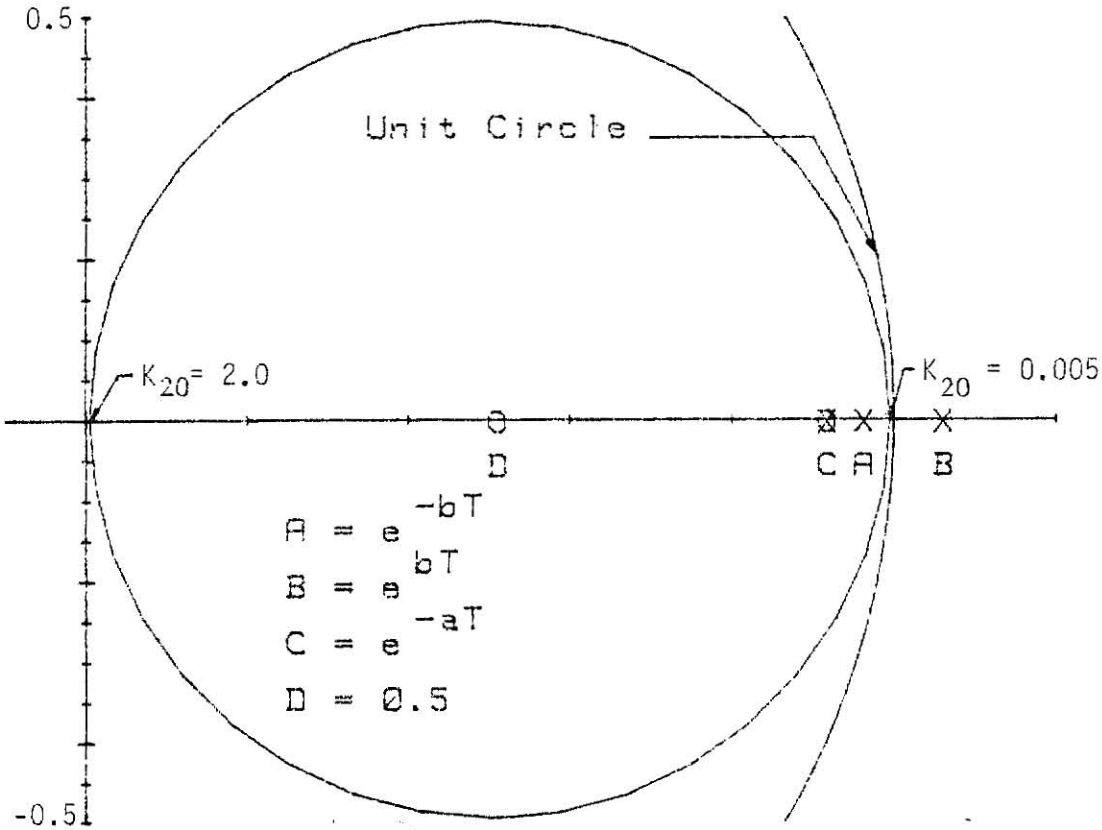


Figure 3-3, The Locations of the Roots

Figure 3-3 shows the location of the poles and zeroes of the Equation (3-11) In order to stablize the system it is desirable to cancel the pole $z = e^{-aT}$ by a zero, and place a zero at the location between the origin and the pole $z = e^{-bT}$, as shown in Figure 3-3. Assuming the zeroes are at .5 and e^{-aT}, Equation (3-11) may be rewritten as follows:

$$\frac{V_q(z)}{U(z)} = \frac{K_{20}(z - 0.5)}{(z - e^{-bT})(z - e^{bT})} \tag{3-12}$$

The characteristic equation is

$$z^2 - (e^{-bT} + e^{bT} - K_{20})z + (1 - \tfrac{1}{2}K_{20}) = 0 \tag{3-13}$$

The system is stable for $0.0048 < K_{20} < 2.668$. For $K_{20} = 2$ the roots are at $z = 0$ and $z = 0.0024$, hence,

$$P_1z^2 + P_2z + P_3 = 2(z - 0.5)(z - e^{-aT}) \tag{3-14}$$

therefore

$$P_1 = K_{10} + K_1K_{11} = 2 \tag{3-15}$$

$$P_2 = K_{10}(C_3 - 1) + K_1(D_3K_{11} + K_{12}) = -2(e^{-aT} + 0.5) \tag{3-16}$$

$$P_3 = K_1D_3K_{12} - K_{10}C_3 = e^{-aT} \tag{3-17}$$

In the case of $K_1 = 0.89$, $K_2 = 1.04$, $K_3 = 1$, and $K_5 = 1.1$, the coefficients of K_{11} and K_{12} are 2.2368 and -1.1133 respectively.

Based on Equation (3-3), the recurrence equation of the digital model, $D_1(z)$, is derived.

$$V_p(k + 1) = N_1V_p(k) + N_2V_p(k - 1) + N_3V_p(k - 2) + K_{10}U(k) + K_{10}N_4U(k - 1) + K_{10}N_5U(k - 2) \tag{3-18}$$

where

$$N_1 = e^{-bT} + e^{bT} + e^{aT}$$

$$N_2 = -1 - e^{-aT}(e^{bT} + e^{-bT})$$

$$N_3 = e^{-aT}$$

$$N_4 = C_3 - 1$$

$$N_5 = -C_3$$

From Equation (3-7), the recurrence equation of the digital model, $D_2(z)$, may be expressed as:

$$V_s(k) = M_1V_s(k - 1) + M_2U(k) + M_3U(k - 1) \tag{3-19}$$

where

$$M_1 = e^{-aT}$$

$$M_2 = K_1$$

$$M_3 = K_1D_3$$

The recurrence equation of the digital compensator is:

$$V_d(k + 1) = H_1V_d(k) + H_2V_d(k - 1) + H_3V_s(k) + H_4V_s(k - 1) \tag{3-20}$$

where

$$H_1 = e^{-bT} + e^{bT}$$

$$H_2 = -1$$

$$H_3 = K_{11}$$

$$H_4 = K_{12}$$

The recurrence equation of Equation (3-12) may be written as

$$V_q(k + 1) = E_1V_q(k) - V_q(k - 1) + K_{20}U(k) - \tfrac{1}{2}K_{20}U(k - 1) \tag{3-21}$$

where

$$E_1 = e^{bT} + e^{-bT}$$

The development of the optimal control law will be discussed in next chapter.

CHAPTER IV

THE OPTIMAL CONTROL

The concept of control system optimization comprises a selection of a performance index and a design which yields the optimal control system within limits imposed by physical constraints (3). The performance index is a function whose value indicates how well the actual performance of the system matches with the desired performance. An optimal control is defined as one that minimizes the performance index.

In this research, the performance of the system is evaluated by an index of the form

$$J = \tfrac{1}{2}\,[V_{qd}(k+1) - V_q(k+1)]^2 \qquad (4\text{-}1)$$

where V_{qd} is the desired output value. This would mean that the performance of the signal V_q at the instant $(k + 1)$ is decided.

The performance index is minimized by differentiating Equation (4-1) with respect to control signal U(k), and solving for U(k) after setting the differentiated equation to zero. Hence,

$$\frac{dJ}{dU(k)} = -[V_{qd}(k+1) - V_q(k+1)]\,\frac{\partial V_q(k+1)}{\partial U(k)} = 0 \qquad (4\text{-}2)$$

Equation (3-21) shows the relationship between V_q and U, hence,

$$\frac{\partial V_q(k+1)}{\partial U(k)} = K_{20} = 2 \qquad (4\text{-}3)$$

therefore, Equation (4-2) requires

$$V_{qd}(k+1) = V_q(k+1) \qquad (4\text{-}4)$$

Substituting Equation (4-4) into (3-21), the optimal control law can then be established as

$$U(k) = \tfrac{1}{2}[U(k-1) - E_1V_q(k) + V_q(k-1) + V_{dq}(k+1)] \qquad (4\text{-}5)$$

The Z-transform expression of Equation (4-5) is given by

$$U(z) = \left(\frac{z^2}{2z - 1}\right)V_{qd}(z) - \frac{(E_1 z - 1)}{2z - 1} V_q(z) \qquad (4\text{-}6)$$

Figure 4-1 shows the block diagram of the optimal control system.

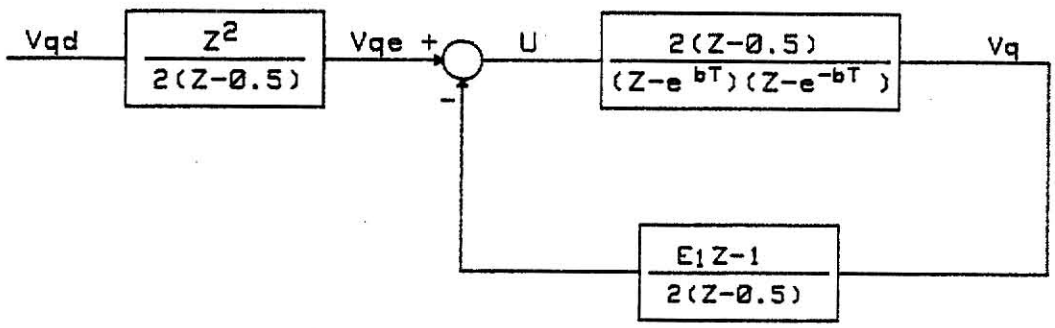


Figure 4-1, The Optimal Control System

The symbol V_{qd} represents the desired output value. The closed loop transfer function of the system shown in Figure 4-3 is

$$\frac{V_q(z)}{V_{qd}(z)} = \frac{\left[\frac{z^2}{2(z - 0.5)}\right]\left[\frac{2(z - 0.5)}{(z - e^{bT})(z - e^{-bT})}\right]}{1 + \frac{(E_1 z - 1)}{(z - e^{bT})(z - e^{-bT})}} = 1 \qquad (4\text{-}7)$$

which means that the actual output signal, V_q, always follows the desired output signal, V_{qd}, if there is no constraint on the control signal, U.

If the control signal is bounded, the output signal may follow the desired output, which depends on the initial condition of V_q and the rate at which the desired output signal varies with its value.

To analyze the effects of the bounded control signal on the stability of the system, a gain, K_{eq}, is added to the system as shown in Figure 4-2

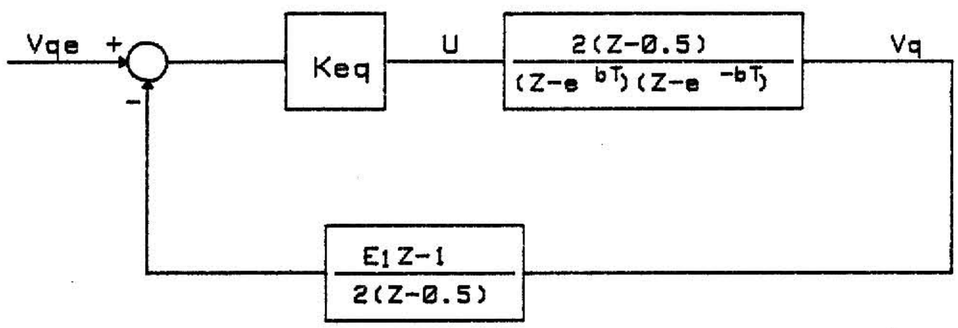


Figure 4-2, The Optimal Control System with the Gain, K_{eq}

The stability of the system can be determined from the locations of the roots of the characteristic equation.

$$z^2 + E_1(K_{eq} - 1)z + (1 - K_{eq}) = 0 \qquad (4\text{-}8)$$

The bilinear transformation maps the unit circle of the z-plane into the entire left half of the r plane, with the transformation, the Routh stability criterion may be applied to the polynomial in r in the same manner as continuous-time systems. The definition of the bilinear transformation is

$$z = \frac{r + 1}{r - 1} \qquad (4\text{-}9)$$

Substituting Equation (4-9) into (4-8), yields

$$s_1 r^2 + s_2 r + s_3 = 0 \qquad (4\text{-}10)$$

where

$$s_1 = 2 - K_{eq} - E_1(K_{eq} - 1)$$

$$s_2 = 2K_{eq}$$

$$s_3 = 2 - K_{eq}$$

The Routh array of Equation (4-10) is:

$$\begin{array}{c|cc} r^2 & s_1 & s_3 \\ r & s_2 & \\ r^0 & s_3 & \end{array}$$

To stabilize the system, it is necessary and sufficient that s_1, s_2, and s_3 be positive. Hence, the following conditions have to be satisfied.

1) $K_{eq} > 0$

2) $K_{eq} < 2$

3) $K_{eq} < (2 + E_1)/(1 + E_1)$

If all the above three conditions are satisfied, the system will be stable, but the actual output signal, V_q, may not be identical with the desired output.

If the initial condition or the desired output is large, the system will become unstable when the control signal is bounded.

In this research, the desired output signal, V_{qd}, is set to zero, in order to minimize the signals of the potentiometer, V_p, and the tachometer, V_t. This would mean that the angular displacement of the pendulum, the velocity and the displacement of the cart are minimized.

CHAPTER V

SIMULATION

When a model is available for a component or system, a computer can be utilized to investigate the behavior of the system. A computer model of a system in a mathematical form suitable for demonstrating the system's behavior may be utilized to investigate various designs of a planned system without actually building the system itself (4). A computer simulation uses a model and the actual conditions of the system being modeled and actual input commands to which the system will be subjected. If a model and the simulation are reliably accurate, the system performance can be observed under a variety of conditions. A system may be simulated using analog or digital computers. In this research, a digital computer simulation is used.

Simulation

A computer simulation was done before running the physical experiment. This simulation is based on the digital models shown in Figure 3-2. The instantaneous computation of the control signal, U, after measuring the signals V_p and V_d is assumed.

In this simulation, the time delay due to the computation and sensing in the real system is not taken into account.

In Figure 3-2, a control signal, U, is produced by the optimal controller. This signal is sent to digital models $D_1(z)$ and $D_2(z)$ and which produce signals V_p and V_s respectively. The signal V_s is then sent to digital compensator, $D_4(z)$. V_d is the signal produced by the digital compensator $D_4(z)$. The sum of the signals V_p and V_d is then fed back to the optimal controller. The optimal controller receives this feedback signal, computes, and produces a new control signal, U.

The recurrence equations of the digital models $D_1(z)$, $D_2(z)$, $D_4(z)$, and the optimal controller are presented in Equations (3-18), (3-19), (3-20), and (4-5) respectively.

In the computer simulation program, the saturation condition of the control signal and the limitation on the angle of the pendulum have been taken into account.

The computer simulation program was written in the BASIC language. The listing of this program is presented in Appendix A.

Figure 5-1 shows the output of the potentiometer which is proportional to the angular displacement of the pendulum vs time. The initial position of the pendulum is 1 v, and the control signal is limited to ±10v. The gains K_1, K_2, K_3, and K_5 are 0.89, 1.04, 1, and 1.1 respectively. The sampling period is set to 10 ms. It is observed from Figure 5-1 that the pendulum is brought back to zero position in less than 0.4 seconds.

Figure 5-2 shows the control signal, U, vs time. This signal converges to zero as time increases which implies that after a period of time, the input voltage to the motor is zero and the cart is stationary.

The response of the signal V_s is shown in Figure 5-3. This signal represents the sum of the signals from the tachometer, V_t, and the integrator, V_x. This Figure shows that, after a period of time, V_s goes to zero, which means that there is no output from the tachometer, and the cart is stationary.

Figure 5-4 shows the signal V_d vs time. V_d is the signal produced by the digital compensator, $D_4(z)$. As the input signal of the digital compensator approaches to zero, the signal V_d goes to zero.

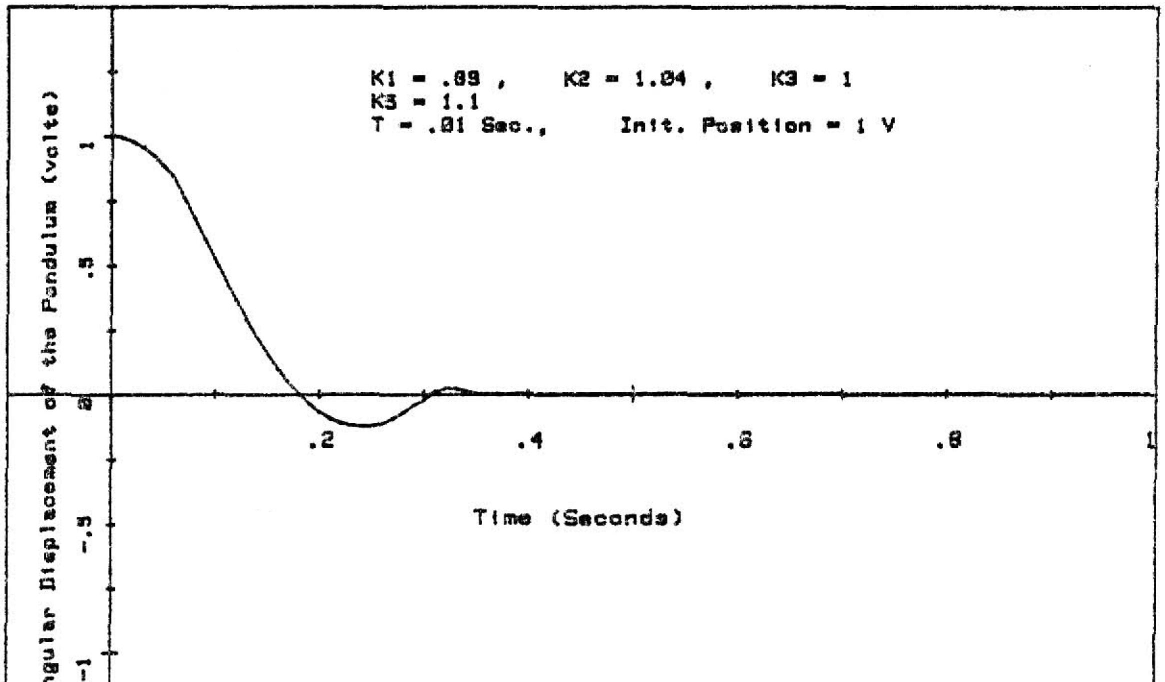


Figure 5-1
The Angular Displacement of the Pendulum vs Time

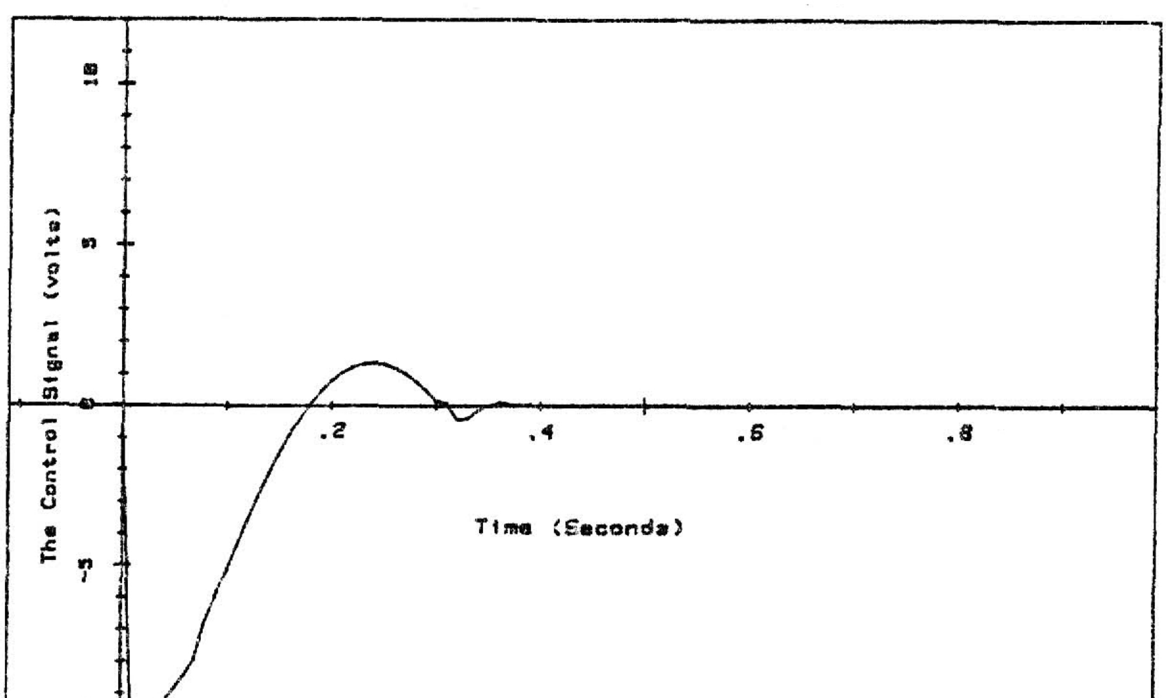


Figure 5-2
The Control Signal vs Time

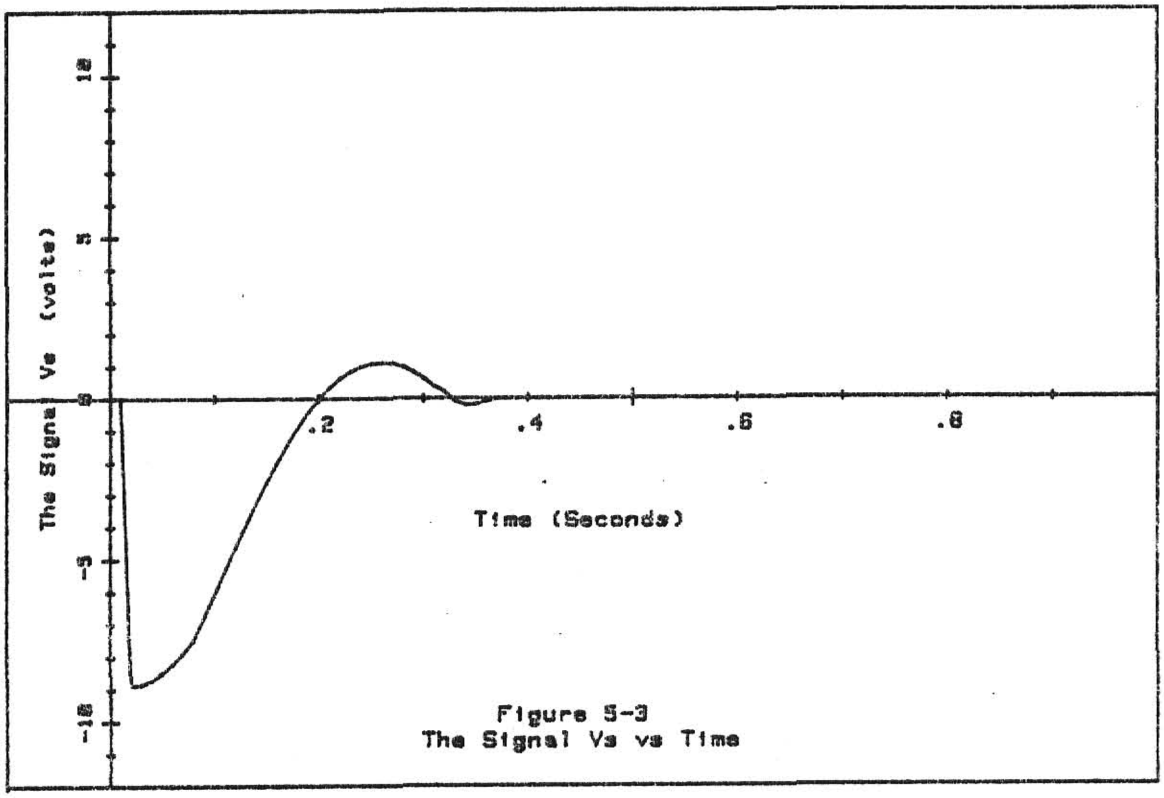


Figure 5-3
The Signal Vs vs Time

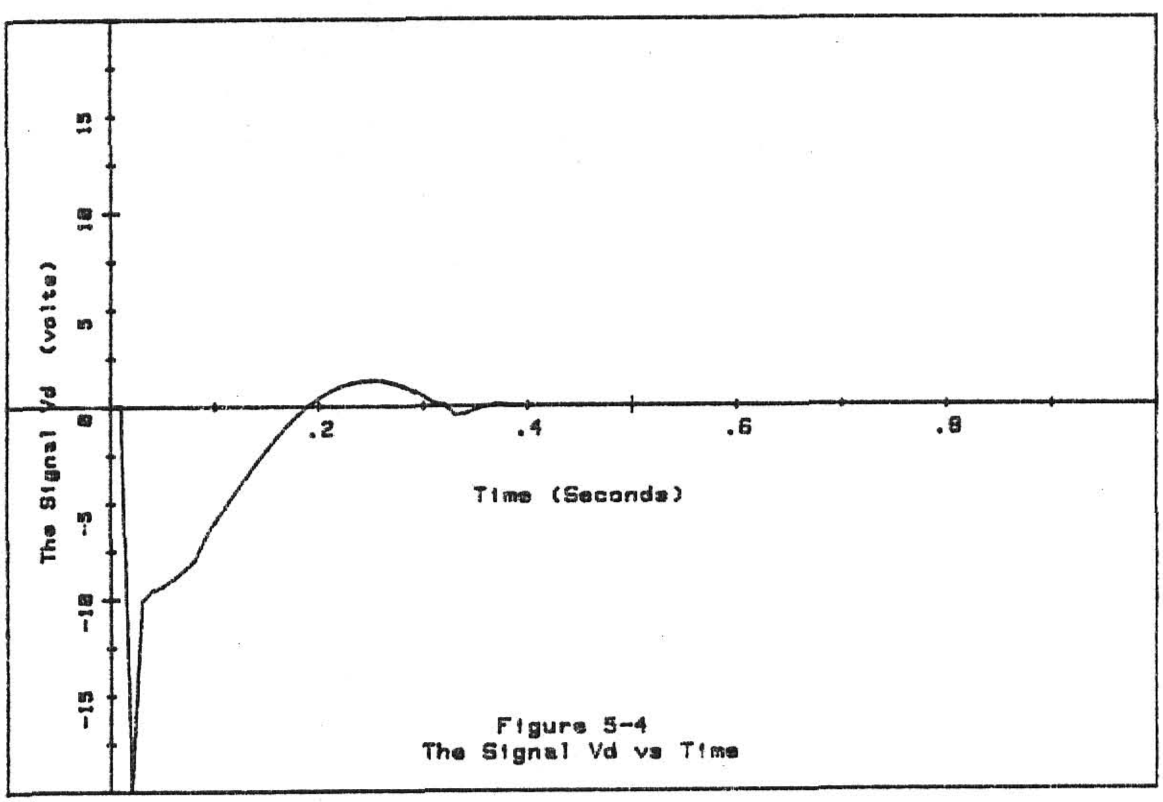


Figure 5-4
The Signal Vd vs Time

CHAPTER VI

THE SOFTWARE

The development of the software for this research was one of the major tasks. The programming of the microcomputer was done in Z-80 assembly language. By using the resident, Z-80 Assembler, the assembly language program was converted to machine image code. A floating point binary representation with a 15 bit mantissa, an 8 bit exponent, and a sign byte, was used for all digital values. This provides a resolution of 1 part in 32,768. By using this type of representation the accuracy of the computation was maintained.

Two Digital Group Z-80 microcomputers were used in this research. One which uses floppy disks as secondary storage was used for program development, and the other which uses cassette tapes as secondary storage was used for the real-time control. The DISKMON Operating System is used in the microcomputer with the disk drives. DISKMON provides a set of executive routines which allow user programs easy access to files. This operating system proved to be very helpful for linking the machine image code programs together.

The assembly language program and the corresponding image code were stored on the disk. When the experiment was conducted, the image code program was loaded into the memory of the development computer from the disk, and then transfered to the real-time control micro-computer. All of the interface devices such as the A/D converter, the D/A converters, and the timer were connected to real-time control microcomputer.

The real-time control program consists of a main program and nine subroutines. The memory required for the real-time control program is

2.5 K. Memory addresses 3E00H to 3E7FH where used for storing the counter, the coefficients, the signs, the exponents and the mantissas. A memory map that shows the memory used in the first page of 3E is presented in the Appendix C.

Main Program

The functions of the main program are to read the digital signals from A/D converter, perform specific computations, and send a digital control signal to the D/A converter.

The memory addresses from 3000H to 32DFH are occupied by the main program. A flow chart of the main program is shown in Figure 6-1. The assembly language program along with the image code is listed in Appendix B along with the rest of the software used in this research.

The main program can be divided into four parts: (1) the initialization, (2) the computation, (3) the modification of the output control signal for the D/A converter, and (4) the updating of all of the parameters.

Initialization

The initialization sequence was necessary to define certain quantities everytime the microcomputer was reset. By the end of this initialization all variables and coefficients used during the computation are given their respective initial values. The flow chart of this program is shown in Figure 6-2. The first step of this program is to initialize the output voltage of the D/A converter to zero so that the cart remains stationary. The next operation initializes memory block 3E00H-3E7FH to zero. Then the subroutines LAST and PENDIS are called. By executing the LAST subroutine, the zero reference and the bias are determined. The zero reference is the output voltage from the

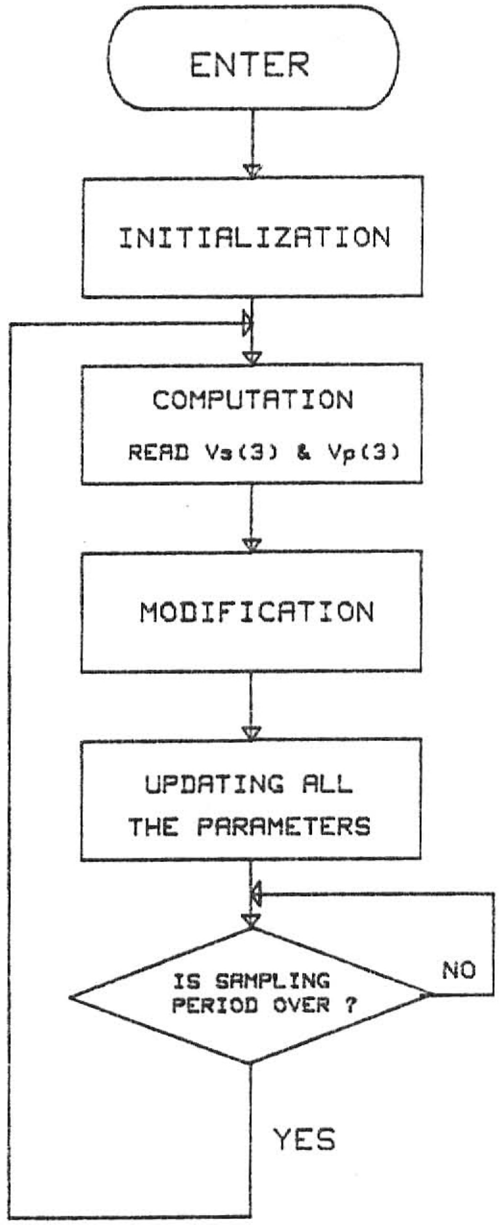


Figure 6-1
The Main Program

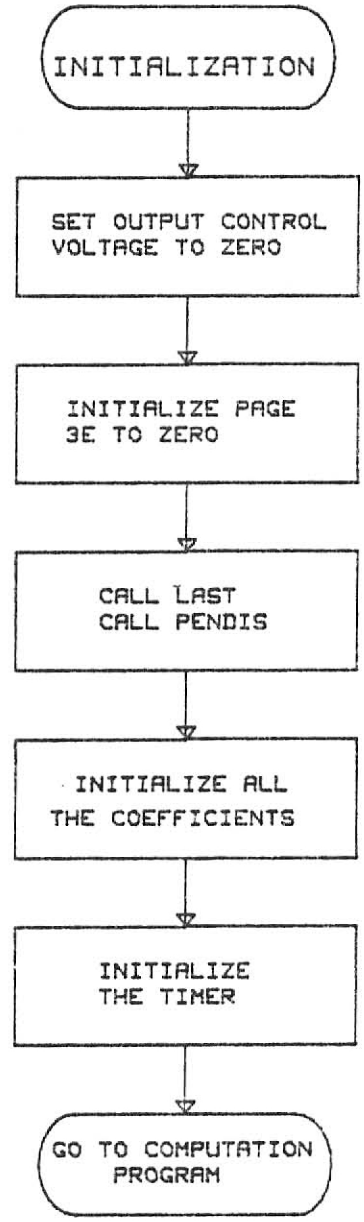


Figure 6-2
The Initialization Program

potentiometer corresponding to the vertical position of the pendulum. The PENDIS subroutine saves the initial position of the pendulum. Details of these two subroutines are given in the section on Subroutines.

The next operation stores all the coefficients and variables required by the software program into appropriate memory locations. The last step of this program initializes the 8253 programmable timer in the condition of: (1) accessing registers twice, (2) binary mode, (3) timer 0, and (4) mode 0.

The initialization program is executed once at the beginning of each experiment. The execution time of this program is not critical, because this execution time is not part of the sampling period.

Computation

The computation program is the most important part of the main program. This program samples the signal V_s and the position of the pendulum from the A/D converter, V_p, and performs computations of the equations shown below for the generation of the current control signal U(3).

(1) $V_d(3) = A_1V_d(2) + A_2V_d(1) + A_3V_s(2) + A_4V_s(1)$

(2) $V_q(3) = V_d(3) + V_p(3)$

(3) $U(3) = B_1U(2) + B_2V_q(3) + B_3V_q(2)$

The coefficients of the above equations are obtained from the analysis in earlier chapters. The flow chart of the computation program is shown in Figure 6-3.

The first step of this program resets the counter to time 10 milli seconds. The programmable timer counts down from the specific value to zero at a clock rate of .4 μ seconds per count. When the timer counts to zero the output signal from the timer is set to HI (logic 1). The next operation initializes the A/D converter to read $V_s(3)$, and sets

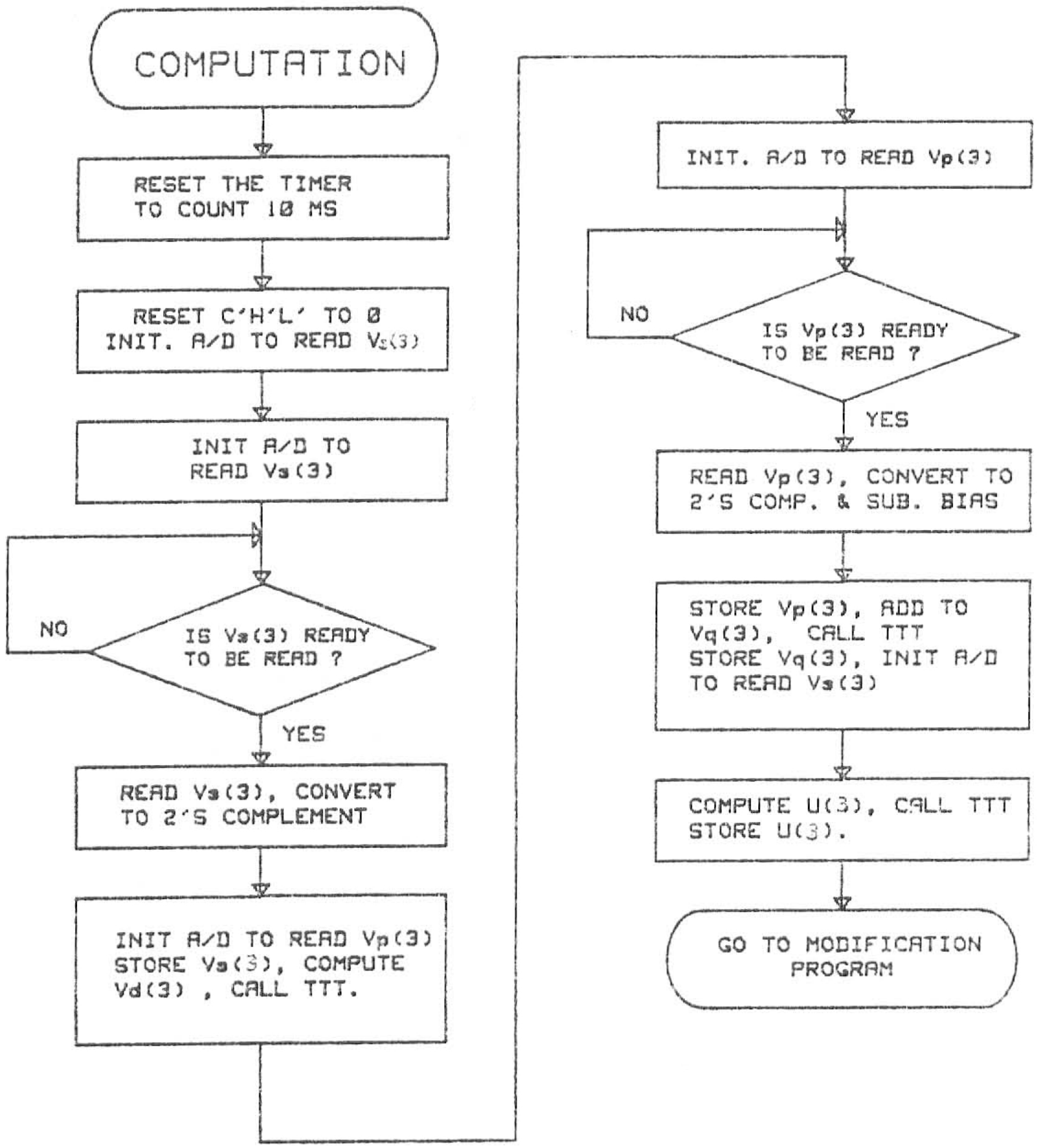


Figure 6-3, The Computation Program

the C'H'L' registers to zero. The C'H'L' registers must set to zero before computation of each of the equations. The next step commands the A/D converter to read $V_s(3)$ again, which results in an increased settling time of the analog signal, thus increasing the accuracy of the reading from the A/D converter. The next operation checks the "BUSY" signal of the A/D converter. This signal indicates that the value of $V_s(3)$ has settled down and is ready to be read. The next step reads $V_s(3)$ from the A/D converter, and converts it to a 2's complement value. The reading from the A/D converter is 11 bits long plus a sign bit.

The A/D converter is then initialized to read $V_p(3)$. The next operation performs the computation of $V_d(3)$. The A/D converter is now commanded to read $V_p(3)$ again, which results in an increased settling time of the analog signal, thus increasing the accuracy of the reading from the A/D converter. Then the "BUSY" signal from the A/D converter is continuously checked until the value of $V_p(3)$ is ready to be read. The next operation reads $V_p(3)$ from the A/D converter, converts to 2's complement value, and adjusts the value by subtracting or adding the bias, based on whether this value is greater or smaller than the zero reference. This bias value was obtained after execution of the subroutine LAST in the Initialization program.

The value of $V_p(3)$ is stored in memory, and is added to $V_d(3)$ which is stored in the C'H'L' resisters. The next operation converts this result to a 15 bit mantissa, a sign byte, and an exponent byte. The next operation performs the computation of U(3), The result of this computation, U(3), is converted to 15 bits mantissa with sign byte and an exponent byte. The last operation of this program saves this value in memory.

Executing the computation program produces the digital control signal U(3). This control signal has to be modified to satisfy the input format of the D/A converter. The program which accomplishes this modification is described in the next section.

Modification

The modification program modifies the three byte control value U(3) to fit the input format of the D/A converter. The D/A converter can only take 10 bit values. A digital value of 0 represents an output voltage of +10V; a digital value of 1FFH represents a 0 volt output; and a digital value of 3FFH represents an output voltage of -10V. A flow chart of the modifiication program is shown in Figure 6-4.

The first step of this program checks the sign of the control value. If the sign is negative, a 2's complement operation is performed, and the saturation condition is checked. If the control value is saturated, then the input to the D/A converter is 3FFH (-10 volts). If the control values is not saturated, then the control value is modified to fit the input format of the D/A converter. If the sign of the control value is positive, the saturation condition is checked. If the value is saturated, then the input to the D/A converter is 0 (+10 volts). If the control value is not saturated, then the control value is modified to fit the input format of the D/A converter.

In order to modify the control value to fit the input format of the D/A converter, a 2's complement operation is performed. Then,

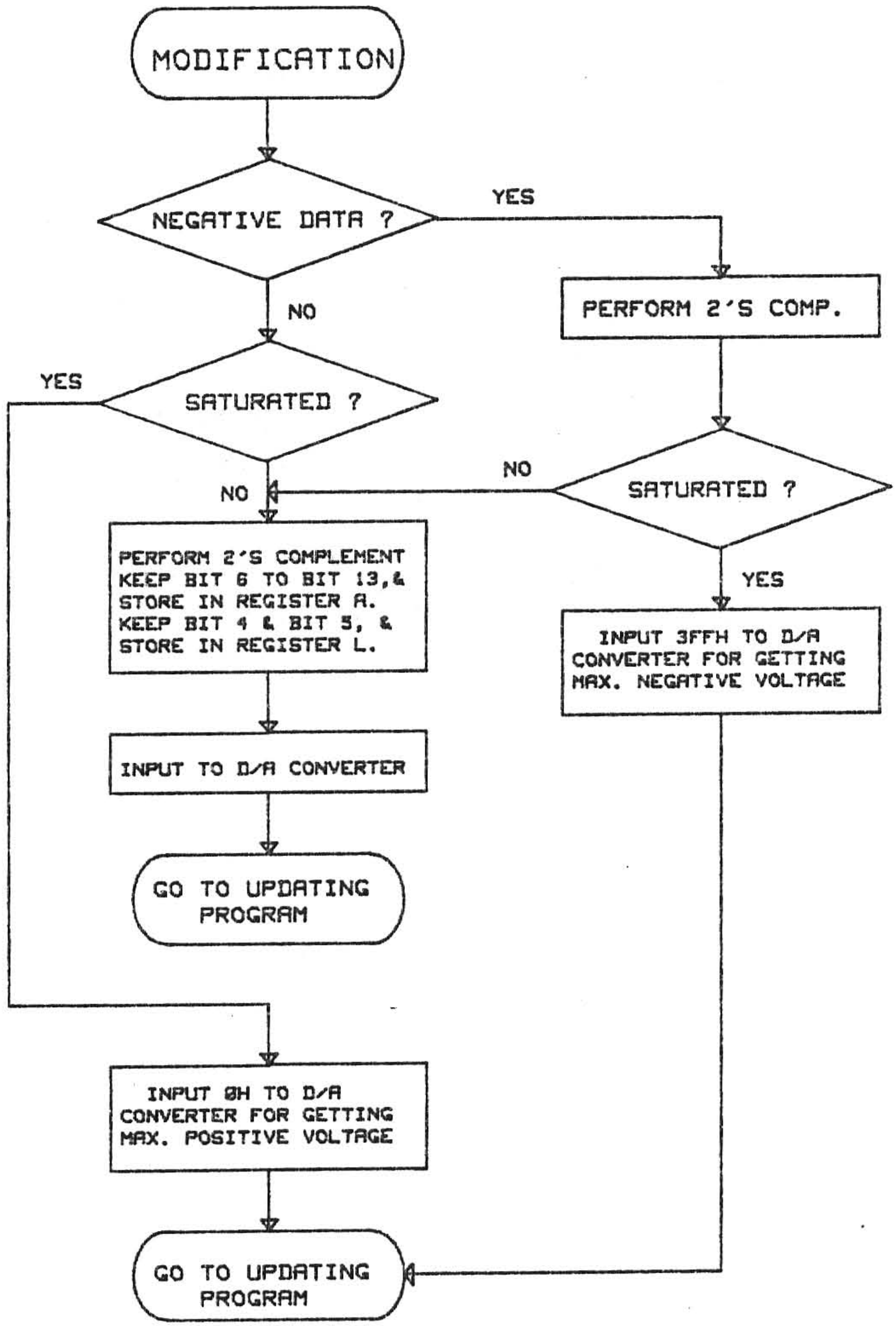


Figure 6-4, The Modification Program

the control value in bits 6 through 13 is transfered to register A, and the bits 4 and 5 of the control value is transfered to bits 3 and 4 of the register L.

The last step of this program inputs the modified control value to D/A converter. After this step, an updating program is executed to keep all the parameters updated.

Updating

All of the parameters have to be updated before executing the computation program in the next sampling period. By executing the updating program, the values are shifted one step down; that is, the value of $V_s(2)$ is shifted to $V_s(1)$, the value of $V_s(1)$ is shifted to $V_s(0)$, etc. A flow chart of the Updating program is shown in Figure 6-5.

The first three steps of this program update the signs, the exponents, and the mantissas of the parameters. The memory blocks of 3E30H through 3E39H, 3E40H through 3E49H, and 3E50H through 3E63H are shifted to 3E31H through 3E3AH, 3E41H through 3E4AH, and 3E52H through 3E65H respectively. The operation of updating of the signs and exponents is illustrated in Figure 6-6 (a) and the updating of the mantissa is illustrated in Figure 6-6 (b). Then a check is made to see whether the 10 milli-seconds sampling time is over; if so, the computation program will be executed. If not, the next operation is deferred until it is over.

The nine subroutines that support the main program will now be discussed individually.

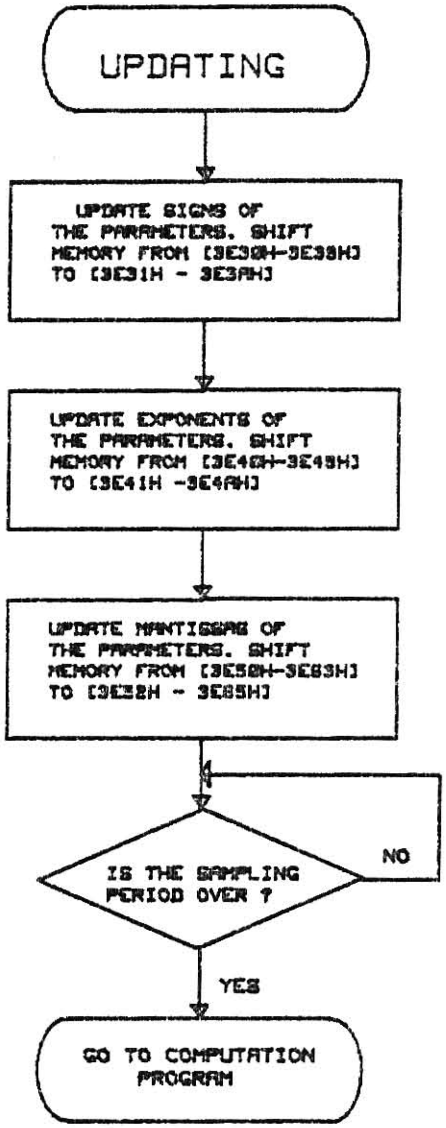


Figure 6-5

The Updating Program

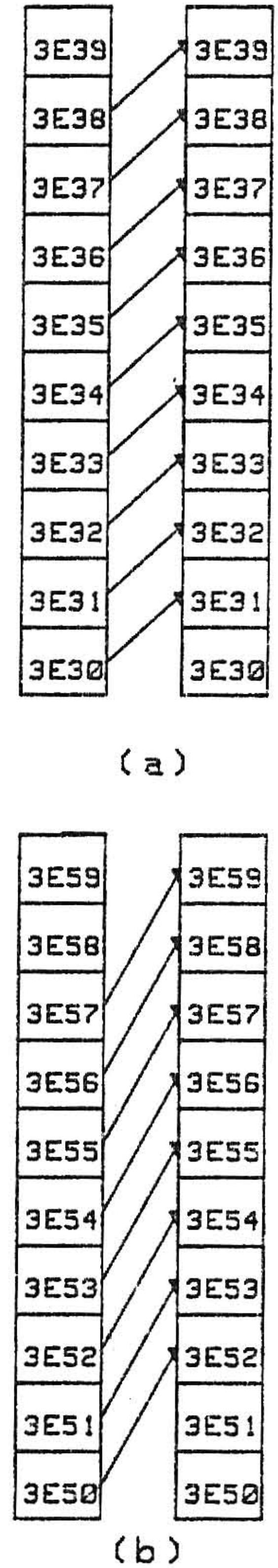


Figure 6-6

The Illustration of the Updating Method

Subroutines

There are nine subroutines that are used by the Main program. These are two fixed point arithmetic routines for multiplication and addition; a floating point operation routine for shifting the data; a routine for converting the value from fixed point representation to floating point; a routine for storing the data in a specific memory block; a routine for displaying the data on the CRT; a routine for performing the 2's complement operation; a routine for finding the zero reference and the bias; and a routine for keeping the value of the initial pendulum position. The following sections describe those subroutines.

Subroutine TTT

Subroutine TTT converts a signed, three byte value stored in C'H'L' registers into a 15 bit unsigned mantissa stored in the H'L' registers, a sign byte, and an exponent byte. The sign byte is placed in the memory location pointed to by the IY register. The exponent byte is placed in the memory location pointed to by the IX register. Before calling this subroutine, the data must be in the C'H'L' registers, and the pointers must be loaded into the IY and IX registers. A flow chart of this subroutine is shown in Figure 6-6. The list of the subroutine is given in Appendix B.

Subroutine SHIFT

Subroutine SHIFT shifts the mantissa stored in C H L registers to the left or right a number of bits according to the sign and magnitude of the exponent. The mantissa is shifted until the value of the exponent becomes zero.

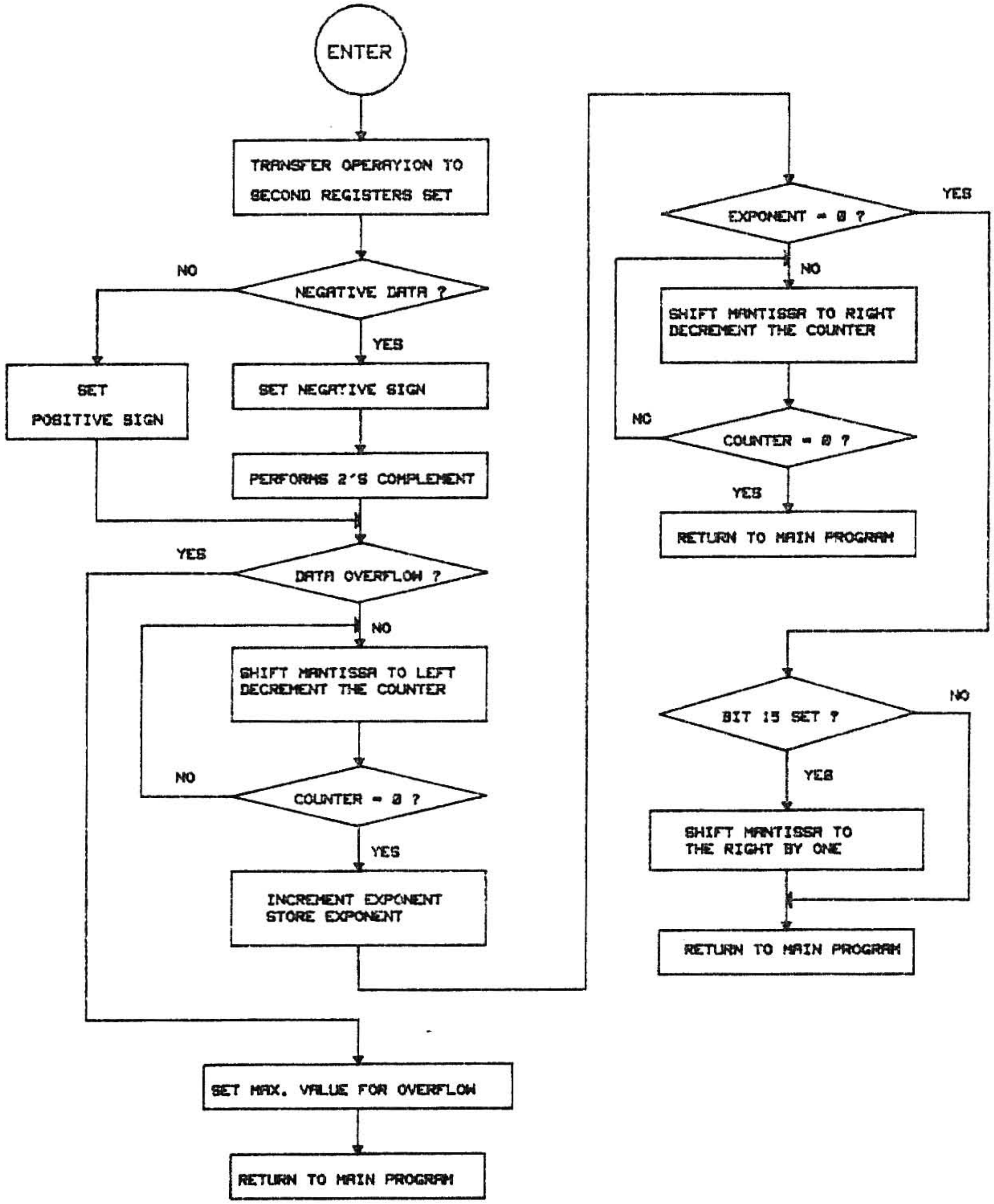


Figure 6-7, Subroutine TTT

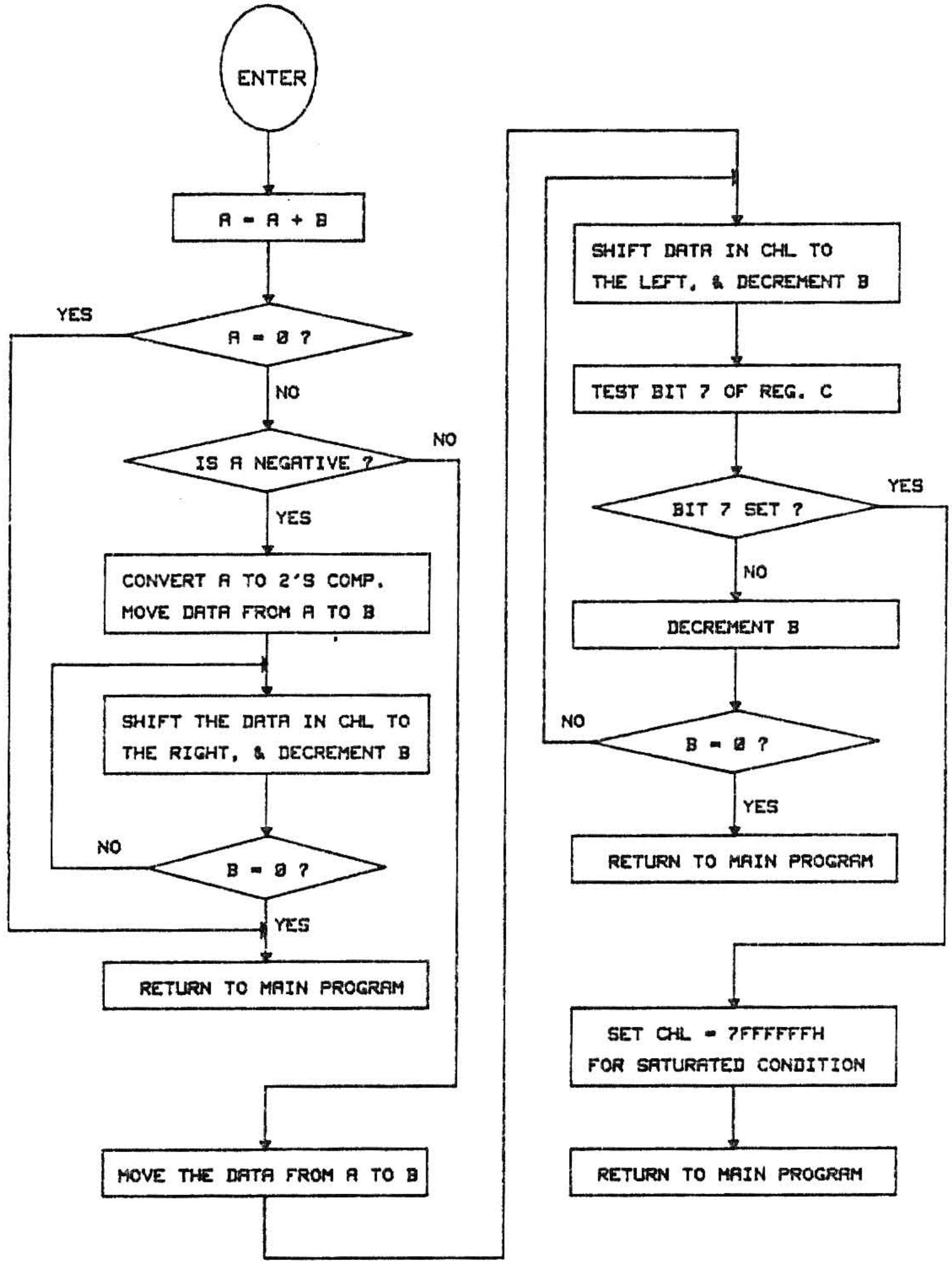


Figure 6-8, Subroutine SHIFT

A flow chart of this subroutine is shown in Figure 6-7. The list of this subroutine is given in Appendix B.

The first step of this subroutine checks whether the exponent is equal to zero. If so, then no shifting operation is carried out and the control is returned back to Main program. If the exponent is not zero the sign of the exponent is checked. If the sign of the exponent is negative, it is changed to positive and the mantissa is shifted to the right and the exponent decrements until the exponent reaches zero. If the sign of the exponent is positive, the data is shifted to the left and the exponent decrements until the exponent reaches zero. The saturation condition is checked during the left shifting operation. If a saturation condition occurs, the maximum value of 7FFFFFH is placed in the CHL registers.

Subroutine MULT

The multiplication subroutine multiplies an 8 bit unsigned multiplier with a 15 bit unsigned multiplicand. To use this subroutine, the multiplicand must be in registers DE, and the multiplier is in the memory location pointed to by the IX register. The result of the multiplication is placed in CHL registers. Basically, this subroutine carries out a series of tests and shifts of the multiplier and multiplicand. Figure 6-8 shows the flow chart of this routine. The listing of the multiplication subroutine is given in Appendix B.

Subroutine COMP

The subroutine COMP converts a twenty-three bit unsigned binary number stored in the CHL registers to 2's complement form. The result of the operation is placed in the CHL registers.

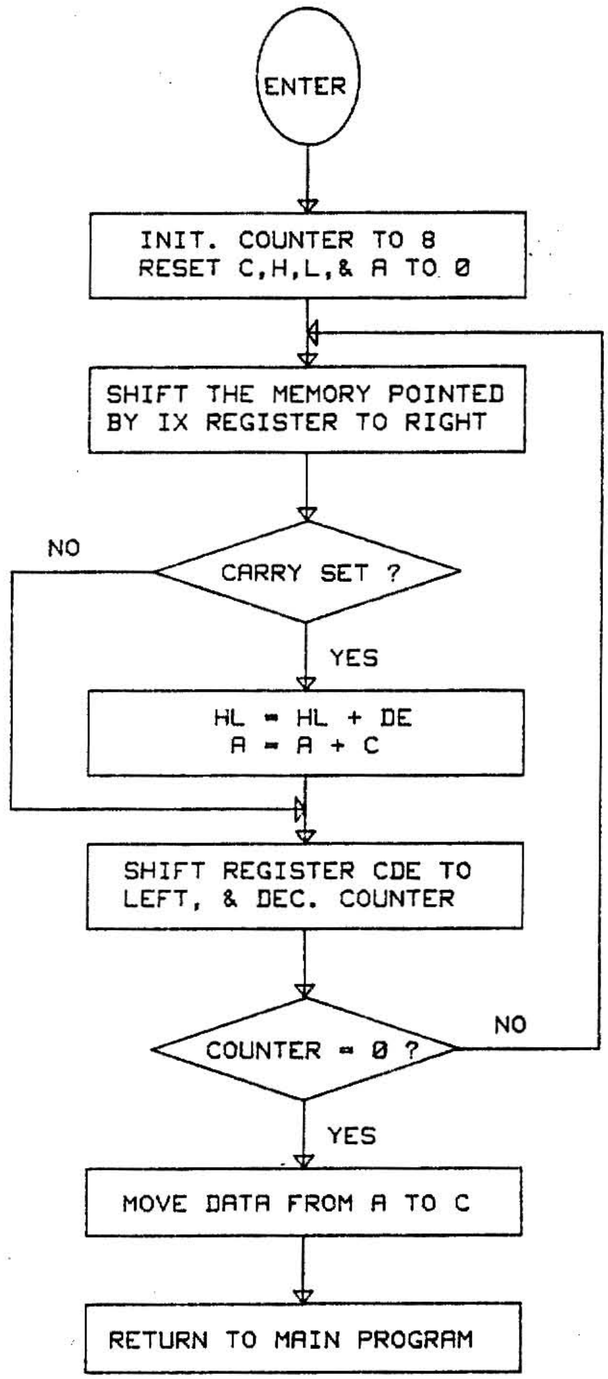
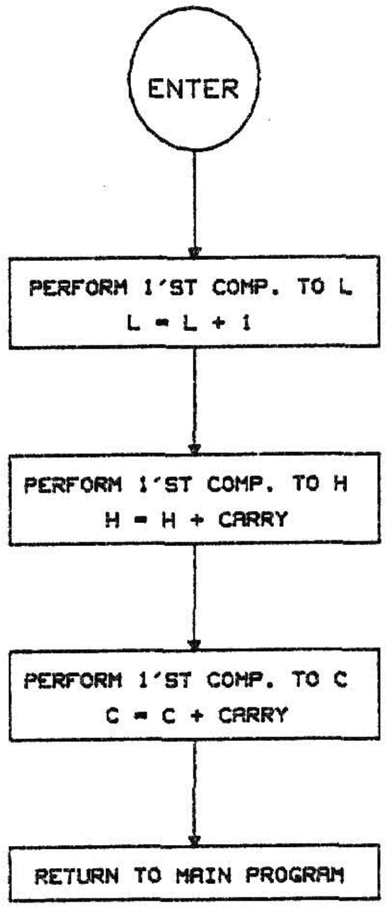


Figure 6-9, Subroutine MULT



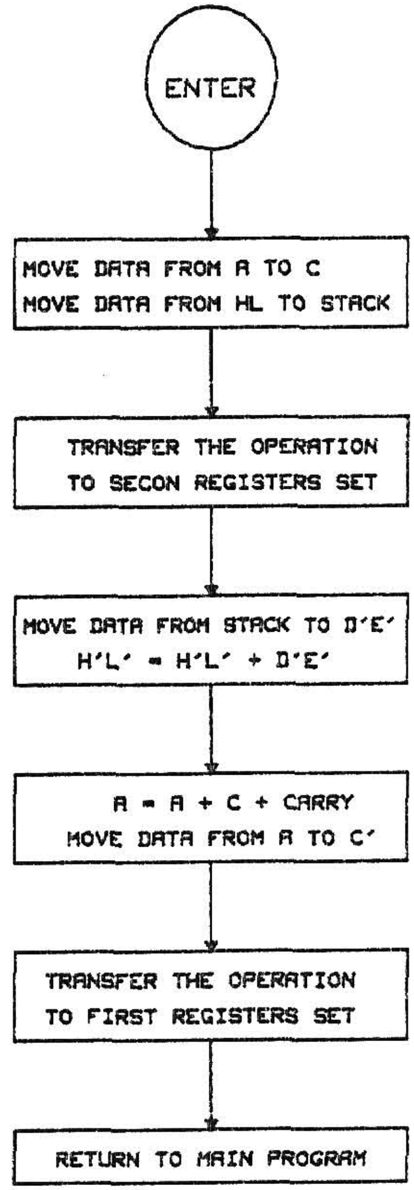


Figure 6-10, Subroutine COMP

Figure 6-11, Subroutine ADD

Figure 4-9 shows the flow chart of this subroutine. The listing of this subroutine is given in Appendix B.

Subroutine ADD

Subroutine ADD adds two twenty-four bit signed binary numbers with one number in the C H L registers, and the other in C'H'L' registers. result of the adding operation is placed in C'H'L' registers. A flow chart of this subroutine is shown in Figure 6-10. The assembly language program of this routine is listed in Appendix B.

Subroutine STORE

The STORE routine stores the values of the pendulum position $V_p(3)$ in certain memory locations. This routine is used for data acquisition and for error diagnostics. The routine is called at the end of the modification program and is able to record a data value every other time the Main program is executed, for up to 256 readings. These data value may subsequently be displayed to show the dynamic response of the system.

The flow chart of this routine is shown in Figure 6-11. The listing of this routine is given in Appendix B.

Subroutine DISPLAY

A subroutine that displays the pendulum position $V_p(3)$ on the CRT was developed to assist with debugging the software and verifying the operation of the hardware. A signed binary value that represented the pendulum position is converted to a hexadecimal ASCII code, and then displayed on the CRT with a positive or negative sign. Figure 6-12 shows the flow chart of this routine. The assembly language listing is given in Appendix B.

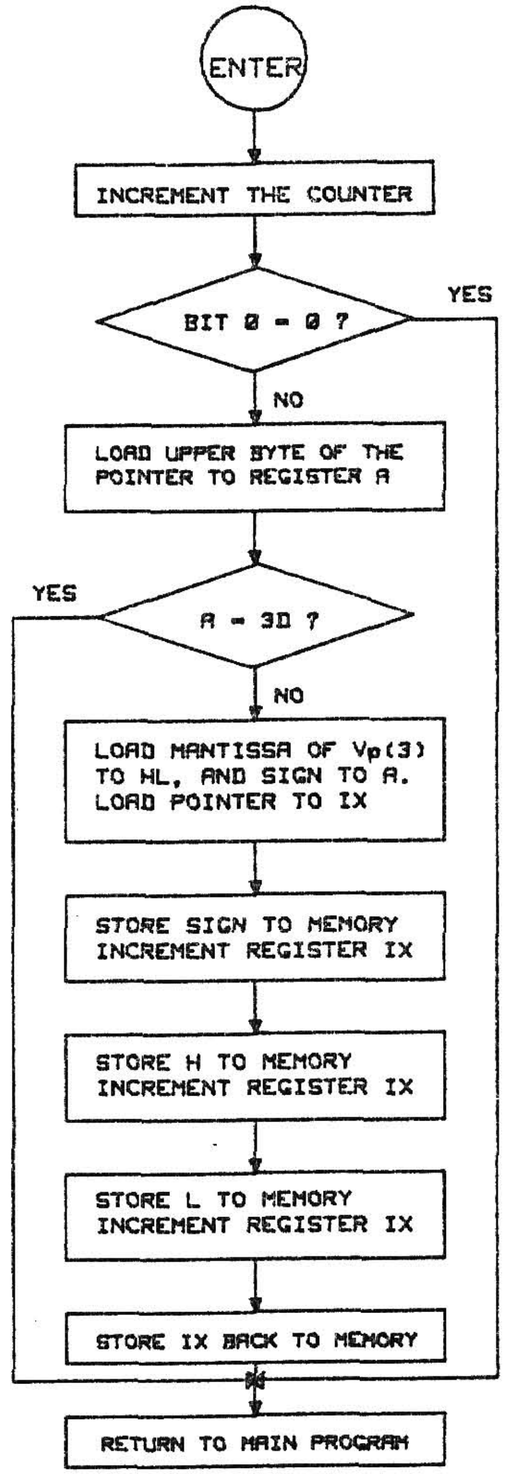


Figure 6-12, Subroutine STORE

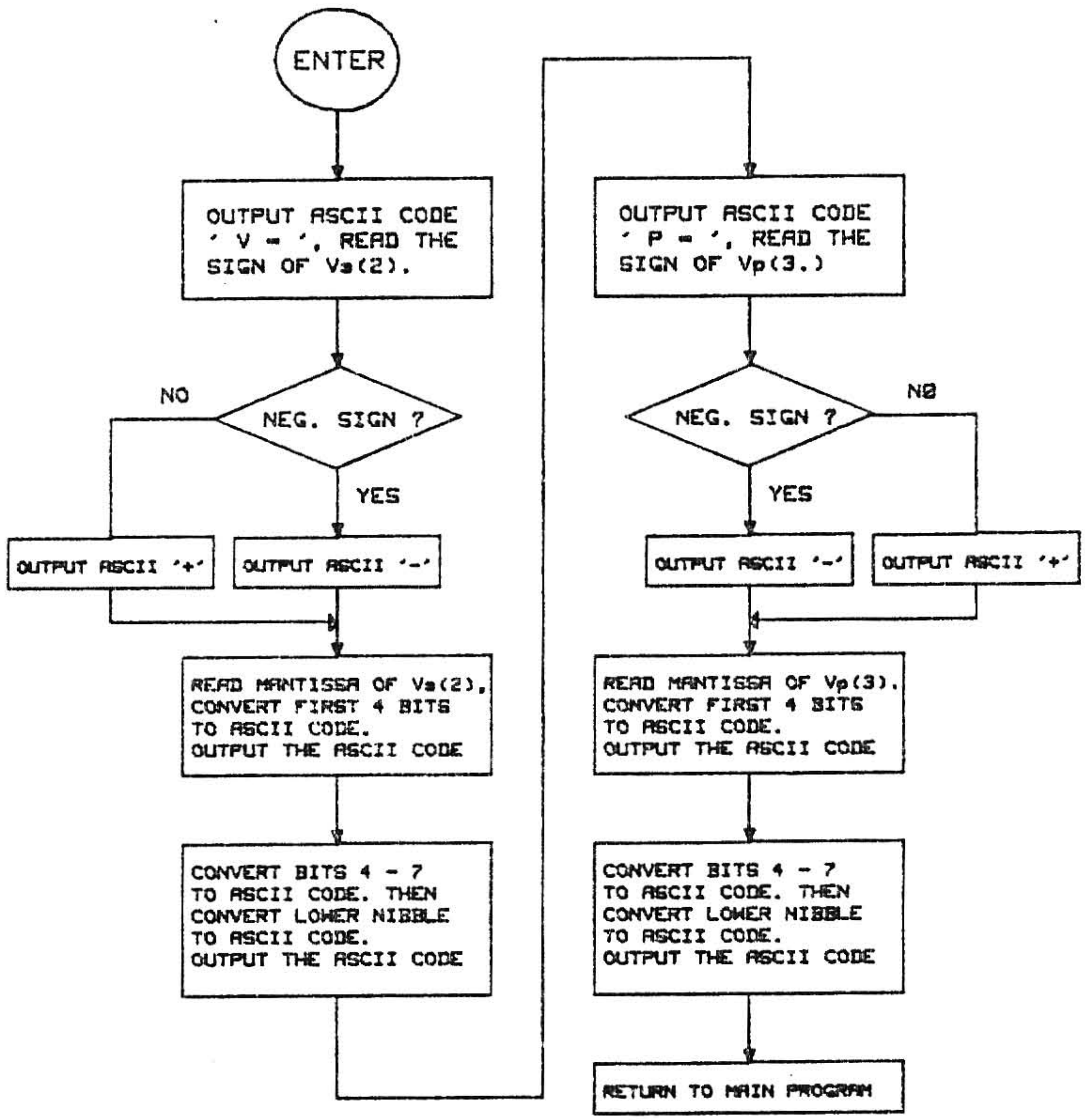


Figure 6-13, Subroutine DISPLAY

Subroutine LAST

Subroutine LAST is called during execution of the Initialization program. The bias voltage is the output from a D/A converter which is connected to the input of an A/D converter. The A/D converter is set to be in the differential mode with one input from the potentiometer and the other from the D/A converter (the bias). The pendulum is set to vertical position before execution of the LAST subroutine. During execution of the subroutine LAST the position of the pendulum is displayed continuously on the CRT. By executing this subroutine, the bias voltage is adjusted to match the voltage from the potentiometer, and the zero reference voltage is found. The bias voltage can be adjusted by depressing certain keys on the keyboard. The bias voltage can be decreased by depressing the key "D", and increased by by depressing the key "I". By appropriately depressing these two keys, the value displayed on the CRT is adjusted as close to 800 H as possible, thus minimizing the error between the bias and the potentiometer voltages. The key "E" is then depressed to transfer control to subroutine PENDIS.

The listing of subroutine LAST is given in Appendix B.

Subroutine PENDIS

This subroutine is executed immediately following the execution of the subroutine LAST. The initial position of the pendulum is saved as a digital value by execution of this subroutine. The limits of the displacement of the pendulum are fixed by adjustment of the set-screws provided near the pivot of the pendulum. The digital value is displayed continuously on the CRT so that an overflow condition caused by oversetting the initial position of the pendulum can be avoided.

After the adjustments are made, the key "R" is pressed to return control back to the Main program. A listing of this subroutine is given in Appendix B.

CHAPTER VII

EXPERIMENTAL PROCEDURES

In this chapter the equipment arrangement will first be presented. Next, the experimental procedures which were followed throughout this research will be discussed.

Equipment Arrangement

The inverted pendulum is mounted in two ball bearings on top of a light weight four wheeled cart. A microtorque potentiometer, attached to the pendulum shaft, provides the voltage, V_p, proportional to the angular position of the pendulum. A 36 volt dc power supply is used to energize the potentiometer. The cart is driven by a dc servo motor, mounted on the bottom of the cart, through a speed reducing belt drive system. The field of the motor is energized by a 20v dc power supply. The armature of the motor is controlled by the output of a dc power amplifier which is supplied by a $\pm$ 30v dc power supply. A permanent magnet dc tachometer, attached to the motor shaft, provides the voltage, V_t, proportional to the motor speed. Electrical signals are passed to and from the cart through an umbilical cord.

Real-time control of the system is provided by a Digital Group, Z-80 microcomputer. Analog signals V_p and V_s are sampled and digitalized by the A/D converter. The digital control signal is delivered in analog form to the system by the D/A converter. The specification of the A/D and D/A converters are given in Table 7-1. An 8253 programmable timer was connected to the microcomputer for timing the sampling period. Four operational amplifiers were used to provide feedback signals around the power amplifier, motor, cart system and

TABLE 7-1

Specification of Analog to Digital Converter

Manufacturer	Burr-Brown
Model	SDM-856
Channel	16 (single)
	8 (differential)
Maximum Input Voltage	± 5 V
Resolution	12 bits

Specification of Digital to Analog Converter

Manufacturer	Analog Devices
Model	DAC-10Z
Channel	2
Maximum Output Voltage	± 10 V
Resolution	10 bits

to generate the signal V_s. Figure 7-1 shows the arrangement of these amplifiers with the rest of the system. Strip chart recorders were used for data collection.

Experimental Procedures

Two Z-80 microcomputers were used for this research. One was used as the real-time controller described in the previous section. The other was used for program development. The program development computer operates under the DISKMON operating system with two floppy disks for file storage. Both microcomputers are equipped with audio cassette recorder interfaces. By connecting the audio cassette output from one microcomputer to the audio cassette input on the other, files can be transferred directly between the two microcomputers.

The machine image code of the real-time control program is developed on the disk based microcomputer and stored in a disk. When the experiment is conducted, the Assembler is loaded into the development microcomputer and the real-time controller from the disk and cassette tape respectively. Then the machine image code of the real-time control program is transferred from the disk to the development microcomputer and is placed in memory starting at address 3200H. Then by executing the instruction "SAVES" on the developement computer, and "LOADS" on the real-time controller, the machine image code program is transferred through the audio cassette interfaces to the real-time controller. The starting address of the machine image code in the real-time controller is changed to 3000H. Then the instruction "NEWFILE" is executed in the real-time controller. At this point, the program is in the real-time controller and ready to be executed. The next step of the experiment is to hold the inverted pendulum in the upright

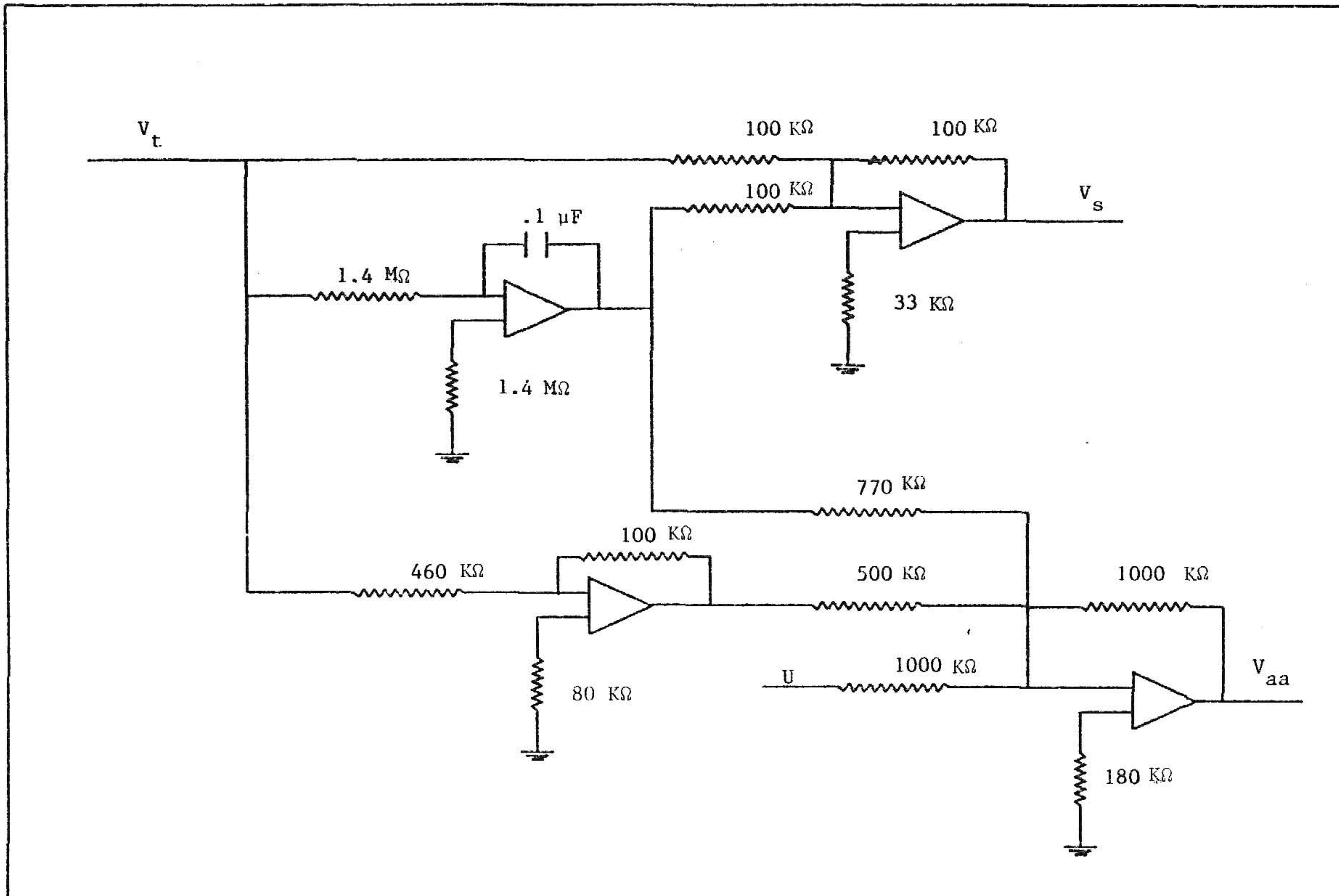


Figure 7-1
The Circuitry for the System

position, and to find the zero reference voltage. This is accomplished by attaching a plumb line on the top of the inverted pendulum and adjusting the two set-screws at the bottom of the inverted pendulum until the pendulum is vertical as checked by the plumb line. Then the plumb line is removed and the subroutine of the real-time control program is executed. By depressing the "I" and "D" keys on the keyboard the value of the bias voltage added to the pendulum voltage is increased or decreased. The sum of the pendulum voltage and the bias voltage is continuously digitalized by the D/A converter and the digital value is displayed on the CRT. The bias voltage is adjusted until the displayed value is as near 800 H (corresponding to 0 V) as possible. Then the "E" key is pressed and the limits of the pendulum motion are fixed by adjustment of the set-screws. The experiment can now be started by depressing the "R" key and supplying power to the motor. Everytime the experiment is re-run, the bias in the real-time controller is reset.

CHAPTER VIII

PRESENTATION OF THE RESULT

A Z-plane stability analysis of the system was given in Chapter III. The mathematical model developed in Chapter III includes three poles and two zeroes. The poles at e^{bT} and e^{-bT} arise from the dynamics of the pendulum. The pole at e^{bT} is outside the unit circle and represents the unstable characteristic of the inverted pendulum. The location of the third pole at e^{-aT} is determined by the characteristic of the motored cart and by the gains of the operational amplifiers ($a = K_1K_3K_5$). The location of the two zeroes are also controlled by the values of the gains of the operational amplifiers and digital compensator. In order to simplifiy the analysis in Chapter III, one of the zeroes was located so as to cancel the pole at e^{-aT}. For the experimental work presented in this chapter, slightly different values of the amplifier gains were used. The root locations corresponding to the exponential values are shown in Figure 8-1. The gains K_1, K_2, K_3, K_5, and K_{20} are 0.89, 1.04, 7, 1.3, and 2 respectively. The coefficients of the digital compensator K_{11} and K_{12} are 2.237 and -1.115 respectively.

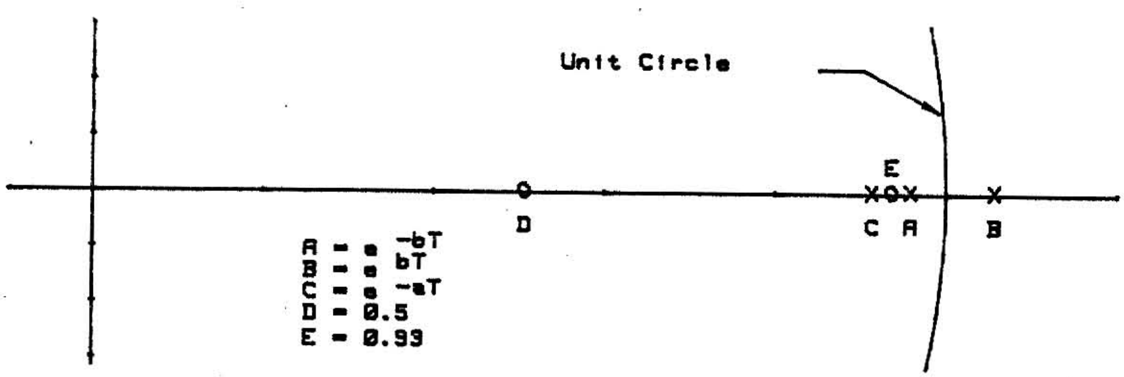


Figure 8-1, The Location of the Roots

An experiment based on the digital models without the optimal controller was performed. No data has been taken during this experiment. The cart was first allowed to move on the flat carpeted floor, and the system was found to be unstable. The cart was then allowed to move on the carpeted floor with a piece of plywood underneath the carpet and both ends of the floor were elevated. Under this condition, the system stabilized. Some observations were made during this experiment.

1) The displacement of the cart was limited in the range of $\pm$ 3.5 feet.

2) The pendulum oscillated at small amplitudes and low frequencies.

A second experiment was conducted applying the optimal control. The results of this experiment are presented in the next section (Results of the Optimal Control). Two strip chart recorders were used to record the control signal, U, the output signals of the potentiometer, V_p, and the tachometer, V_t. The cart was first allowed to move on the flat floor. The system was unstable, and the cart moved in only one direction. A suspicion arose that the bias was not taken care of appropriately. The cart was then allowed to move on the carpeted floor with elevated ends. The system then became stable. Some limited data was taken and is presented in the next section. The results of the above two experiments are compared and conclusions can be drawn as below:

1) The displacement of the cart during the second experiment was much smaller.

2) The oscillations of the pendulum in the second experiment

were less.

3) The velocity of the cart in the second experiment was less. Hence, it may be concluded that, although the system was stablized in both the instances, the overall performance of the system can be enhanced by using the optimal control.

Results of the Optimal Control

Figures 8-2, 8-3, and 8-4, show the output voltage of the potentiometer vs time for different speeds of the recorder. The gain of the potentiometer is 5.73 v/radian, the chart speed for these three recordings are 125, 5, and 1 mm/second respectively. The sensitivity is held at 50 mv/division, which in turn corresponds to 0.5 angle degree/mm. The initial position of the pendulum is 0.218 radians away from the vertical line. It is observed from the Figure 8-2 that the pendulum is brought back to vertical position in less than 0.3 seconds, which then oscillates with a very small amplitude. Figure 8-4 shows that the pendulum position remains stable even after two minutes.

Figures 8-5 and 8-6 show the response of the control signal. This signal is sent out from the D/A converter. The chart speeds are 125 and 5 mm/second respectively. The sensitivity is 500 mv/division. Figures 8-7 and 8-8 show the output voltage from the tachometer vs time. The chart speeds for these two recordings are 5 and 1 mm/second. The sensitivity is 100 mv/division or about 0.024 ft/sec/mm. The maximum speed of the cart is about 0.5 ft/second. The displacement of the cart may be found by integrating the curve shown in Figure 8-6. This curve can be approximated to a sine wave. The area under the curve is the displacement of the cart from its initial position. In this case, the displacement is found to be about 2 feet on either side of of the initial position.

The above results lead to the following conclusion.

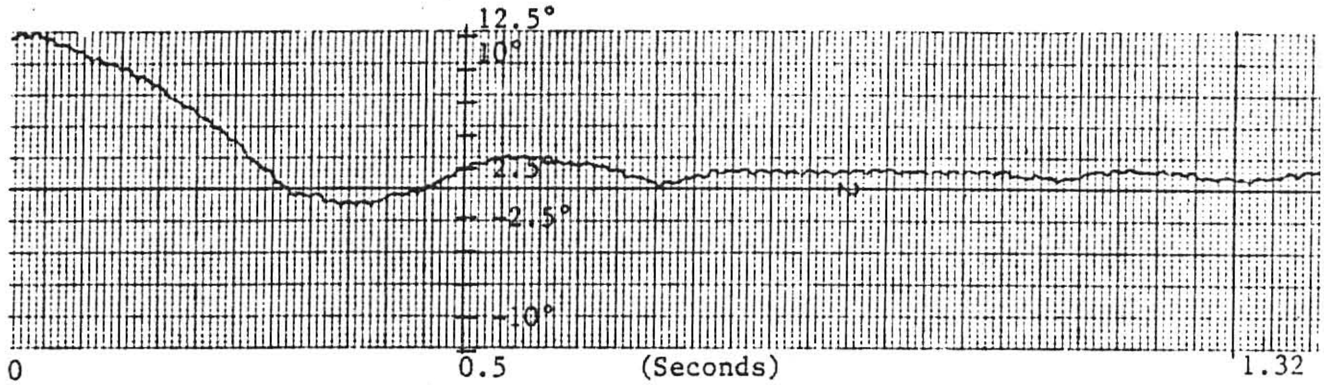


Figure 8-2, The Angular Displacement of the Pendulum,50 mm/div, 125 mm/sec

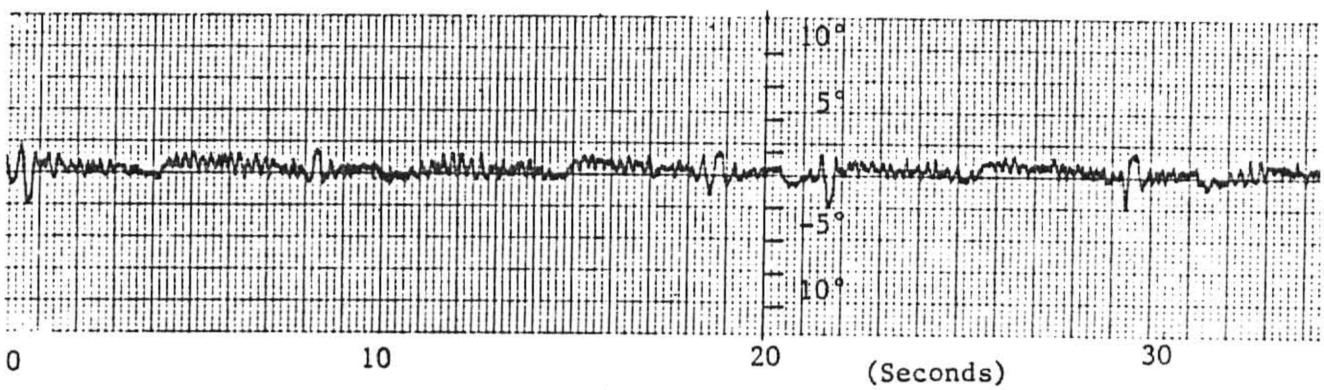


Figure 8-3, The Angular Displacement of the Pendulum,50 mv/div, 5 mm/sec

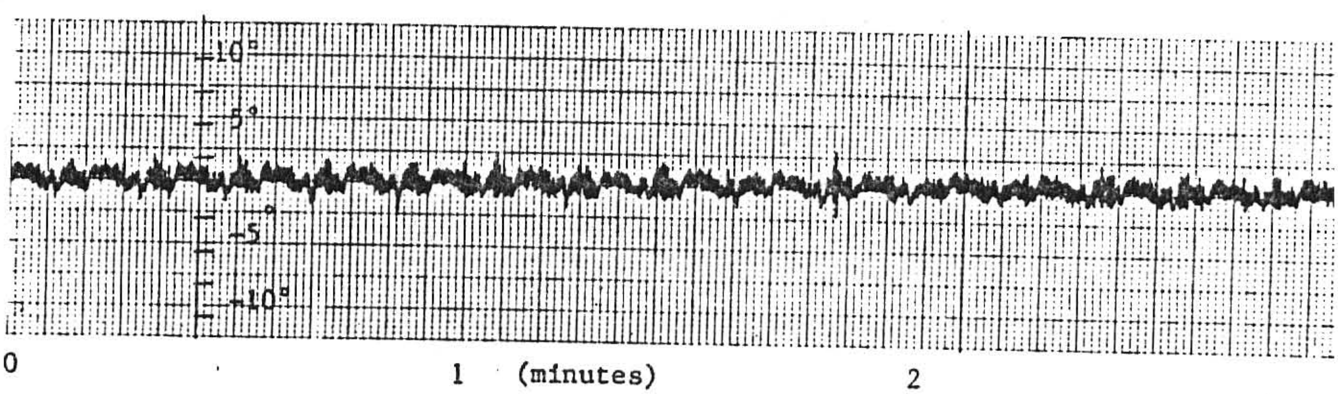


Figure 8-4, The Angular Displacement Of The Pendulum,50 mv/div, 1 mm/sec

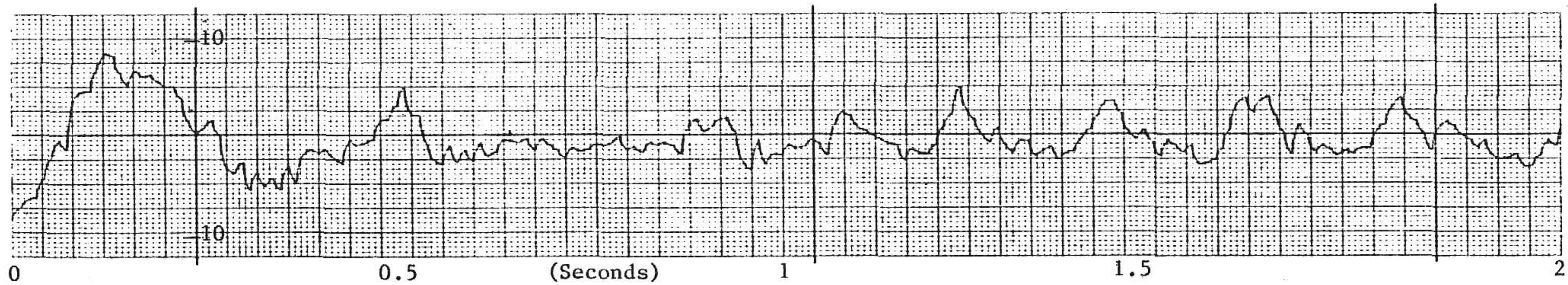


Figure 8-5, The Control Signal, 500 mv/div, 125 mm/sec

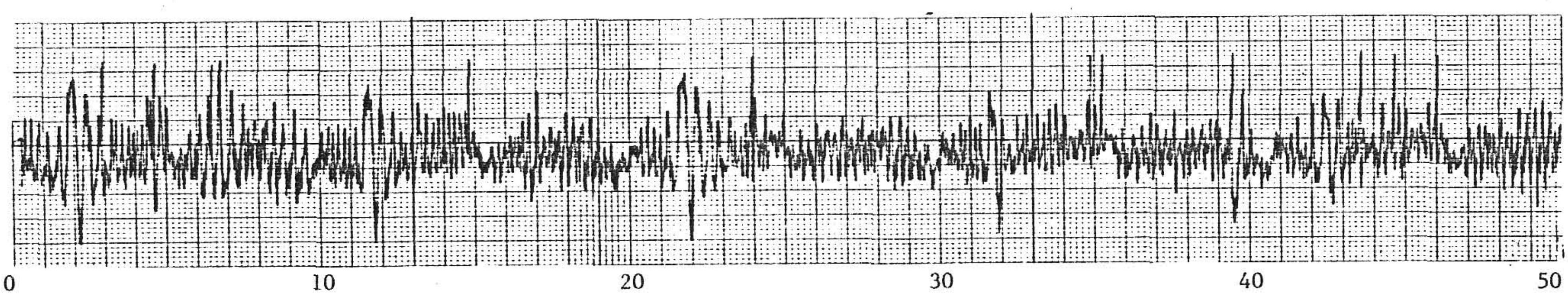


Figure 8-6, The Control Signal, 500 mv/div, 5mm/sec

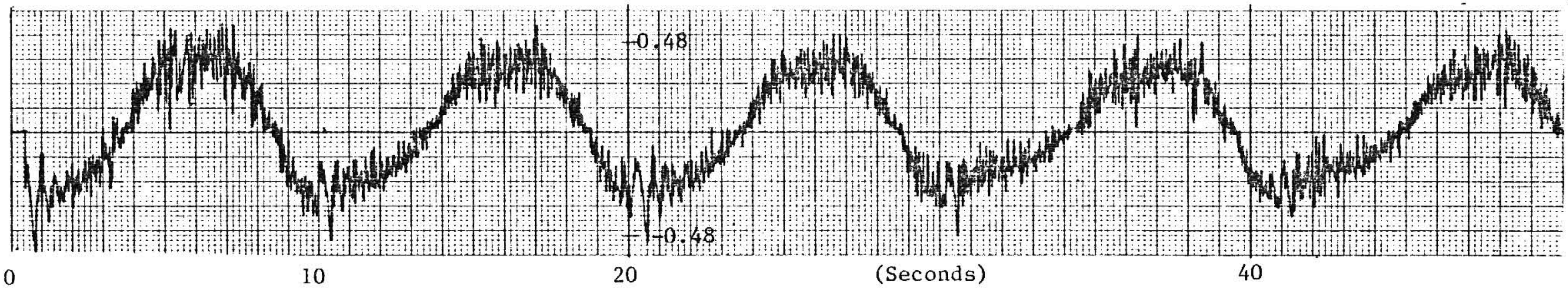


Figure 8-7, The Output of Tachometer, 100 mv/div, 5mm/sec

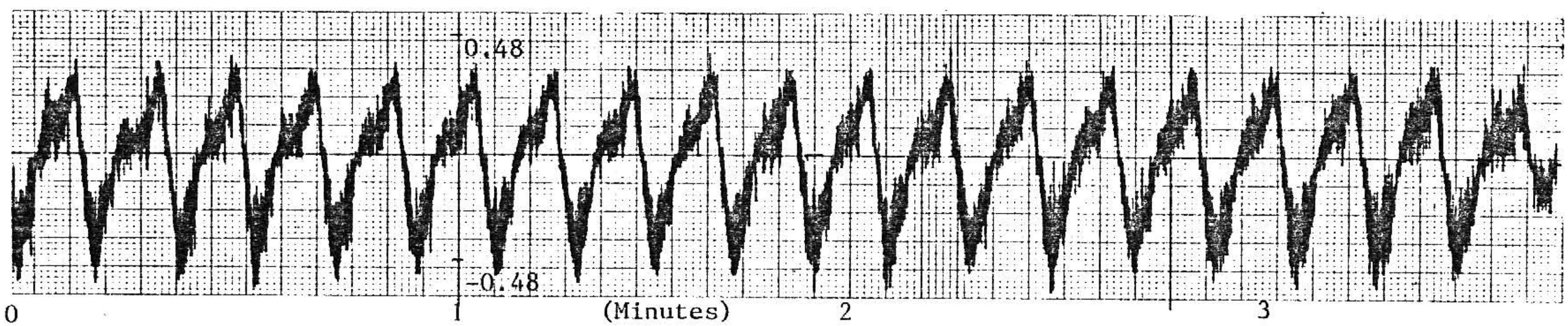


Figure 8-8, The Output of Tachometer, 100 mv/div, 1 mm/sec

CHAPTER IX

OBSERVATIONS, CONCLUSIONS AND RECOMMENDATIONS

Observations

During the final evaluation of the real time control program, an error that has been overlooked throughout the research was detected. The control signal is represented by a 23 bit binary value, whereas the D/A converter is capable of accepting only a 10 bit long value. Hence, in order to fit the format of the D/A converter, and setting K_{eq} to 0.5, the bits 4 through 13 of the control signal were to have been transferred to the D/A converter. However, bits 2 and 3 of the control signal were placed in the D/A converter in locations where bits 4 and 5 should have been placed, with the other bits occupying correct locations. The effect of this mistake on the analog output of the control signal is presented in the form of a graph in Figure 9-1.

When the pendulum is in near vertical position, the output signal from the potentiometer V_p is small, which produces a small control signal. It will be observed from Figure 9-1 that for small digital values of the control signal, the gain K_{eq} is 2.0 or 0. But, discussions in Chapter IV showed that the system will not stabilize if K_{eq} is greater than 1.33 or equal to 0.

When the pendulum moves away from the vertical position, the strength of the control signal increases, which makes the gain, K_{eq}, fall within the range of 0.5 to 1.0, which has a stabilizing effect on the system.

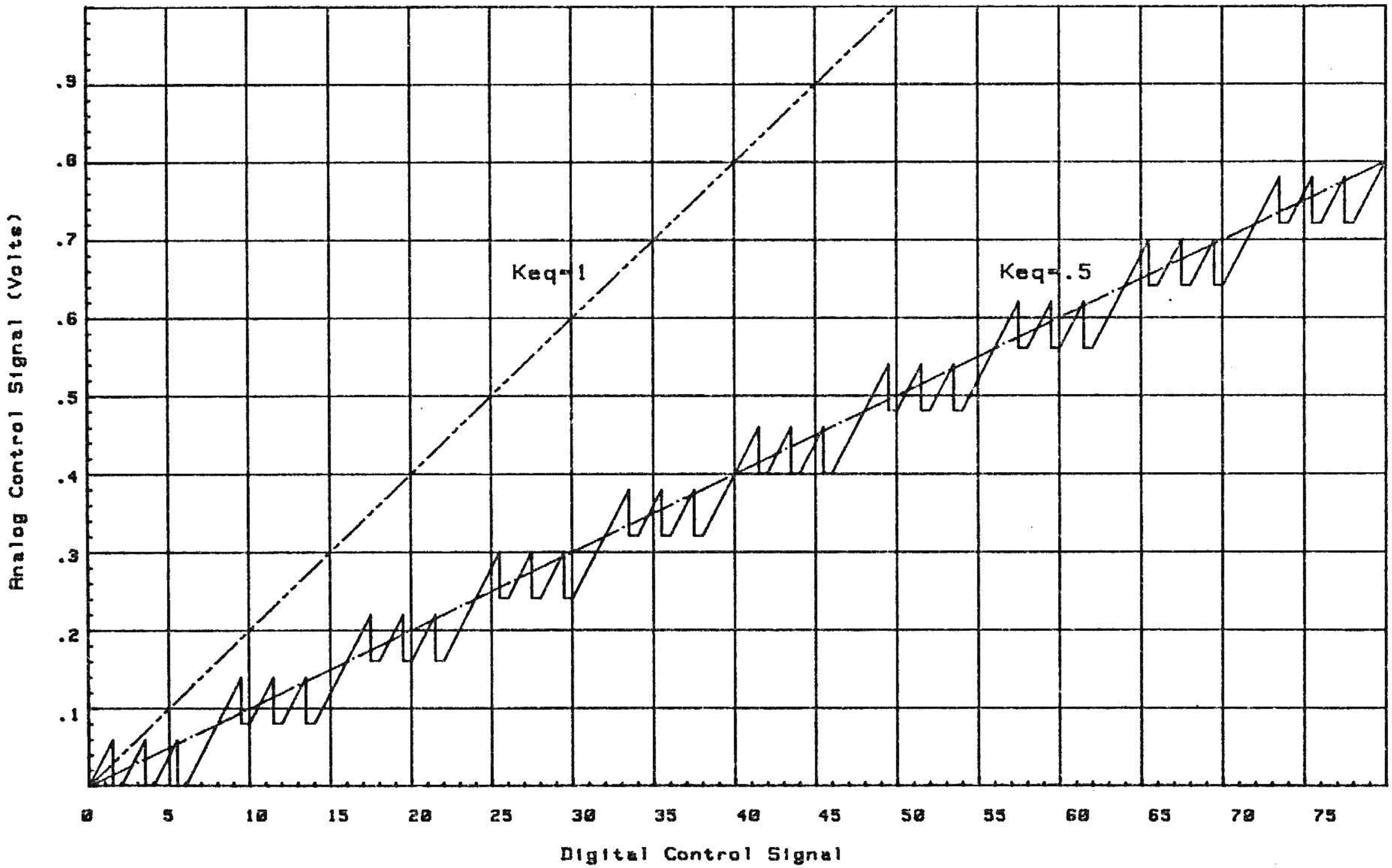


Figure 9-1

The Relationship Between the Digital and Analog Control Signal

Therefore, the pendulum is unable to stay in an upright position but oscillates in a limit cycle within a small range. This fact can be observed from the various graphs presented in the preceeding chapter.

<u>Conclusions</u>

1) The technique of the optimal control with digital compensation is proved to be successful in stabilizing the naturally unstable cart-pendulum system.

2) For this research, the behavior of the motor can be adequately described as a gain.

3) The bias of the angular displacement of the pendulum is taken care of by allowing the cart to move on the carpeted floor, either ends of which are propped up like a small ramp.

4) The oscillations of the pendulum and the cart could have been caused by the varying characteristic of the gain K_{eq}.

5) A comparison of Figures 5-1 and 5-2 with 8-2 and 8-5 shows that the responses of the pendulum and control signal match with the results of the computer simulation during the first 0.4 seconds. Subsequently, the effects of the bias and the varying value of K_{eq} and the nonlinearity of the system make the actual response deviate slightly away from the predicted response. It is believed that in the absence of these three effects, the actual response could exactly match with the computer simulation.

<u>Recommendations</u>

There are several recommendations which can be made to improve upon the research conducted for this thesis, and to expand upon the system for further research.

The accuracy of the computation may be improved by using true floating point arithmetic operations in the multiplication and addition routines. A task of writing the real time control program can be eased by employing a more advanced microprocessor (16 bits) or a micrcomputer with a FORTRAN compiler.

Two problems that was encountered with the physical system were regarding the belt and the potentiometer. The belt that couples the motor with the wheels of the cart broke down. It is recommended that either the belt material be changed or the driving mechanism be modified. The microtorque potentiometer failed occasionally. A different method for measuring the displacement of the pendulum is recommended.

Since all the design work has been done with the assumption that the value of K_{eq} equal to one, an experiment conducted with this value of the gain, K_{eq}, would be worthwhile.

For further research, the technique of adaptive optimal control may be applied.

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APPENDICES

Appendix A

The Simulation Program

```
10 !  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
20 !  $$                                        $$
30 !  $$            SIMULATION PROGRAM          $$
40 !  $$                                        $$
50 !  $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
60 !  PLOTTER IS 13,"GRAPHICS"
70 !  GRAPHICS
80    PLOTTER IS 7,5,"9872A"
90    PRINTER IS 7,5
100   PRINT "VS5"
110   LIMIT 25,175,25,125
120   FRAME
130   SCALE -10,100,-12,12
140   AXES 10,1,0,0,5,4
150   Init=1
160   K1=.89
170   K2=1.04
180   K3=1
190   K5=1.1
200   T=.01
210   A=K1*K3*K5
220   B=24.15^.5
230   A3=(A+B)*EXP(-B*T)+(A-B)*EXP(B*T)-2*A*EXP(-A*T)
240   B3=-2*A+(A+B)*EXP((B-A)*T)+(A-B)*EXP(-(A+B)*T)
250   C3=B3/A3
260   K10=K1*K2*A3/(2*(A^2-B^2))
270   D3=K3*(1-EXP(-A*T))/A-1
280   K11=2.2368
290   K12=-1.1133
300   N1=EXP(B*T)+EXP(-B*T)+EXP(-A*T)
310   N2=-1-EXP(-A*T)*(EXP(B*T)+EXP(-B*T))
320   N3=EXP(-A*T)
330   N4=C3-1
340   N5=-C3
350   M1=EXP(-A*T)
360   M2=K1
370   M3=K1*D3
380   H1=EXP(-B*T)+EXP(B*T)
390   H2=-1
400   PRINTER IS 16
410   H3=K11
420   H4=K12
430 ! $$$$$$$$$$$$$  INITIALIZATION  $$$$$$$$$$$$$$$
440   Vp(1)=Vp(2)=Vp(0)=Init
450   Vd(1)=Vd(2)=Vd(3)=Vs(1)=Vs(2)=Vs(3)=0
460   U(1)=U(2)=U(3)=Vq(1)=Vq(2)=Vq(3)=0
470 ! $$$$$$$$$$$$$$  COMPUTATION  $$$$$$$$$$$$$$$$
480   FOR W=0 TO 100
490   Vp(3)=N1*Vp(2)+N2*Vp(1)+N3*Vp(0)+K10*U(2)
500 !        +K10*N4*U(1)+K10*N5*U(0)
510   PLOT W,U(2)
520   Vd(3)=H1*Vd(2)+H2*Vd(1)+H3*Vs(2)+H4*Vs(1)
530   Vq(3)=Vp(3)+Vd(3)
540   U(3)=.5*U(2)-.5*(EXP(B*T)+EXP(-B*T))*Vq(3)+.5*Vq(2)
550   Vs(3)=M1*Vs(2)+M2*U(3)+M3*U(2)
560   IF U(3)>10 THEN U(3)=10
570   IF U(3)<-10 THEN U(3)=-10
580   PRINT Vp(3),U(3),Vd(3),Vs(3)
```

```
590 ! $$$$$$$$$$$$$$$$$  UPDATING  $$$$$$$$$$$$$$$$$
600   U(0)=U(1)
610   U(1)=U(2)
620   U(2)=U(3)
630   Vs(0)=Vs(1)
640   Vs(1)=Vs(2)
650   Vs(2)=Vs(3)
660   Vd(0)=Vd(1)
670   Vd(1)=Vd(2)
680   Vd(2)=Vd(3)
690   Vq(1)=Vq(2)
700   Vq(2)=Vq(3)
710   Vp(0)=Vp(1)
720   Vp(1)=Vp(2)
730   Vp(2)=Vp(3)
740   NEXT W
750 ! $$$$$$$$$$$$$$  PLOTTING  $$$$$$$$$$$$
760   S=.2
770   X=18.5
780   FOR A=0 TO 4
790   MOVE X,-1
800   LABEL S
810   X=X+20
820   S=S+.2
830   NEXT A
840   MOVE 35,-4
850   LABEL "Time (Seconds)"
860   MOVE 28,-10
870   LABEL "       Figure 5-2"
880   LABEL "The Control Signal vs Time"
890   DEG
900   LDIR 90
910   CSIZE 2.75
920   X=-10
930   Y=-10.5
940   FOR A=0 TO 4
950   MOVE -2,Y
960   Y=Y+5
970   LABEL X
980   X=X+5
990   NEXT A
1000  CSIZE 3
1010  MOVE -5.5,-5
1020  LABEL "The Control Signal (volts)"
1030  LDIR 0
1040  MOVE 30,9
1050  LABEL "K1 =";K1;",     K2 =";K2;",     K3 =";K3
1060  LABEL
1070  LABEL "T =";T;"Sec.,      Init. Position = 1 V"
1080  END
```

Appendix B

The Real-Time Control Program

```
3AD7            0000 ********************************************
3AD7            0010 *                MAIN PROGRAM.               *
3AD7            0020 ********************************************
3AD7            0110 MULT   EQU  399AH
3AD7            0115 LAST   EQU  3600H
3AD7            0120 SHIFT  EQU  3958H
3AD7            0125 PENDIS EQU  3800H
3AD7            0130 TTT    EQU  3900H
3AD7            0140 ADD    EQU  3981H
3AD7            0145 COMP   EQU  398AH
3000            0150        ST   3000H
3000 3E 7F      0160        LD   A,7FH    * OUTPUT 0 V TO MOTOR
3002 32 F1 FF   0170        LD   (0FFF1H),A
3005 32 F2 FF   0180        LD   (0FFF2H),A
3008 3E 00      0190        LD   A,0
300A 06 80      0200        LD   B,80H    * RESET 3E00 - 3E7F
300C 21 00 3E   0210        LD   HL,3E00H
300F 77         0220 LOOP   LD   (HL),A
3010 23         0230        INC  HL
3011 10 FC      0240        DJNZ LOOP
3013 3E 0A      0250        LD   A,0AH  * INIT. RESETTING VALUE
3015 32 71 3E   0260        LD   (3E71H),A
3018 CD 00 36   0270        CALL LAST
301B CD 00 38   0280        CALL PENDIS
301E CD E6 00   0290        CALL 000346   * HOME ERASE
3021 3E 80      0300        LD   A,80H
3023 32 00 3E   0310        LD   (3E00H),A      * A1
3026 3E 80      0320        LD   A,80H
3028 32 01 3E   0330        LD   (3E01H),A      * A2
302B 3E 8F      0340        LD   A,8FH
302D 32 02 3E   0350        LD   (3E02H),A      * A3
3030 3E 8F      0360        LD   A,8FH
3032 32 03 3E   0370        LD   (3E03H),A      * A4
3035 3E 80      0380        LD   A,80H
3037 32 10 3E   0390        LD   (3E10H),A       * B1
303A 3E 80      0400        LD   A,80H
303C 32 11 3E   0410        LD   (3E11H),A       * B2
303F 3E 80      0420        LD   A,80H
3041 32 12 3E   0430        LD   (3E12H),A       * B3
3044 3E FF      0631        LD   A,0FFH
3046 D3 10      0632        OUT  10H      * CLEAR INPUT PORT
3048 3E 30      0635        LD   A,30H    * SET UP CONTROL REG.
304A D3 17      0636        OUT  17H
304C 3E 60      0640 MAIN   LD   A,60H     * RESET TIMER
304E D3 14      0642        OUT  14H
3050 D3 14      0643        OUT  14H
3052 3E 00      0646        LD   A,0
3054 67         0650        LD   H,A
3055 6F         0660        LD   L,A
3056 4F         0670        LD   C,A
3057 D9         0680        EXX                  * C'H'L'=0
3058 3E 12      0750        LD   A,12H           * READ VP(3)
305A 32 F3 FF   0760        LD   (0FFF3H),A
305D 3A F1 FF   0770 LOW    LD   A,(0FFF1H)
```

```
3060 CB 7F                   BIT  7,A
3062 28 F9                   JR   Z,LOW
3064 3A F1 FF          HIGH  LD   A,(0FFF1H)
3067 CB 7F                   BIT  7,A
3069 20 F9                   JR   NZ,HIGH
306B 3A F2 FF                LD   A,(0FFF2H)    * READ UP(3)
306E CB 5F                   BIT  3,A
3070 28 29                   JR   Z,NEG
3072 E6 07                   AND  07H
3074 67                      LD   H,A
3075 3A F0 FF                LD   A,(0FFF0H)
3078 6F                      LD   L,A
3079 ED 5B 7B 3E             LD   DE,(3E7BH)    * BIAS
307D ED 52                   SBC  HL,DE
307F CB 7C                   BIT  7,H
3081 28 06                   JR   Z,C4A
3083 19                      ADD  HL,DE
3084 7B                      LD   A,E
3085 95                      SUB  L
3086 6F                      LD   L,A
3087 18 23                   JR   C4B
3089 06 02             C4A   LD   B,02H       * GAIN
308B CB 25             HHH   SLA  L
308D CB 14                   RL   H
308F 10 FA                   DJNZ HHH
3091 22 5A 3E                LD   (3E5AH),HL   * STORE UP(3)
3094 3E 00                   LD   A,0
3096 32 3A 3E                LD   (3E3AH),A
3099 18 21                   JR   C4C
309B 3A F0 FF          NEG   LD   A,(0FFF0H)
309E 2F                      CPL
309F 6F                      LD   L,A
30A0 3A F2 FF                LD   A,(0FFF2H)
30A3 2F                      CPL
30A4 E6 07                   AND  07H
30A6 67                      LD   H,A
30A7 ED 5B 7B 3E             LD   DE,(3E7BH)
30AB 19                      ADD  HL,DE
30AC 3E 01             C4B   LD   A,01H
30AE 32 3A 3E                LD   (3E3AH),A
30B1 06 02                   LD   B,02H
30B3 CB 25             HH    SLA  L
30B5 CB 14                   RL   H
30B7 10 FA                   DJNZ HH
30B9 22 5A 3E                LD   (3E5AH),HL
30BC 3E 00             C4C   LD   A,0H         * READ US(3)
30BE 32 F3 FF                LD   (0FFF3H),A
30C1 3E 00                   LD   A,0
30C3 4F                      LD   C,A
30C4 67                      LD   H,A
30C5 6F                      LD   L,A
30C6 D9                      EXX
30C7 ED 5B 52 3E             LD   DE,(3E52H)       * UD(3)
30CB DD 21 00 3E             LD   IX,3E00H     * A1
30CF CD 9A 39                CALL MULT
30D2 06 FA                   LD   B,0FAH
```

```
30D4 3A 41 3E    1340        LD   A,(3E41H)
30D7 CD 58 39    1350        CALL SHIFT
30DA 3A 31 3E    1360        LD   A,(3E31H)
30DD CB 47       1370        BIT  0,A
30DF 00          1380        NOP
30E0 28 03       1385        JR   Z,A1
30E2 CD 8A 39    1390        CALL COMP
30E5 CD 91 39    1400 A1     CALL ADD
30E8 ED 5B 54 3E 1420        LD   DE,(3E54H)    * VD(1)
30EC DD 21 01 3E 1430        LD   IX,3E01H      * A2
30F0 CD 9A 39    1440        CALL MULT
30F3 06 F9       1450        LD   B,0F9H
30F5 3A 42 3E    1460        LD   A,(3E42H)
30F8 CD 58 39    1470        CALL SHIFT
30FB 3A 32 3E    1480        LD   A,(3E32H)
30FE 3C          1490        INC  A
30FF CB 47       1500        BIT  0,A
3101 28 03       1510        JR   Z,A2
3103 CD 8A 39    1520        CALL COMP
3106 CD 91 39    1530 A2     CALL ADD
3109 3E 02       1540        LD   A,02H     * INIT A/D TO READ VS(3)
310B 32 F3 FF    1550        LD   (0FFF3H),A
310E 3A F1 FF    1560 LLL    LD   A,(0FFF1H)
3111 CB 7F       1570        BIT  7,A
3113 28 F9       1580        JR   Z,LLL
3115 3A F1 FF    1590 H      LD   A,(0FFF1H)
3118 CB 7F       1600        BIT  7,A
311A 20 F9       1610        JR   NZ,H
311C 3A F2 FF    1620        LD   A,(0FFF2H)  * READ VS(3)
311F CB 5F       1630        BIT  3,A    * POSITIVE OR NEGATIVE ?
3121 28 19       1640        JR   Z,NNN
3123 E6 07       1650        AND  07H
3125 67          1660        LD   H,A
3126 3A F0 FF    1670        LD   A,(0FFF0H)
3129 6F          1680        LD   L,A
312A 06 09       1780 A3A    LD   B,9
312C CB 25       1790 WWW    SLA  L
312E CB 14       1800        RL   H
3130 10 FA       1810        DJNZ WWW
3132 22 60 3E    1820        LD   (3E60H),HL    * STORE VS(3)
3135 3E 00       1830        LD   A,0
3137 32 33 3E    1840        LD   (3E33H),A
313A 18 1C       1850        JR   A3C
313C 3A F0 FF    1860 NNN    LD   A,(0FFF0H)
313F 2F          1870        CPL
3140 6F          1880        LD   L,A
3141 3A F2 FF    1890        LD   A,(0FFF2H)
3144 2F          1900        CPL
3145 E6 07       1910        AND  07H
3147 67          1920        LD   H,A
3148 3E 01       1950        LD   A,01H         * STORE SIGN
314A 32 33 3E    1960        LD   (3E33H),A
314D 06 00       1970        LD   B,0
314F CB 25       1980 DDD    SLA  L
3151 CB 14       1990        RL   H
3153 10 FA       2000        DJNZ DDD
```

```
3155 22 60 3E       2010          LD   (3E60H),HL
3158 ED 5B 62 3E    2020 A3C      LD   DE,(3E62H)     * VS(2)
315C DD 21 02 3E    2030          LD   IX,3E02H       * A3
3160 CD 9A 39       2040          CALL MULT
3163 06 F6          2050          LD   B,0F6H
3165 3E 00          2060          LD   A,0
3167 CD 58 39       2070          CALL SHIFT
316A 3A 34 3E       2080          LD   A,(3E34H)
316D 00             2090          NOP
316E CB 47          2100          BIT  0,A
3170 28 03          2110          JR   Z,A3
3172 CD 8A 39       2120          CALL COMP
3175 CD 81 39       2130 A3       CALL ADD
3178 ED 5B 64 3E    2140          LD   DE,(3E64H)     * VS(1)
317C DD 21 03 3E    2150          LD   IX,3E03H       * A4
3180 CD 9A 39       2160          CALL MULT
3183 06 F9          2170          LD   B,0F9H
3185 3E 00          2180          LD   A,0
3187 CD 58 39       2190          CALL SHIFT
318A 3A 35 3E       2200          LD   A,(3E35H)
318D 3C             2210          INC  A
318E CB 7F          2220          BIT  7,A
3190 28 03          2230          JR   Z,A4
3192 CD 8A 39       2240          CALL COMP
3195 CD 81 39       2250 A4       CALL ADD          * VD(3)
3198 0E 00          2260          LD   C,0
319A 2A 5A 3E       2270          LD   HL,(3E5AH)   * GET VP(3)
319D 3A 3A 3E       2280          LD   A,(3E3AH)
31A0 CB 7F          2290          BIT  7,A
31A2 28 03          2300          JR   Z,A7
31A4 CD 8A 39       2310          CALL COMP
31A7 CD 81 39       2320 A7       CALL ADD            * VQ(3)
31AA D9             2330          EXX
31AB DD 21 48 3E    2340          LD   IX,3E48H
31AF FD 21 38 3E    2350          LD   IY,3E38H
31B3 CD 00 39       2360          CALL TTT
31B6 22 56 3E       2370          LD   (3E56H),HL     * STORE VQ(3)
31B9 3E 00          2380          LD   A,0
31BB 21 00 00       2390          LD   HL,0
31BE 0E 00          2400          LD   C,0
31C0 D9             2410          EXX
31C1 DD 21 10 3E    2420          LD   IX,3E10H       * B1
31C5 ED 5B 5E 3E    2430          LD   DE,(3E5EH)     * U(2)
31C9 CD 9A 39       2440          CALL MULT
31CC 3A 47 3E       2450          LD   A,(3E47H)
31CF 06 F8          2460          LD   B,0F8H
31D1 3A 37 3E       2470          LD   A,(3E37H)
31D4 00             2480          NOP
31D5 CB 47          2490          BIT  0,A
31D7 28 03          2500          JR   Z,B1
31D9 CD 8A 39       2510          CALL COMP
31DC CD 81 39       2520 B1       CALL ADD
31DF DD 23          2530          INC  IX             * B2
31E1 ED 5B 56 3E    2540          LD   DE,(3E56H)    * VQ(3)
31E5 CD 9A 39       2550          CALL MULT
31E8 06 F9          2560          LD   B,0F9H
```

```
31EA 3A 48 3E       2570           LD    A,(3E48H)
31ED CD 58 39       2580           CALL  SHIFT
31F0 3A 38 3E       2590           LD    A,(3E38H)
31F3 3C             2600           INC   A
31F4 CB 47          2610           BIT   0,A
31F6 28 03          2620           JR    Z,B2
31F8 CD 8A 39       2630           CALL  COMP
31FB CD 81 39       2640 B2        CALL  ADD
31FE DD 23          2650           INC   IX          * B3
3200 ED 5B 58 3E    2660           LD    DE,(3E58H)  * VO(2)
3204 CD 9A 39       2670           CALL  MULT
3207 06 F8          2680           LD    B,0F8H
3209 3A 49 3E       2690           LD    A,(3E49H)
320C CD 58 39       2700           CALL  SHIFT
320F 3A 39 3E       2710           LD    A,(3E39H)
3212 00             2720           NOP
3213 CB 47          2730           BIT   0,A
3215 28 03          2740           JR    Z,B3
3217 CD 8A 39       2750           CALL  COMP
321A CD 81 39       2760 B3        CALL  ADD         * U(3)
321D D9             2770           EXX
3239 E5             2840           PUSH  HL
323A 79             2850           LD    A,C
323B D9             2860           EXX
323C E1             2870           POP   HL
323D 4F             2880           LD    C,A
323E DD 21 46 3E    2890           LD    IX,3E46H
3242 FD 21 36 3E    2900           LD    IY,3E36H
3246 CD 00 39       2910           CALL  TTT
3249 22 5C 3E       2920           LD    (3E5CH),HL
324C D9             2930           EXX
324D                2935 *************** MODIFICATION ***************
324D 79             2940           LD    A,C
324E CB 7F          2950           BIT   7,A
3250 20 21          2960           JR    NZ,LOOPA
3252 E6 FF          2970           AND   0FFH
3254 20 18          2980           JR    NZ,SATU   * SATURATED ?
3256 7C             2990           LD    A,H
3257 E6 F8          3000           AND   0F8H
3259 20 13          3010           JR    NZ,SATU
325B 7D             3020           LD    A,L
325C 2F             3030           CPL
325D E6 0C          3040           AND   0CH
325F 06 02          3050           LD    B,02H     * KEEP BITS 4 THRU 13
3261 CB 25          3060 RH        SLA   L
3263 CB 14          3070           RL    H
3265 10 FA          3080           DJNZ  RH
3267 6F             3090           LD    L,A
3268 7C             3100           LD    A,H
3269 2F             3110           CPL
326A E6 7F          3120           AND   7FH
326C 18 27          3130           JR    OUT
326E 3E 00          3140 SATU      LD    A,0       * OUTPUT 10 V
3270 6F             3150           LD    L,A
3271 18 22          3160           JR    OUT
3273 2F             3170 LOOPA     CPL
3274 E6 7F          3180           AND   7FH
```

```
3276 20 19        3190          JR    NZ,SATU1
3278 7C           3200          LD    A,H
3279 2F           3210          CPL
327A E6 F8        3220          AND   0F8H
327C 20 13        3230          JR    NZ,SATU1
327E 7D           3240          LD    A,L
327F 2F           3250          CPL
3280 E6 0C        3260          AND   0CH
3282 06 02        3270          LD    B,02H     * KEEP BITS 4 THRU 13
3284 CB 25        3280 WEN      SLA   L
3286 CB 14        3290          RL    H
3288 10 FA        3300          DJNZ  WEN
328A 6F           3310          LD    L,A
328B 7C           3320          LD    A,H
328C 2F           3330          CPL
328D F6 80        3340          OR    80H
328F 18 04        3350          JR    OUT
3291 2E 0C        3360 SATU1    LD    L,0CH     * OUTPUT - 10 V
3293 3E FF        3370          LD    A,0FFH
3295 32 F1 FF     3380 OUT      LD    (0FFF1H),A  * INPUT CONTROL SIGNAL
3298 7D           3390          LD    A,L         * TO D/A CONVERTER
3299 32 F2 FF     3400          LD    (0FFF2H),A
329C CD A0 34     3410          CALL  DISPL
329F              3415 **************** UPDATING ****************
329F 21 39 3E     3420          LD    HL,3E39H
32A2 06 0A        3430          LD    B,0AH
32A4 7E           3440 QQQ      LD    A,(HL)    * UPDATING SIGN
32A5 23           3450          INC   HL
32A6 77           3460          LD    (HL),A
32A7 2B           3470          DEC   HL
32A8 2B           3480          DEC   HL
32A9 10 F9        3490          DJNZ  QQQ
32AB 21 49 3E     3500          LD    HL,3E49H
32AE 06 0A        3510          LD    B,0AH
32B0 7E           3520 QQ       LD    A,(HL)    * UPDATING EXPONENT
32B1 23           3530          INC   HL
32B2 77           3540          LD    (HL),A
32B3 2B           3550          DEC   HL
32B4 2B           3560          DEC   HL
32B5 10 F9        3570          DJNZ  QQ
32B7 21 62 3E     3580          LD    HL,3E62H
32BA 06 0A        3590          LD    B,0AH
32BC 11 05 00     3600          LD    DE,0005H
32BF C6 00        3610          ADD   0
32C1 7E           3620 YY       LD    A,(HL)    * UPDATING MANTISSAS
32C2 23           3630          INC   HL
32C3 4E           3640          LD    C,(HL)
32C4 23           3650          INC   HL
32C5 77           3660          LD    (HL),A
32C6 23           3670          INC   HL
32C7 71           3680          LD    (HL),C
32C8 ED 52        3690          SBC   HL,DE
32CA 10 F5        3700          DJNZ  YY
32CC 3E 12        3710          LD    A,12H
32CE 32 F3 FF     3720          LD    (0FFF3H),A
32D1 DB 10        3730 CHECK    IN    10H       * IS SAMPLING TIME OVER ?
32D3 A7           3740          AND   A
32D4 28 FB        3750          JR    Z,CHECK
32D6 C3 4C 30     3760          JP    MAIN
```

```
35B2                0100 *             SUBROUTINE TTT
35B2                0110 ***************************************
3CA0                0120          ST    3CA0H
3CA0                0125 COMP     EQU   3470H
3CA0 D9             0130 TTT      EXX               * SHIFT TO C'H'L'
3CA1 79             0140          LD    A,C         * CHECK SIGN
3CA2 CB 27          0150          SLA   A
3CA4 30 3D          0160          JR    NC,T1
3CA6 3E 01          0170          LD    A,01H       * NEGATIVE SIGN
3CA8 FD 77 00       0180          LD    (IY+0),A
3CAB CD 70 34       0185          CALL  COMP
3CAE 79             0190 T5       LD    A,C         * OVERFLOW ?
3CAF CB 7F          0200          BIT   7,A
3CB1 20 37          0210          JR    NZ,FULL
3CB3 06 07          0220          LD    B,07H       * WHICH BIT IS SET ?
3CB5 CB 27          0230          SLA   A
3CB7 CB 27          0240 T3       SLA   A
3CB9 38 02          0250          JR    C,T2
3CBB 10 FA          0260          DJNZ  T3
3CBD 78             0270 T2       LD    A,B         * EXPONENT = 0 ?
3CBE E6 FF          0280          AND   0FFH
3CC0 28 13          0290          JR    Z,ZERO
3CC2 04             0300          INC   B           * OBTAIN EXPONENT
3CC3 DD 70 00       0310          LD    (IX+0),B
3CC6 CB 39          0320 T4       SRL   C           * SHIFT MANTISSA
3CC8 CB 1C          0330          RR    H
3CCA CB 1D          0340          RR    L
3CCC 10 F8          0350          DJNZ  T4
3CCE C9             0360          RET
3CCF 3E 00          0362 RR       LD    A,0         * EXPONENT = 0
3CD1 DD 77 00       0365          LD    (IX+0),A
3CD4 C9             0368          RET
3CD5 CB 7C          0370 ZERO     BIT   7,H         * BIT 15 SET ?
3CD7 28 F6          0380          JR    Z,RR
3CD9 CB 3C          0390          SRL   H
3CDB CB 1D          0400          RR    L
3CDD 3E 01          0410          LD    A,01H
3CDF DD 77 00       0420          LD    (IX+0),A
3CE2 C9             0430          RET
3CE3 3E 00          0440 T1       LD    A,0         * POSITIVE SIGN
3CE5 FD 77 00       0450          LD    (IY+0),A
3CE8 18 C4          0460          JR    T5
3CEA 21 00 40       0470 FULL     LD    HL,4000H    * MAX. VALUE
3CED 3E 01          0480          LD    A,01H
3CEF FD 77 00       0490          LD    (IY+0),A
3CF2 3E 09          0500          LD    A,09H
3CF4 DD 77 00       0510          LD    (IX+0),A
3CF7 C9             0520          RET
```

```
3381                0100 *           SUBROUTINE MULT
3381                0110 ****************************************
3CE5                0120        ST   3CE5H
3CE5 06 08          0130        LD   B,08H      * INIT. COUNTER
3CE7 3E 00          0140        LD   A,0        * RESET CHL
3CE9 67             0150        LD   H,A
3CEA 6F             0160        LD   L,A
3CEB 4F             0170        LD   C,A
3CEC DD CB 00 3E    0180 LOOP1  SRL  (IX+0)     * SHIFT MULTIPLIER
3CF0 30 02          0190        JR   NC,SKIP
3CF2 19             0200        ADD  HL,DE
3CF3 89             0210        ADC  C
3CF4 CB 23          0220 SKIP   SLA  E          * SHIFT CDE TO LEFT
3CF6 CB 12          0230        RL   D
3CF8 CB 11          0240        RL   C
3CFA 10 F0          0250        DJNZ LOOP1
3CFC 4F             0260        LD   C,A        * RESULT IN CHL
3CFD C9             0270        RET
```

```
330C                0100 *          SUBROUTINE ADD
330C                0110 ***************************************
3C30                0140        ST   3C30H
3C30 79             0150 ADD    LD   A,C  * SAVE CHL
3C31 E5             0160        PUSH HL
3C32 D9             0170        EXX
3C33 D1             0180        POP  DE  * RETRIVE HL FROM STACK
3C34 19             0190        ADD  HL,DE  * ADDING
3C35 89             0200        ADC  C
3C36 4F             0210        LD   C,A  * MOVE DATA FROM A TO C
3C37 D9             0220        EXX
3C38 C9             0230        RET
```

```
3327                0100 *           SUBROUTINE COMP
3327                0110 ****************************************
3C00                0140        ST   3C00H
3C00 7D             0150        LD   A,L      * 2'S COMP. OF L
3C01 2F             0160        CPL
3C02 C6 01          0170        ADD  01H
3C04 6F             0180        LD   L,A
3C05 7C             0190        LD   A,H      * 2'S COMP. OF H
3C06 2F             0200        CPL
3C07 CE 00          0210        ADC  0
3C09 67             0220        LD   H,A
3C0A 79             0230        LD   A,C      * 2'S COMP. OF C
3C0B 2F             0240        CPL
3C0C CE 00          0250        ADC  0
3C0E 4F             0260        LD   C,A
3C0F C9             0270        RET
```

```
3427              0100 *            SUBROUTINE SHIFT
3427              0110 ****************************************
3C70              0115        ST    3C70H
3C70 80           0120 SHIFT  ADD   B          * A + B -> A
3C71 E6 FF        0125        AND   0FFH       * A = 0 ?
3C73 28 0F        0126        JR    Z,S5
3C75 CB 7F        0130        BIT   7,A        * NEGATIVE ?
3C77 28 0C        0140        JR    Z,S1
3C79 ED 44        0150        NEG              * 2'S COMPLEMENT
3C7B 47           0160        LD    B,A
3C7C CB 39        0170 S2     SRL   C          * SHIFT MANTISSA
3C7E CB 1C        0180        RR    H
3C80 CB 1D        0190        RR    L
3C82 10 F8        0200        DJNZ  S2
3C84 C9           0210 S5     RET              * RETURN
3C85 47           0220 S1     LD    B,A
3C86 CB 25        0230 S3     SLA   L    * SHIFT MANTISSA TO LEFT
3C88 CB 14        0240        RL    H
3C8A CB 11        0250        RL    C
3C8C CB 79        0260        BIT   7,C        * OVERFLOW ?
3C8E 20 03        0270        JR    NZ,S4
3C90 10 F4        0280        DJNZ  S3
3C92 C9           0290        RET              * RETURN
3C93 21 FF FF     0300 S4     LD    HL,0FFFFH  * MAX. POST. VALUE
3C96 0E 7F        0310        LD    C,07FH
3C98 C9           0320        RET
```

```
3942              0010 *            SUBROUTINE DISPLAY              *
3942              0020 ****************************************
3500              0100        ST    3500H
3500 3E D6        0110        LD    A,0D6H     * ASCII " V "
3502 CD FA 00     0120        CALL  000372
3505 3E BD        0130        LD    A,0BDH     * ASCII " = "
3507 CD FA 00     0140        CALL  000372
350A 3A 33 3E     0150        LD    A,(3E33H)  * SIGN OF V(2)
350D CB 47        0160        BIT   0,A
350F 20 04        0170        JR    NZ,NEG
3511 3E AB        0180        LD    A,0ABH     * ASCII " + "
3513 18 02        0190        JR    VALUE
3515 3E AD        0200 NEG    LD    A,0ADH     * ASCII " - "
3517 CD FA 00     0210 VALUE  CALL  000372
351A 2A 60 3E     0220        LD    HL,(3E60H)  * MANTISSA
351D 7C           0230        LD    A,H     * CONVERT LOWER NIBBLE
351E E6 0F        0240        AND   0FH     * OF H TO ASCII CODE
3520 FE 0A        0250        CP    0AH
3522 F2 2A 35     0260        JP    P,V1
```

```
3525 C6 B0       0270         ADD  0B0H
3527 C3 2C 35    0280         JP   V2
352A C6 B7       0290 V1      ADD  0B7H
352C CD FA 00    0300 V2      CALL 000372
352F 7D          0310         LD   A,L   * CONVERT UPPER NIBBLE
3530 CB 3F       0320         SRL  A     * OF L TO ASCII CODE
3532 CB 3F       0330         SRL  A
3534 CB 3F       0340         SRL  A
3536 CB 3F       0350         SRL  A
3538 FE 0A       0360         CP   0AH
353A F2 42 35    0370         JP   P,V3
353D C6 B0       0380         ADD  0B0H
353F C3 44 35    0390         JP   V4
3542 C6 B7       0400 V3      ADD  0B7H
3544 CD FA 00    0410 V4      CALL 000372
3547 7D          0420         LD   A,L   * CONVERT LOWER NIBBLE
3548 E6 0F       0430         AND  0FH   * OF L TO ASCII CODE
354A FE 0A       0440         CP   0AH
354C F2 54 35    0450         JP   P,V5
354F C6 B0       0460         ADD  0B0H
3551 C3 56 35    0470         JP   NEXT
3554 C6 B7       0480 V5      ADD  0B7H
3556 CD FA 00    0490 NEXT    CALL 000372
3559 CD F8 00    0500         CALL 000370  * SPACE
355C CD F8 00    0510         CALL 000370
355F 3E D0       0520         LD   A,0D0H  * ASCII " P "
3561 CD FA 00    0530         CALL 000372
3564 3E BD       0540         LD   A,0BDH  * ASCII " = "
3566 CD FA 00    0550         CALL 000372
3569 3A 38 3E    0560         LD   A,(3E38H)  * SIGN OF P(2)
356C CB 47       0570         BIT  0,A
356E 20 05       0580         JR   NZ,NEG1
3570 3E AB       0590         LD   A,0ABH  * ASCII " + "
3572 C3 77 35    0600         JP   P1
3575 3E AD       0610 NEG1    LD   A,0ADH  * ASCII " - "
3577 CD FA 00    0620 P1      CALL 000372
357A 2A 56 3E    0630         LD   HL,(3E56H) * MANTISSA OF P(2)
357D 7C          0640         LD   A,H     * CONVERT LOWER NIBBLE
357E E6 0F       0650         AND  0FH     * OF H TO ASCII CODE
3580 FE 0A       0660         CP   0AH
3582 F2 8A 35    0670         JP   P,P2
3585 C6 B0       0680         ADD  0B0H
3587 C3 8C 35    0690         JP   P3
358A C6 B7       0700 P2      ADD  0B7H
358C CD FA 00    0710 P3      CALL 000372
358F 7D          0720         LD   A,L  * CONVERT UPPER NIBBLE
3590 CB 3F       0730         SRL  A    * OF L TO ASCII CODE
3592 CB 3F       0740         SRL  A
3594 CB 3F       0750         SRL  A
3596 CB 3F       0760         SRL  A
3598 FE 0A       0770         CP   0AH
359A F2 A2 35    0780         JP   P,P4
359D C6 B0       0790         ADD  0B0H
```

```
359F C3 A4 35              JP    P5
35A2 C6 B7           P4    ADD   0B7H
35A4 CD FA 00        P5    CALL  000372
35A7 7D                    LD    A,L   * CONVERT LOWER NIBBLE
35A8 E6 0F                 AND   0FH   * OF L TO ASCII CODE
35AA FE 0A                 CP    0AH
35AC F2 B4 35              JP    P,P6
35AF C6 B0                 ADD   0B0H
35B1 C3 B6 35              JP    FINAL
35B4 C6 B7           P6    ADD   0B7H
35B6 CD FA 00        FINAL CALL  000372
35B9 CD F8 00              CALL  000370   * SPACE
35BC CD F8 00              CALL  000370
35BF C9                    RET            * RETURN
```

```
351F                 ********** SUBROUTINE LAST ***********
3600                       ST    3600H
3600 21 CD 01              LD    HL,01CDH   * INITIALIZATION
3603 22 07 3E              LD    (3E07H),HL
3606 21 00 00              LD    HL,0
3609 22 7B 3E              LD    (3E7BH),HL
360C 22 7D 3E              LD    (3E7DH),HL
360F 2A 07 3E        LOOP  LD    HL,(3E07H) * SHIFT LEFT 6 TIMES
3612 45                    LD    B,L
3613 CB 25                 SLA   L
3615 CB 14                 RL    H
3617 CB 25                 SLA   L
3619 CB 14                 RL    H
361B CB 25                 SLA   L
361D CB 14                 RL    H
361F CB 25                 SLA   L
3621 CB 14                 RL    H
3623 CB 25                 SLA   L
3625 CB 14                 RL    H
3627 CB 25                 SLA   L
3629 CB 14                 RL    H
362B 7C                    LD    A,H
362C 32 F0 FF              LD    (0FFF0H),A   * INPUT TO D/A
362F 78                    LD    A,B
3630 32 F2 FF              LD    (0FFF2H),A
3633 3E D0                 LD    A,0D0H     * ASCII " P "
3635 CD FA 00              CALL  000372
3638 3E C2                 LD    A,0C2H     * ASCII " B "
363A CD FA 00              CALL  000372
363D 3E BD                 LD    A,0BDH     * ASCII " = "
363F CD FA 00              CALL  000372
3642 3E 12                 LD    A,12H    * INIT. A/D TO READ P(2)
```

```
3644 32 F3 FF     8480           LD    (0FFF3H),A
3647 3A F1 FF     8490 LOOP1     LD    A,(0FFF1H)  * READY TO BE READ ?
364A E6 80        8500           AND   80H
364C 28 F9        8510           JR    Z,LOOP1
364E 3A F1 FF     8520 LOOP2     LD    A,(0FFF1H)
3651 E6 80        8530           AND   80H
3653 20 F9        8540           JR    NZ,LOOP2
3655 3A F2 FF     8550           LD    A,(0FFF2H)  * READ UPPER 4 BIT
3658 E6 0F        8560           AND   0FH
365A 67           8570           LD    H,A
365B 3A F0 FF     8580           LD    A,(0FFF0H)  * READ LOWER BYTE
365E 6F           8590           LD    L,A
365F CD 0F 37     8600           CALL  SCREEN
3662 3E 00        8610           LD    A,0   * INIT. A/D TO READ V(2)
3664 32 F3 FF     8620           LD    (0FFF3H),A
3667 CD C7 36     8630           CALL  DEL1
366A 11 FF 07     8640           LD    DE,07FFH  * VALUE 0 OF A/D
366D 3A 7B 3E     8650           LD    A,(3E7BH)  * MINIMIZE THE BIAS
3670 C6 00        8660           ADD   0
3672 ED 52        8670           SBC   HL,DE
3674 85           8680           ADD   L
3675 CB 3F        8690           SRL   A
3677 32 7B 3E     8700           LD    (3E7BH),A
367A CD C7 36     8710           CALL  DEL1
367D 3E D6        8720           LD    A,0D6H    * ASCII " V "
367F CD FA 00     8730           CALL  000372
3682 3E C2        8740           LD    A,0C2H    * ASCII " B "
3684 CD FA 00     8750           CALL  000372
3687 3E BD        8760           LD    A,0BDH    * ASCII " = "
3689 CD FA 00     8770           CALL  000372
368C 3E 00        8780           LD    A,0   * INIT. A/D TO READ V(2)
368E 32 F3 FF     8790           LD    (0FFF3H),A
3691 CD C7 36     8800           CALL  DEL1
3694 CD C7 36     8810           CALL  DEL1
3697 3A F2 FF     8820           LD    A,(0FFF2H)  * READ V(2)
369A E6 0F        8830           AND   0FH
369C 67           8840           LD    H,A
369D 3A F0 FF     8850           LD    A,(0FFF0H)
36A0 6F           8860           LD    L,A
36A1 CD 0F 37     8870           CALL   SCREEN
36A4 11 FF 07     8880           LD    DE,07FFH  * ZERO OF D/A
36A7 3A 7D 3E     8890           LD    A,(3E7DH) * MINIMIZE THE BIAS
36AA C6 00        8900           ADD   0
36AC ED 52        8910           SBC   HL,DE
36AE 85           8920           ADD   L
36AF CB 3F        8930           SRL   A
36B1 32 7D 3E     8940           LD    (3E7DH),A
36B4 3E 12        8950           LD    A,12H
36B6 3E 12        8960           LD    A,12H  * INIT. A/D TO READ P(2)
36B8 CD C7 36     8970           CALL  DEL1
36BB CD C7 36     8980           CALL  DEL1
36BE CD C7 36     8990           CALL  DEL1
36C1 CD C7 36     9000           CALL  DEL1
36C4 C3 0F 36     9010           JP    LOOP
```

```
36C7                  9011          ST    36C7H
36C7                  9012 * THIS PART CHECKS IF ANY INPUT FROM THE
36C7                  9013 * KEYBOARD IS MADE TO EITHER INC. OR DEC.
36C7                  9014 * THE BIAS VOLTAGE TO A/D TO READ THE
36C7                  9015 * PENDULUM POSITION P(2) OR TO JUMP BACK
36C7                  9016 * TO MAIN PROGRAM.
36C7 06 3F            9020 DELI     LD    B,3FH  * INIT. COUNTER
36C9 DB 00            9030 JM       IN    0,A
36CB FE C4            9040          CP    'D'
36CD CC E0 36         9050          CALL  Z,DEC
36D0 DB 00            9060          IN    0,A
36D2 FE C9            9070          CP    'I'
36D4 CC EB 36         9080          CALL  Z,INC
36D7 DB 00            9090          IN    0,A
36D9 FE C5            9100          CP    'E'
36DB 28 19            9110          JR    Z,END
36DD 10 EA            9120          DJNZ  JM
36DF C9               9130          RET
36E0                  9135 * DEC. THE OUTPUT VOLTAGE TO D/A
36E0 2A 07 3E         9140 DEC      LD    HL,(3E07H)
36E3 23               9150          INC   HL
36E4 22 07 3E         9160          LD    (3E07H),HL
36E7 CD 09 37         9170          CALL  DELAY
36EA C9               9180          RET
36EB                  9185 * INC. THE OUTPUT VOLTAGE TO D/A
36EB 2A 07 3E         9190 INC      LD    HL,(3E07H)
36EE 2B               9200          DEC   HL
36EF 22 07 3E         9210          LD    (3E07H),HL
36F2 CD 09 37         9220          CALL  DELAY
36F5 C9               9230          RET
36F6                  9235 * SAVE LAST 2 BITS OF D/A
36F6                  9236 * JUMP BACK TO MAIN PROGRAM
36F6 3A 07 3E         9240 END      LD    A,(3E07H)
36F9 E6 03            9250          AND   03H
36FB 32 0D 3E         9260          LD    (3E0DH),A
36FE 3A 7B 3E         9261          LD    A,(3E7BH)    * TO ACCOMODATE VOLTAGE
3701 D6 04            9262          SUB   04H          * DROP OF 0.002 VOLT
3703 32 7B 3E         9263          LD    (3E7BH),A
3706 C3 1C 30         9270          JP    301CH
3709 0E 4F            9280 DELAY    LD    C,4FH        * TIME DELAY
370B 0D               9290 LAB      DEC   C
370C 20 FD            9300          JR    NZ,LAB
370E C9               9310          RET
370F                  9315 * DISPLAY THE DATA STORED IN LAST 12
370F                  9316 * BITS OF HL REGISTERS ON CRT
370F 7C               9320 SCREEN LD    A,H
3710 E6 7F            9330          AND   7FH
3712 F6 B0            9340          OR    0B0H
3714 FE BA            9350          CP    0BAH
3716 F4 43 37         9360          CALL  P,HEX
3719 CD FA 00         9370          CALL  000372
371C 7D               9380          LD    A,L
371D CB 3F            9390          SRL   A
371F CB 3F            9400          SRL   A
3721 CB 3F            9410          SRL   A
```

```
3723 CB 3F          9420          SRL  A
3725 F6 B0          9430          OR   0B0H
3727 FE BA          9440          CP   0BAH
3729 F4 43 37       9450          CALL P,HEX
372C CD FA 00       9460          CALL 000372
372F 7D             9470          LD   A,L
3730 E6 0F          9480          AND  0FH
3732 F6 B0          9490          OR   0B0H
3734 FE BA          9500          CP   0BAH
3736 F4 43 37       9510          CALL P,HEX
3739 CD FA 00       9520          CALL 000372
373C CD F8 00       9530          CALL 000370
373F CD F8 00       9540          CALL 000370
3742 C9             9550          RET
3743 C6 07          9560 HEX      ADD  07H
3745 C9             9570          RET
```

```
3795                0090 ****  SUBROUTINE PENDIS  ****
3795                0100 SCREEN EQU  3712H
3800                0110          ST   3800H
3800 3E 12          0111          LD   A,12H  * INIT. A/D TO READ P(2)
3802 32 F3 FF       0112          LD   (0FFF3H),A
3805 3E 05          0114          LD   A,05H  * DELAY
3807 06 FF          0115 DEL1     LD   B,0FFH
3809 00             0116 DEL      NOP
380A 10 FD          0117          DJNZ DEL
380C 3D             0118          DEC  A
380D 20 F8          0119          JR   NZ,DEL1
380F 3E D0          0120 AGAIN    LD   A,0D0H  * ASCII " P "
3811 CD FA 00       0130          CALL 000372
3814 3E BD          0140          LD   A,0BDH  * ASCII " = "
3816 CD FA 00       0150          CALL 000372
3819 3E 12          0160          LD   A,12H  * INIT. A/D TO READ P(2)
381B 32 F3 FF       0170          LD   (0FFF3H),A
381E 3A F1 FF       0180 POST     LD   A,(0FFF1H)  * READY TO BE READ ?
3821 E6 80          0190          AND  80H
3823 28 F9          0200          JR   Z,POST
3825 3A F1 FF       0210 POST1    LD   A,(0FFF1H)
3828 E6 80          0220          AND  60H
382A 20 F9          0230          JR   NZ,POST1
382C 3A F2 FF       0240          LD   A,(0FFF2H)  * READ P(2)
382F E6 08          0250          AND  08H    * CONVERT READING
3831 28 24          0260          JR   Z,SKIP
3833 3E 00          0263          LD   A,0
3835 32 38 3E       0266          LD   (3E38H),A
3838 3E AB          0270          LD   A,0ABH  * ASCII " + "
383A CD FA 00       0280          CALL 000372
383D 3A F2 FF       0290          LD   A,(0FFF2H)  * READ UPPER NIBBLE
3840 E6 07          0300          AND  07H
3842 67             0310          LD   H,A
3843 3A F0 FF       0320          LD   A,(0FFF0H)  * READ LOWER BYTE
3846 6F             0330          LD   L,A
```

```
3847 ED 5B 7B 3E  0340        LD   DE,(3E7BH)  * TAKE CARE THE BIAS
384B ED 52        0350        SBC  HL,DE
384D 7C           0360        LD   A,H
384E E6 80        0370        AND  80H
3850 28 20        0380        JR   Z,SKIP2
3852 21 00 00     0390        LD   HL,0
3855 18 1B        0400        JR   SKIP2
3857 3E 01        0403 SKIP   LD   A,01H
3859 32 38 3E     0407        LD   (3E38H),A
385C 3E AD        0410        LD   A,0ADH   * ASCII " - "
385E CD FA 00     0420        CALL 000372
3861 3A F2 FF     0430        LD   A,(0FFF2H)  * READ UPPER NIBBLE
3864 2F           0440        CPL
3865 E6 07        0450        AND  07H
3867 67           0460        LD   H,A
3868 3A F0 FF     0470        LD   A,(0FFF0H)  * READ LOWER BYTE
386B 2F           0480        CPL
386C 6F           0490        LD   L,A
386D ED 5B 7B 3E  0500        LD   DE,(3E7BH)  * ADD BIAS
3871 19           0510        ADD  HL,DE
3872 22 58 3E     0515 SKIP2  LD   (3E58H),HL  * SAVE INIT. COND.
3875 CD 12 37     0520        CALL SCREEN
3878 DB 00        0530        IN   0,A
387A FE D2        0540        CP   'R'   * RETURN TO MAIN PROGRAM
387C 28 02        0550        JR   Z,END
387E 18 8F        0560        JR   AGAIN
3880 21 00 3A     0570 END    LD   HL,3A00H  * INIT. STORE ADDRESS
3883 22 2E 3E     0580        LD   (3E2EH),HL
3886 C9           0590        RET


3407              0100 *      SUBROUTINE STORE
3807              0101 ****************************************
38D0              0105        ST   38D0H
38D0 3A 2D 3E     0110 STORE  LD   A,(3E2DH)  * CHECK COUNTER
38D3 3C           0120        INC  A
38D4 32 2D 3E     0130        LD   (3E2DH),A
38D7 CB 47        0140        BIT  0,A        * RETURN IF RESET
38D9 28 24        0150        JR   Z,RETURN
38DB 3A 2F 3E     0160        LD   A,(3E2FH)  * CHECK ADDRESS
38DE FE 3D        0170        CP   3DH
38E0 28 1D        0180        JR   Z,RETURN
38E2 DD 2A 2E 3E  0190        LD   IX,(3E2EH)  * GET POINTER
38E6 2A 58 3E     0200        LD   HL,(3E58H)  * GET P(2)
38E9 3A 38 3E     0210        LD   A,(3E38H)
38EC DD 77 00     0220        LD   (IX+0),A     * STORE P(2)
38EF DD 23        0230        INC  IX
38F1 DD 74 00     0240        LD   (IX+0),H
38F4 DD 23        0250        INC  IX
38F6 DD 75 00     0260        LD   (IX+0),L
38F9 DD 23        0270        INC  IX
38FB DD 22 2E 3E  0280        LD   (3E2EH),IX  * RESET COUNTER
38FF C9           0290 RETURN RET
```

Appendix C

Memory Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3E00	A1	A2	A3	A4												
3E10	B1	B2	B3													
3E20														DATA COUNT.	DATA STORING INDEX	
3E30	SIGN Vd(3)	SIGN Vd(2)	SIGN Vd(1)	SIGN Vs(3)	SIGN Vs(2)	SIGN Vs(1)	SIGN U(2)	SIGN U(1)	SIGN Vq(2)	SIGN Vq(1)	SIGN Vp(3)					
3E40	EXP Vd(3)	EXP Vd(2)	EXP Vd(1)	EXP Vs(3)	EXP Vs(2)	EXP Vs(1)	EXP U(2)	EXP U(1)	EXP Vq(2)	EXP Vq(1)	EXP Vp(3)					
3E50	MANTISSA Vd(3)	Vd(3)	MANTISSA Vd(2)	Vd(2)	MANTISSA Vd(1)	Vd(1)	MANTISSA Vq(3)	Vq(3)	MANTISSA Vq(2)	Vq(2)	MANTISSA Vp(3)	Vp(3)	MANTISSA U(3)	U(3)	MANTISSA U(2)	U(2)
3E60	MANTISSA Vs(3)	Vs(3)	MANTISSA Vs(2)	Vs(2)	MANTISSA Vs(1)	Vs(1)										
3E70	COUNTER	TEMP. MEMO.								BIAS INIT.	BIAS INIT.	BIAS PEN.	BIAS PEN.	BIAS VEL.	BIAS VEL.	

Appendix C, Memory Map

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THE APPLICATION OF LOCALLY OPTIMAL CONTROL WITH DIGITAL COMPENSATION TO A NATURALLY UNSTABLE SYSTEM

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ABSTRACT OF MASTER'S THESIS

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ABSTRACT

The development of microprocessors has provided the capablity of implementing complex control strategies. There is a need to develop analysis and design techniques for the development of digital control strategies. The objective of this research was to apply digital control to a naturally unstable system. The technique of locally optimal control with digital compensation was used. An inverted pendulum mounted on a motor driven cart was chosen as the naturally unstable system.

Mathematical models were first developed and then the digital models were derived by employing Z-transform techniques. The stability of the system was checked by the methods of root locus and Routh array. A computer simulation was performed and shown that the naturally unstable system could be made stable.

A microcomputer was programmed to control the system based on the equations developed in the analysis. The sampling period was decided to be 10 milliseconds.

The cart was allowed to move on a carpeted track, the ends of which were propped up like small ramps, for eliminating the effect of the bias. The results of the experiment showed that the techniques of optimal control with digital compensation could be used to stabilize this naturally unstable system.