DESIGN AND ANALYSIS OF AN INTEGRATED PULSE MODULATED S-BAND POWER AMPLIFIER IN GALLIUM NITRIDE PROCESS

by

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Abstract

The design of power amplifiers in any semi-conductor process is not a trivial exercise and it is often encountered that the simulated solution is significantly different than the results obtained. Oscillatory phenomena occurring either in-band or out of band and sometimes at subharmonic intervals can render a design useless. Other less apparent effects such as jumps, hysteresis and continuous spectrum, often referred to as chaos, can also invalidate a design. All of these problems might have been identified through a more rigorous approach to stability analysis.

Designing for stability is probably the one area of amplifier design that receives the least amount of attention but incurs the most catastrophic of effects if it is not performed properly. Other parameters such as gain, power output, frequency response and even matching may have suitable mitigation paths. But the lack of stability in an amplifier has no mitigating path. In addition to the loss of the design there are the increased production cycle costs, costs involved with investigating and resolving the problem and the costs involved with schedule slips or delays resulting from it.

The Linville or Rollett stability criteria that many microwave engineers follow and rely exclusively on is not sufficient by itself to ensure a stable and robust design. It will be shown that the belief that unconditional stability is obtained through an analysis of the scattering matrix S to determine if $K > 1$ and $|\Delta_S| < 1$ can fail and other tools must be used to validate circuit stability.

With the emphasis being placed on stability, a 1W pulse modulated S-band power amplifier is designed using a battery of analysis tools in addition to the standard Linville or Rollett criteria to rigorously confirm the stability of the circuit. Test measurements are then presented to confirm the stability of the design and illustrate the results.

The research shown contributes to the state of the art by offering a detailed approach to stability design and then applying the techniques to the design of a 1W pulse modulated S-band power amplifier demonstrating the first with 20 nanosecond pulse width switching and single digit nanosecond rise and fall times at 1 Watt power levels.

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Acknowledgements

I would like to express my sincere thanks and appreciation to my friend and learned colleague, Jeff Dimsdle, who has been a great source of knowledge and inspiration over the years and who has helped clarify some of the more challenging aspects of this subject.

Chapter 1 - **Introduction**

"December 7, 1941, a date which will live in infamy" proclaimed president Franklin Delanor Roosevelt in response to the horrific destruction of the Pearl Harbor naval base at the hands of the Japanese in a what was a complete surprise attack due in large part to the lack of a coordinated early warning radar system. The army at the time had five operational mobile sets and had even seen the Japanese planes approaching. But the communications between the fighter director officers and the fighter aircraft was inadequate and the Japanese planes were mistaken to be American B-17 bombers expected in the harbor about the same time [13]. This tragic event magnified the urgency for the development of an effective early warning radar system.

Today's modern radar systems have many more applications besides early warning systems. They are also used in air traffic control networks, radar astronomy, weather prediction, ocean surveillance systems, automotive collision systems, altimeter applications and a host of variations of these [15]. At the heart of many of these systems is the pulse modulated amplifier. Many types of pulse modulation schemes are in use such as FM (frequency modulated), linear, used in chirp radar, and non-linear PM (phase modulated) [15].

This thesis will discuss the proper techniques necessary to design a GaN (Gallium Nitride) based pulse modulated 1 Watt amplifier irrespective of the specific pulse modulation scheme used. The emphasis will be placed on a thorough stability analysis and will explore the conditions that lead to oscillatory or unstable behavior in microwave amplifier circuits. Ways to identify and eliminate them will also be addressed so that early in the process the system can be designed with margin so as to avoid these conditions.

Chapter 2 begins with the building blocks and focuses on the common amplifier types in use today, in broad terms they can be classified as current mode or switch mode amplifiers. A thorough understanding of the amplifier types is imperative to the stability design process.

In chapter 3 the emphasis is on oscillations in linear and nonlinear systems and the necessary condition for steady state oscillation in terms of admittance parameters. Constructive discussion on ways to eliminate oscillations that may be due to power supply feedback, bias network instability, parametric oscillation or thermal feedback is also presented.

Chapter 4 contains a thorough look at linear stability analysis measures involving the Linville or Rollett stability criteria and is based on the work by Aryeh Platzker and Wayne Struble [5]. This Rollett measure is found in every simulator package sold today and is based on an analysis of the scattering matrix S to determine if $K > 1$ and $|\Delta_S| < 1$. This chapter demonstrates four cases of the use of this measure and its failure to predict in all cases the stability of the two port network. This thesis expands upon this work by including the geometric stability measures $Mu1$ and $Mu2$, the results of transient analysis for all four cases and an additional root for all four cases not identified in the original analysis.

In chapter 5 the nonlinear techniques to stability analysis are discussed. The large signal S-parameter analysis is discussed first. The large signal S-parameters differ from the small signal complement in that they include nonlinear amplifier effects and the effects of harmonics. A more detailed analysis follows with the auxiliary generator method and the Nyquist stability analysis.

Chapter 6 is a transitional chapter away from the general stability concepts and analysis's of general amplifier types and architectures to the specific case involving a class AB, GaN based, 1W pulse modulated amplifier. This chapter focuses on the characteristics of the GaN technology and why it is a good choice for high power amplifier circuits.

Thermal analysis is an important part of the design process and affects the reliable operation of the device as well as ensures that thermal feedback issues that can cause instabilities are avoided. The basic concepts and failure mechanisms are outlined in Chapter 7.

The specific design and measurement results of the fabricated 1W pulse modulated amplifier is contained in Chapters 8 and 9 respectively followed by the conclusion of Chapter 10. Many of the techniques described in the previous chapters are pulled together to methodically design the amplifier and present the results.

Chapter 2 - **RF PAs**

2.1 Amplifier Classes

Amplifiers are electronic circuits designed to increase or at least maintain the signal level present at the input. There are a wide variety of amplifiers in use today covering a few mW to MW depending on the application. These are broadly defined by the attempt to preserve the original waveshape seen at the amplifiers input to that occurring at the output. Amplifiers that must maintain the original waveshape seen at its input are known as *linear amplifiers* and those that do not make an attempt to preserve the original waveshape characteristics are known as *non-linear* or *constant envelope amplifiers* [1].

Linear amplifiers are required whenever the modulation scheme introduces an amplitude component or when the modulation scheme is based on amplitude variations such as Amplitude Modulation (AM). Non-linear amplifiers can be used in modulation schemes that do not introduce amplitude variations as part of the modulation process such as Frequency Modulation (FM). Some digital modulation schemes can contain amplitude components requiring the use of linear and sometimes ultra linear amplifiers. Table 2-1 is a partial listing of some common modulation techniques and if a linear amplifier is required.

Linear Amplifier Required	Non-Linear Amplifier can be used
BPSK	GMSK
QPSK	FSK
QAM	GFSK
OFDM	FM
AM	CW
SSB	PM

Table 2-1: Amplifier Type for various modulation formats

Amplifiers are additionally subdivided into types that are simply identified by a letter or a combination of two letters. The main classes of linear amplifiers are A, AB and B. These amplifiers are common place in areas where signal envelope preservation is important such as those identified in Table 2-1. [1]. Class A is the most linear of this group but suffers from low efficiency. These types of amplifiers in general suffer from nonlinearity and spectral effects that not only occur in band but also spill out to adjacent channels [1].

In addition to the linear amplifiers there are a number of nonlinear amplifiers types prominent today. These are denoted C, D, E,F,G,H,J and S with more types appearing all the time. The Class C type operates with much higher efficiency and in a current source configuration similar to a Class A, but its biasing is much different and because of this incurs considerable amounts of distortion. Class D,E,F and S operate in a switch mode operation where the transistor is switched off and on at microwave frequencies for a portion of the RF cycle in order to obtain high efficiencies. Unfortunately one of the drawbacks to this mode of operation is large drain voltages swings which can approach $3.65V_{DD}$[2].

RF Power amplifiers have many important parameters that must be achieved throughout the designed operating environment. Chief among these include the following:

- Output Power
- Gain
- Match
- Linearity
- Stability
- DC Supply Voltage tolerance
- Efficiency
- Robustness
- Bandwidth

Of these important parameters, stability is a topic that seems to receive the least amount of attention in the amplifier design process and this thesis will devote a considerable amount of discussion on it. Often a designer is presented a set of specifications and operating parameters for

the amplifier such as gain, output power, efficiency, bandwidth, input/ output return loss, power supplies available and temperature operating range extremes, but nothing is really specified about stability. It is just assumed that the design will be unconditionally stable to all source and load impedances presented. Many designers run K and B stability criteria from DC to daylight and call it good if it maintains the stability requirements. As Platzker has shown this is not always the case and the conventional stability criteria measurements can and do fail [5].

Linearity and efficiency are also critical parameters but they do not operate in a complementary fashion to one another. Amongst many other specifications a design will dictate a specified efficiency value and as the amplifier stage is driven harder into compression to achieve it the amplifier will compress at the higher drive values generating high levels of harmonics. This phenomena is caused by the cubic term for transconductance nonlinearity and will be described in detail later.

Efficiency is another critical parameter for RF power amplifiers especially when battery operated systems are involved. An amplifier with higher efficiency would relax the constraints upon the battery capacity, reduce heat dissipated throughout the system as regulators and support circuitry could be relaxed, free up board area and ease requirements of the heatsink for RF power devices. Thus amplifier efficiency is critical to good amplifier design and it is this requirement that will dictate the type of amplifier required.

To begin our discussion of amplifier types, it is necessary to define what efficiency is. Efficiency (η) is defined as the ratio of the RF Power output to the DC power supplied by the system.

$$\eta = \frac{P_o}{P_{DC}} \tag{2.1}$$

Power added efficiency is more commonly used and includes the RF drive power in the equation in order to relay a more precise definition.

$$PAE = \frac{P_o - P_{IN}}{P_{DC}} \tag{2.2}$$

In order to maximize efficiency the portion of the RF cycle that an amplifier spends in its active region is controlled and is referred to as the conduction angle and denoted by $2\theta_C$[2]. Following this criteria the current source amplifiers are broadly classified as:

- Class A amplifiers in the active region during the entire RF cycle. $2\theta_C$=360°.
- Class B amplifiers operate in the active region for ½ the cycle or $2\theta_C$ =180°.
- Class AB amplifiers operate in the active region 180° < $2\theta_C$<360°.
- Class C amplifiers operate in the active region $2\theta_C$ <180°.

2.2 Class A Amplifiers

Class A operation is characterized by a 360 degree conduction angle and the amplifier must be operated such that it stays in its active region during the full 360 degree swing of the input drive. This is accomplished by setting the quiescent point I_{DC} to operate in the center of the load line as depicted in Figure 2.1.

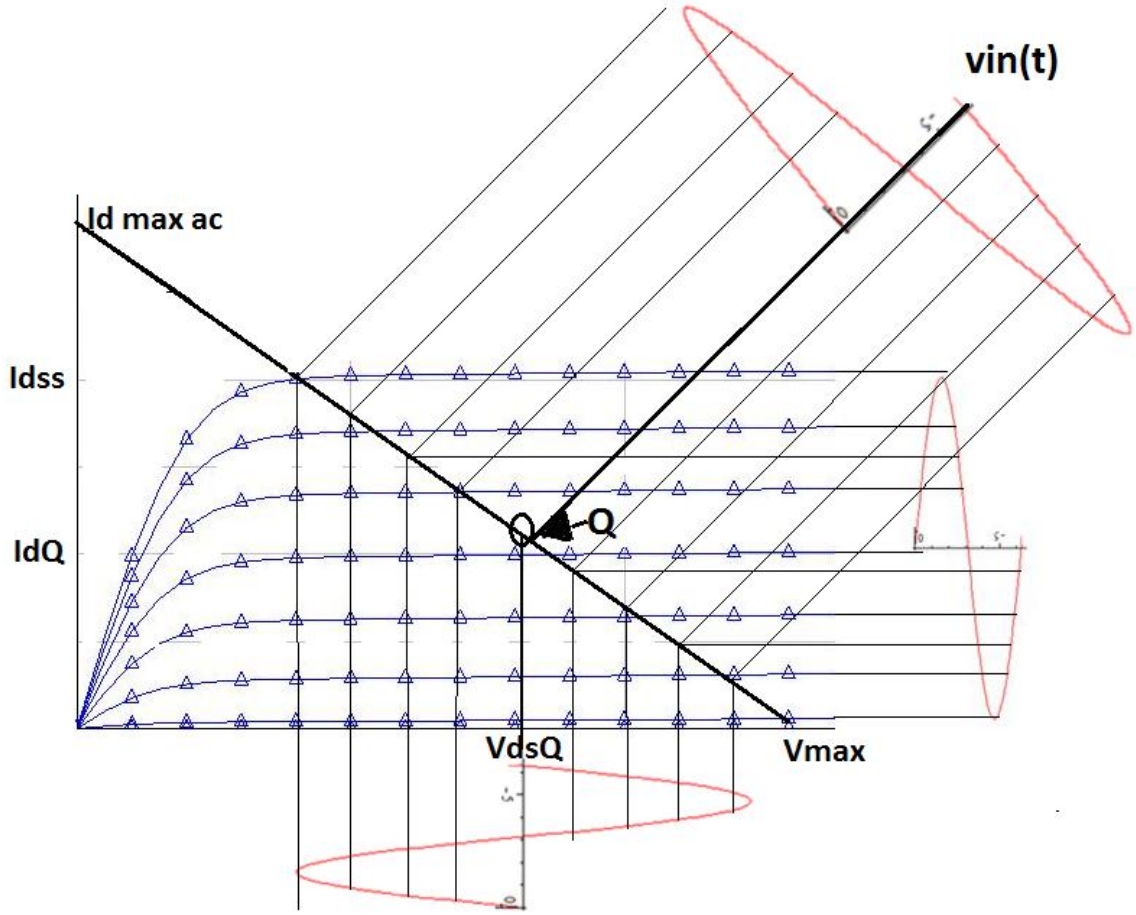

Figure 2-1: Class A Load Line

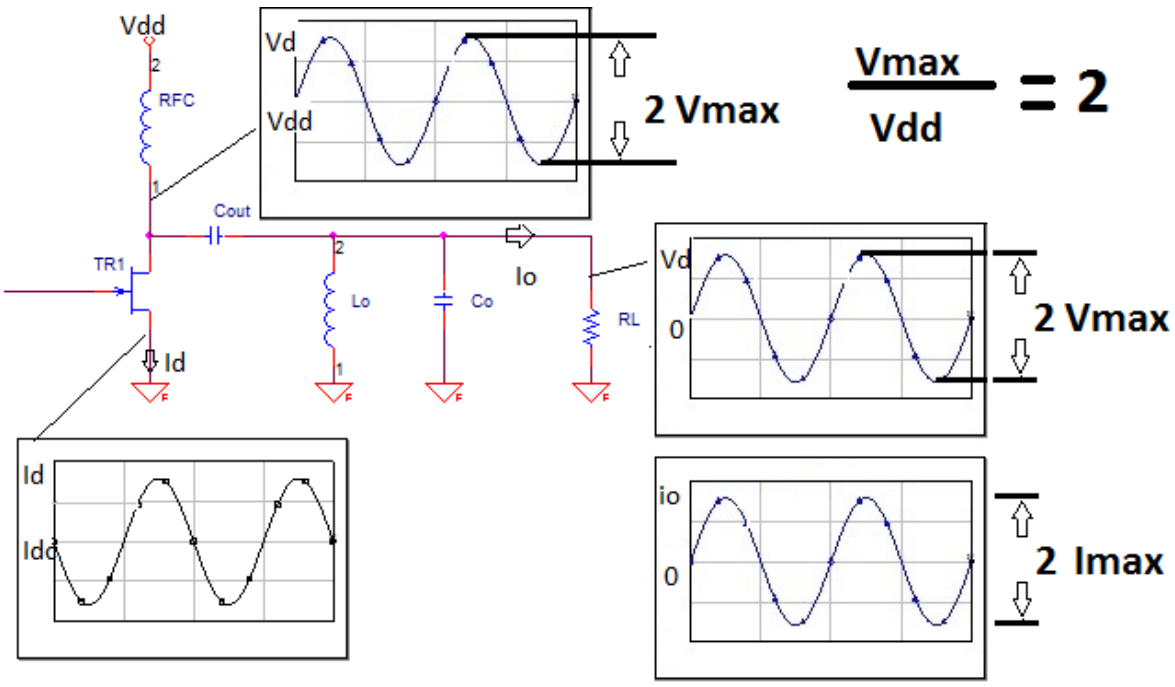

Figure 2-2: Simplified Class A schematic

In the simplified schematic it is assumed that the components are ideal. The active device, TR1, behaves as an ideal controlled current source and the device is perfectly linear such that a sinusoidal gate drive produces a sinusoidal drain current. The radio frequency choke labeled RFC has no resistance and offers infinite impedance to the RF frequency while passing the average DC bias drain current that is set by the gate bias circuit. C_{out} acts as a DC block and presents a short to the RF operating frequency.

Under these conditions the drain current and voltage are given by

$$i_D(\emptyset) = I_{DC} - I_D \sin \emptyset \tag{2.3}$$

$$v_d(\emptyset) = V_{dd} + V_O \sin \emptyset \tag{2.4}$$

Where $\emptyset = wt = 2\pi ft$

The power from the supply is equal to

$$P_S = \frac{{V_{dd}}^2}{R_L} \tag{2.5}$$

The maximum theoretical value for the Power output is

$$P_{L,max} = \frac{1}{2}\frac{{V_{dd}}^2}{R_L} \tag{2.6}$$

The theoretical best value for efficiency is 50% and is given by

$$\eta = \frac{P_o}{P_{DC}} = \frac{1}{2}\frac{{V_0}^2}{{V_{dd}}^2} \leq \eta_{max} = \frac{1}{2} \tag{2.7}$$

Class A amplifiers suffer from low efficiency and under conditions of no input drive the power dissipated in the amplifier is completely absorbed by the active device. This is not the case in Class B or C amplifiers. These amplifiers do not dissipate any power under no drive conditions.

Class A amplifiers have the advantage that they present a linear transfer characteristic and high power gains even at microwave frequencies with gains of 20 to 30dB. But due to the low efficiency values, the class A amplifier is usually limited to low level drivers for more efficient Power Amplifiers [2]. In this manner the fact that the efficiency is low for a stage that is consuming a small amount of the total power budget is insignificant and does not have an appreciable effect on the total system efficiency. These amplifiers are also widely used in laboratory grade equipment where very low distortion and highly linear operation is desired and the efficiency and power consumption needed to obtain it are not overriding concerns.

2.3 Class B Amplifiers

The quiescent voltage and current of the class B amplifier is approximately zero [1]. This offers a nice efficiency advantage over class A as ideally no power is consumed under no drive conditions and operation occurs during sinusoidal excitation of the driving signal over one-half of the cycle.

The circuit architecture is shown in Figure 2-3. This arrangement makes use of a push-pull arrangement so-called because the two transistors, TR1 and TR2 operating in Class B, are driven 180° out of phase with one another due to transformer TX1. During the positive cycle of the input drive one transistor will be biased on while the other is biased off. During the next half cycle the condition will be reversed. This arrangement ensures that only one transistor at a time is conducting and dissipating power while the other is off.

When the transistor is biased on it is ideally considered to be operating in its active region and behaving as a perfectly linear current source. The outputs from both devices flow through the output transformer recombining so that the sinusoid is reconstructed. Most class B circuits involve this type of approach. To operate in a single ended manner would create significant distortion.

Class B amplifiers are often favored in audio power amplifiers, but in this application a totem pole arrangement utilizing complementary transistors is typically used to avoid the use of the transformer. This is not possible at high frequencies due to the poor availability of PNP or complementary devices so the transformer method is often used [1]. The complementary class B amplifiers are utilized up through the HF bands [1].

In comparison to the Class A amplifier, the Class B has the same RF output power but the gain is reduced 6dB. For class B, input voltage is double that of Class A, requiring 6dB more power to get the same RF power with 6dB less gain. [3]. For this reason class AB is generally used with less gain reduction while maintaining good efficiency.

The optimum efficiency of the class B amplifier in idealized circuit conditions is

$$\eta = \frac{P_o}{P_{DC}} = \frac{\pi}{4} = 78.5\% \tag{2.8}$$

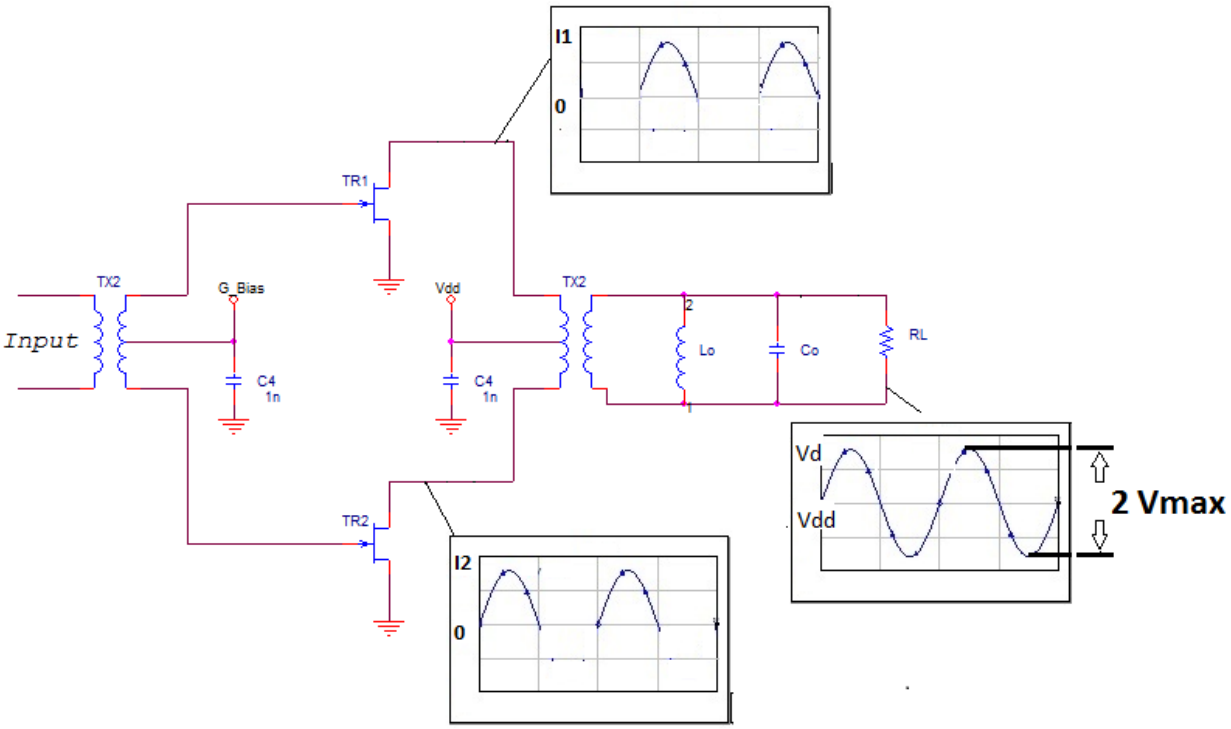

Figure 2-3: Class B Amplifier Schematic

2.4 Class AB Amplifiers

As you might expect from the name, Class AB is a compromise between Class A mode of operation and Class B mode. The output is zero for part of the input sinusoid but less than one-half of the sinusoid. This gives rise to some distortion, the level of which can be improved upon through the level of standing bias applied and the amount of inefficiency that can be tolerated for the application [1]. Additionally class AB can be used in a push pull configuration to obtain better efficiency.

Since Class A operates at a conduction angle of 360° and Class B operates at a conduction angle of 180° it stands to reason that Class AB would operate in between this range. Class AB conduction angle is therefore 180° to 360°. Many Power Amplifiers choose this mode of operation in an attempt to reap the benefits of both classes. The circuit configuration is identical to Figure 2-2 with the only difference being the quiescent bias point.

2.5 Class C Amplifiers

Not all applications require linear amplification of the input signal such as that obtained in the class A amplifier. Some applications that do not require linear amplification are CW and FM signals. Class C has the important distinction that it has the highest collector or drain efficiency of all the classical current mode amplifier classes. The major disadvantage is Class C operation produces higher harmonic content at the output and may require additional filtering that will lower the power gain [2].

Class C amplifiers are classified as either *Current-Source or Saturated amplifiers*. In the current source mode the transistor current is zero when the transistor is shut off. In addition the transistor does not saturate during the entire RF cycle. In the Saturated mode the collector or drain current may be zero when the transistor is cut off, a portion of the sine wave when it is active and another portion of the sine wave when it is saturated [2]. For our purposes we will limit our discussion to the classical current source mode.

In the *Current-Source* Class C amplifier the output current is zero for more than one-half of the input sinusoid rendering it unsuitable for linear amplification. This is accomplished by biasing the Class C amplifier slightly negative so the input sinusoid must reach nearly its positive peak value to overcome this bias and cause conduction. The circuit configuration and current waveforms are depicted in Figure 2-4 and the following expressions are derived in [1] [2].

The drain current is dependent on the RF drive exceeding the negative gate bias and in an ideal memoryless system is given by

$$I_D(t) = \begin{cases} I_{DQ} - I_{DD}\sin(wt) & , I_{DQ} - I_{DD}\sin(wt) \geq 0 \\ 0\,, & I_{DQ} - I_{DD}\sin(wt) \leq 0 \end{cases} \tag{2.9}$$

The relationship between the conduction angle and the bias and drain currents is

$$-I_{DQ} = I_{DD}\cos\theta_C \tag{2.10}$$

And finally the efficiency is related to the conduction angle by

$$\eta = \frac{2\theta_C - \sin 2\theta_C}{4(\sin\theta_C - \theta_C\cos\theta_C)} \tag{2.11}$$

The drain current harmonics as a function of conduction angle for the DC and fundamental component are

$$\alpha_{0(\theta_C)} = \frac{\sin(\theta_C) - (\theta_C)\cos(\theta_C)}{\pi(1 - \cos(\theta_C)} \tag{2.12}$$

$$\alpha_{1(\theta_C)} = \frac{\theta_C - \sin(\theta_C)\cos(\theta_C)}{\pi(1 - \cos(\theta_C)} \tag{2.13}$$

These harmonic equations are valid for Class A and AB as well at low frequencies.

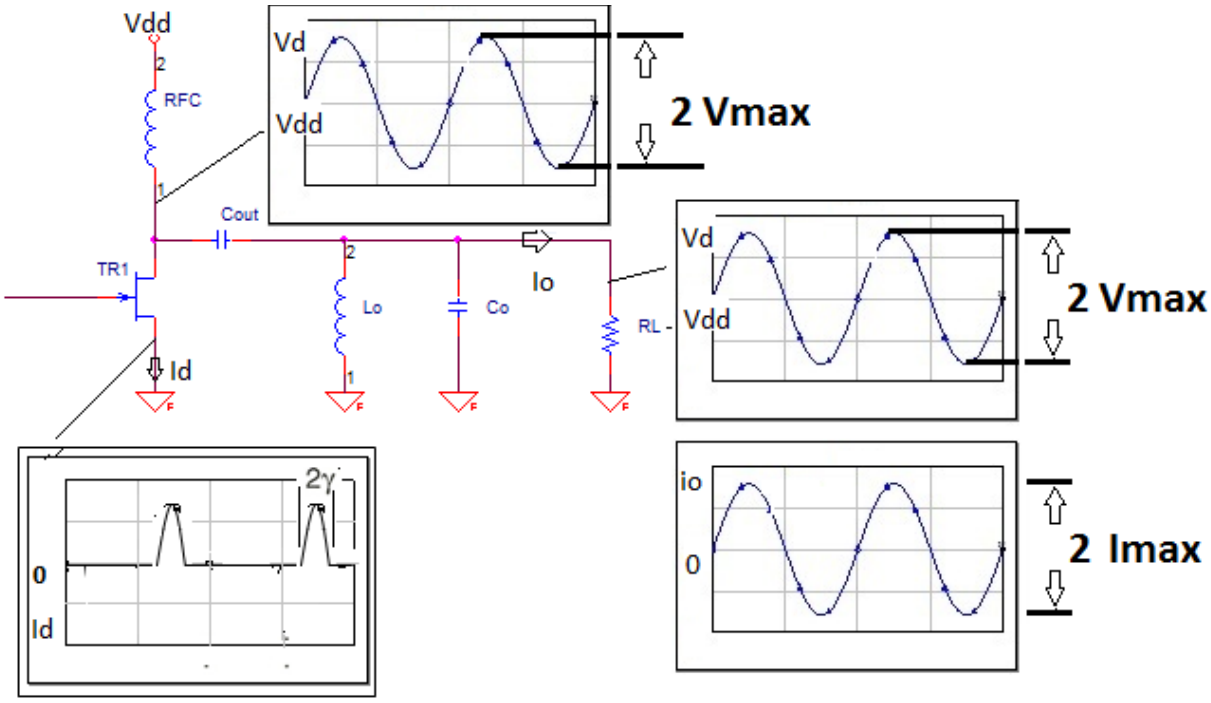

Figure 2-4: Class C Amplifier Schematic

2.6 Theoretical Performance of the classes

Another performance measure of a power amplifier is its power output capability, C_p . This is defined as the output power produced when the device has a peak collector/drain voltage of 1 volt and a peak collector/drain current of 1 amp [2]. Power output capability is defined as

$$C_p = \frac{P_o}{NI_{C,pk}V_{C,pk}} \tag{2.14}$$

If the amplifier contains more than one transistor the additional devices are included in the denominator term. This allows for fair comparison of the various amplifier types whether they are single ended or contain multiple transistors by their ability to deliver power to the load based on circuit configuration. In addition for the designer this helps to evaluate the lowest cost solution for the job at hand whereas the cost of the transistor is usually the most expensive part of the design [2].

A comparison between the theoretical performance of the current mode classes is shown in table 2-1. This table is most useful in distinguishing between the efficiency tradeoffs between the classes and the peak voltage and current present at the active device. It must be kept in mind however that these are theoretical best values and in practice the values listed will be lower.

Class	η_{max}	$\frac{P_O}{{V_{DC}}^2}$	$\frac{V_{max}}{V_{DC}}$	$\frac{I_{max}}{I_{DC}}$	C_p
A	50%	0.5	2	2	0.125
B	78.5%	0.5	2	π	0.125
C	$\frac{\alpha_1(\theta_C)}{2\alpha_0(\theta_C)}$	0.5	2	$\frac{1}{\alpha_0(\theta_C)}$	$\frac{\alpha_1(\theta_C)}{4}$

Table 2-2: Theoretical performance of the amplifier classes

2.7 Nonlinear Phenomena

A perfect amplifier would take an input signal and amplify it linearly so that the output signal would be an exact scalar replica of the input signal. In mathematical terms this would be

$$V_{OUT}(t) = GV_{IN}(t) \tag{2.15}$$

Where G is the voltage gain. Unfortunately amplifiers are not perfect devices and some distortion products occur.

A second order distortion occurs when a distortion term is introduced that is the square of the input voltage. This is also known as the *Square Law characteristic* [1]. The transfer function thus becomes

$$V_{OUT}(t) = G_1 V_{IN}(t) + G_2 {V_{IN}}^2(t) \tag{2.16}$$

Looking at the second order term, G_2, the larger the coefficient is the more curved the transfer characteristic will become thus causing increased distortion [1]. In addition to this it is noticed that a second signal has now appeared in the frequency domain which is twice the input frequency. This term gives rise to what is referred to as *second harmonic distortion.* A DC term also results. Figure 2-5 illustrates this in the frequency domain while figures 2- 6 and 2-7 show the distortion to a sine wave input for a value of $G_1 = 7$ and $G_2 = 3$ in the time domain.

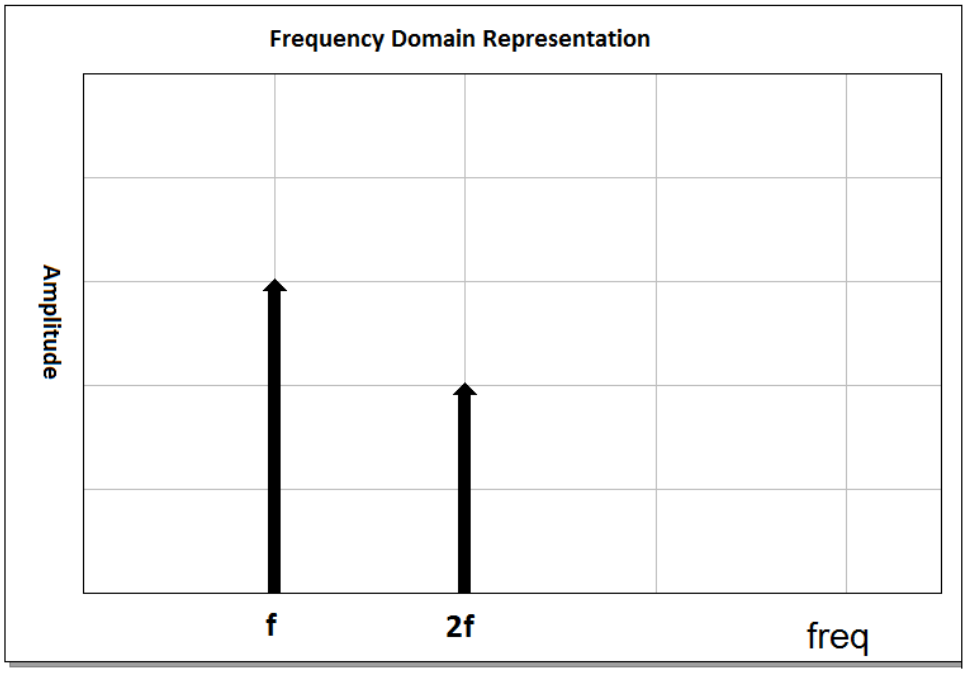

Figure 2-5: Second order distortion in Frequency domain

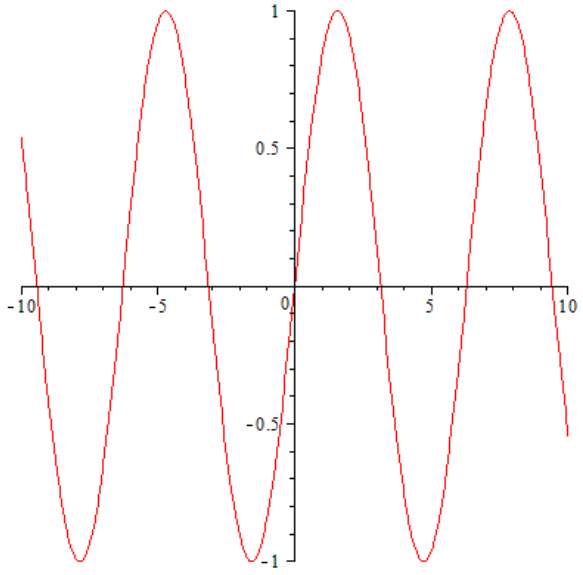

Figure 2-6: Input drive signal

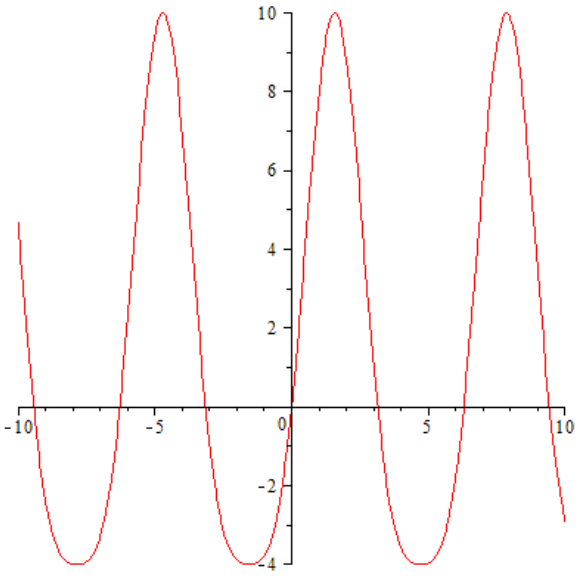

Figure 2-7: Amplifier with second order distortion

An amplifier can also exhibit third order distortion. The appearance of this type of distortion will cause a symmetrical rounding of the sinusoid and a term at three times the input frequency now appears in the output spectrum. One of the common measurements taken and included in amplifier data sheets is the third order intercept point. This is the intersection between the linear gain line extrapolated forward to the third harmonic component extrapolated forward. The higher the third order intercept point the better.

The equation for the third order transfer characteristic is

$$V_{OUT}(t) = G_1 V_{IN}(t) + G_3 {V_{IN}}^3(t) \tag{2.17}$$

The appearance of $V_{OUT}(t)$ is illustrated in Figure 2-8 and the frequency domain representation in Figure 2-9.

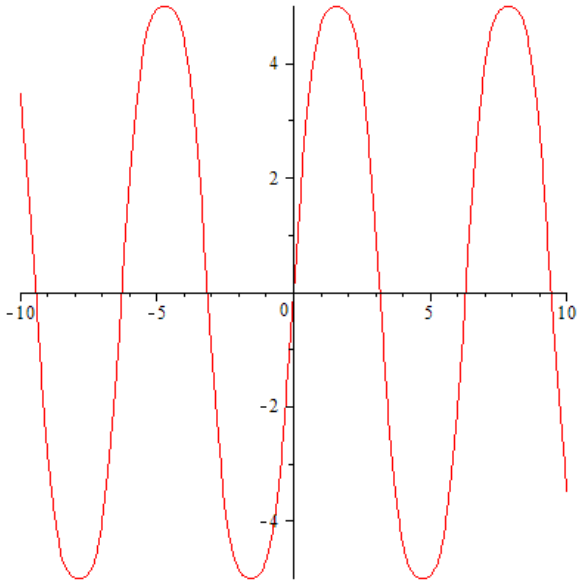

Figure 2-8: Third order harmonic distortion

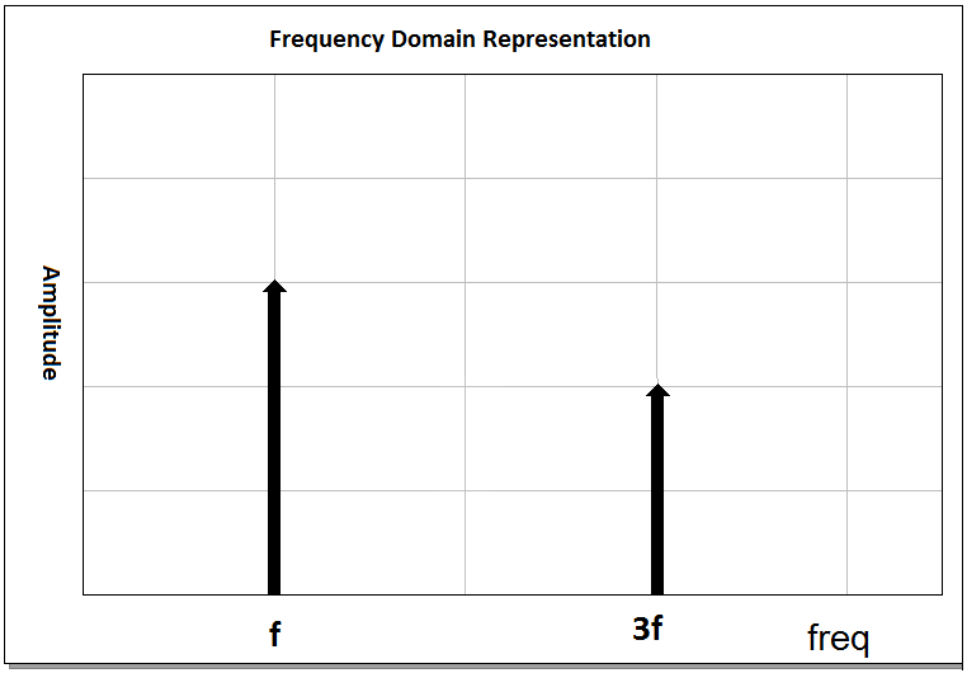

Figure 2-9: Third order harmonic distortion in the Frequency domain

One important distinction between second order and third order nonlinearities is the fact that second order effects produce harmonic distortion but do not produce in-band intermodulation distortion. This is an important distinction, in general even-order nonlinearities do not generate in-band intermodulation distortion [1].

Gain compression is a common third order effect that causes the gain to decrease from the ideal linear response as depicted in Figure 2-10. In the figure the linear gain is represented by the red trace and the blue trace illustrates the compression that is occurring. The amplifier deviates by 1 dB from the linear gain to an output value of 10.13 dBm. It likewise deviates by 3 dB as the input power is increased further such that its output power is 10.76 dBm. This decrease is usually indicated on data sheets as the 1 dB or 3 dB compression point. Often designers will purposely operate an amplifier in compression to obtain higher efficiencies. This is quite common in Class AB amplifiers.

Another type of distortion is known as cross modulation distortion. This is caused when two amplitude modulated carriers are the input drive to the amplifier. The amount of compression experienced by one carrier will depend on the instantaneous amplitude of the other carrier being amplified [1]. It is possible that one carrier can amplitude modulate the other carrier in this process. This can be a serious problem for AM receivers in the presence of strong signals.

Finally one of the most challenging problems to eliminate is intermodulation distortion. This type of distortion appears in the pass-band from frequency products mixing together and usually cannot be filtered out [1]. These products occur at the following locations

$$2f_2 - f_1 \tag{2.18}$$

$$2f_1 - f_2 \tag{2.19}$$

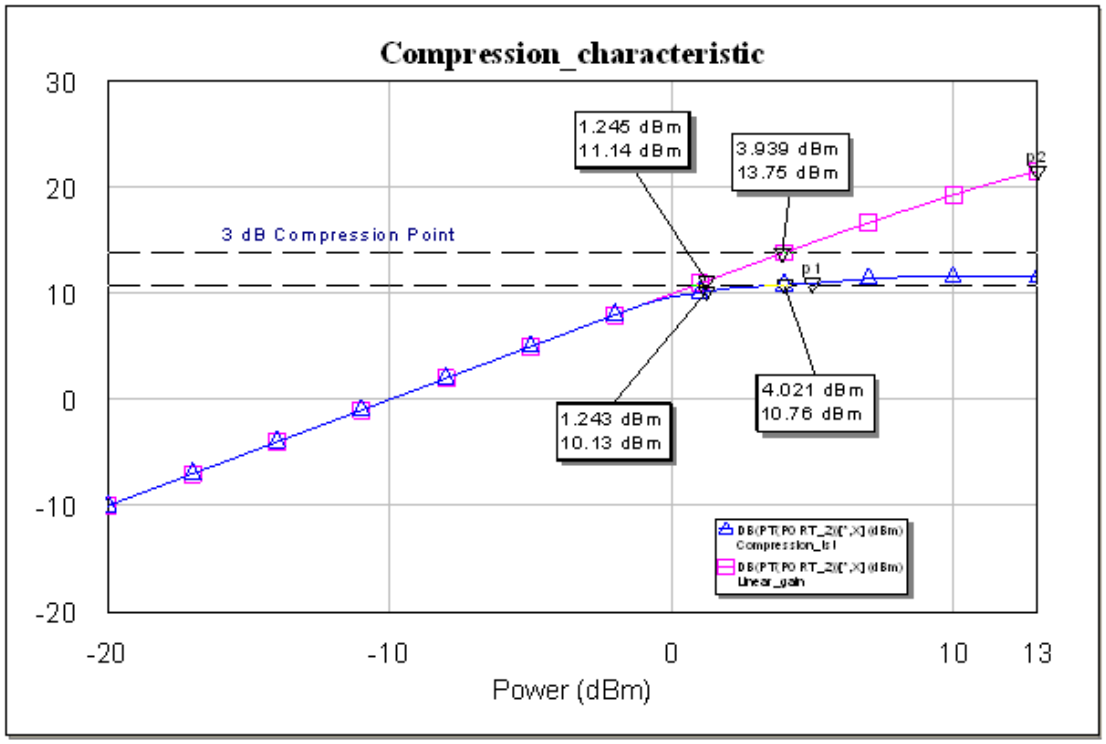

Figure 2-10: 1dB compression point

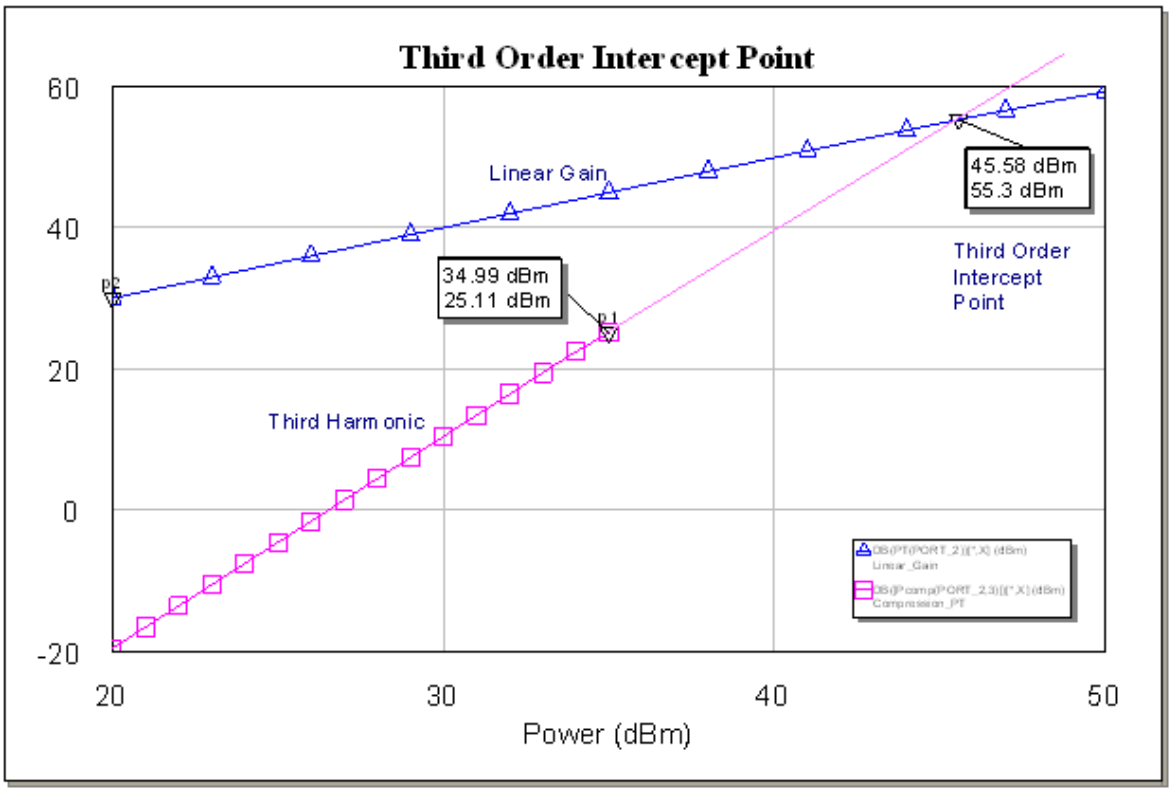

Figure 2-11: Third order intercept point

2.8 High Efficiency Amplifiers

Most high efficiency amplifiers belong to a class of amplifiers known as *Switch Mode.* In this mode of operation the transistor is operated as a switch swinging from cutoff to saturation at RF frequencies. The most common amplifiers of this class are denoted Class D, E, and F but there are many others and variations such as inverse F and class S. Type D, E, and F are commonly used in RF and microwave design. Circuits of type S, have been used for many years in the KHz to MHz range in DC to DC converter applications and recent advances in switching power supply circuits have benefited the RF high efficiency architecture [4].

One of the limiting factors for these architectures is switching speed. At microwave frequencies the active device is not a simple switch and the problem persists that it cannot change states fast enough. It's also imperative that the device parasitic values are properly accounted for and modeled and that its operation in the linear region be included in the circuit simulations. These factors severely limit the usable frequency range of these amplifier classes.

But the benefits to this mode of operation are many. Ideally the active device dissipates no power and all the DC power is converted to RF power for the load. Efficiency is 100% under these conditions. Since the active device is not dissipating any power it does not get hot and does not require any extensive heat sinking. This also relaxes the size that the power supply system needs to be or reduces the capacity requirements of the battery and any external regulators used. This in turn can free up board space or help reduce the footprint of the board even more.

2.9 Class D Amplifiers

The class-D circuit architecture utilizes two active devices that are alternatively switched on and off in a single pole double throw (SPDT) switch arrangement to engage either a rectangular voltage or rectangular current to a tuned circuit that includes the load. For the voltage switching case, the load circuit includes a series LC tuned network but this could also consist of a matching network doing double duty as a matching network and tuned filter. The simplified

circuit and equivalent circuit arrangement is illustrated in Figure 2-12.

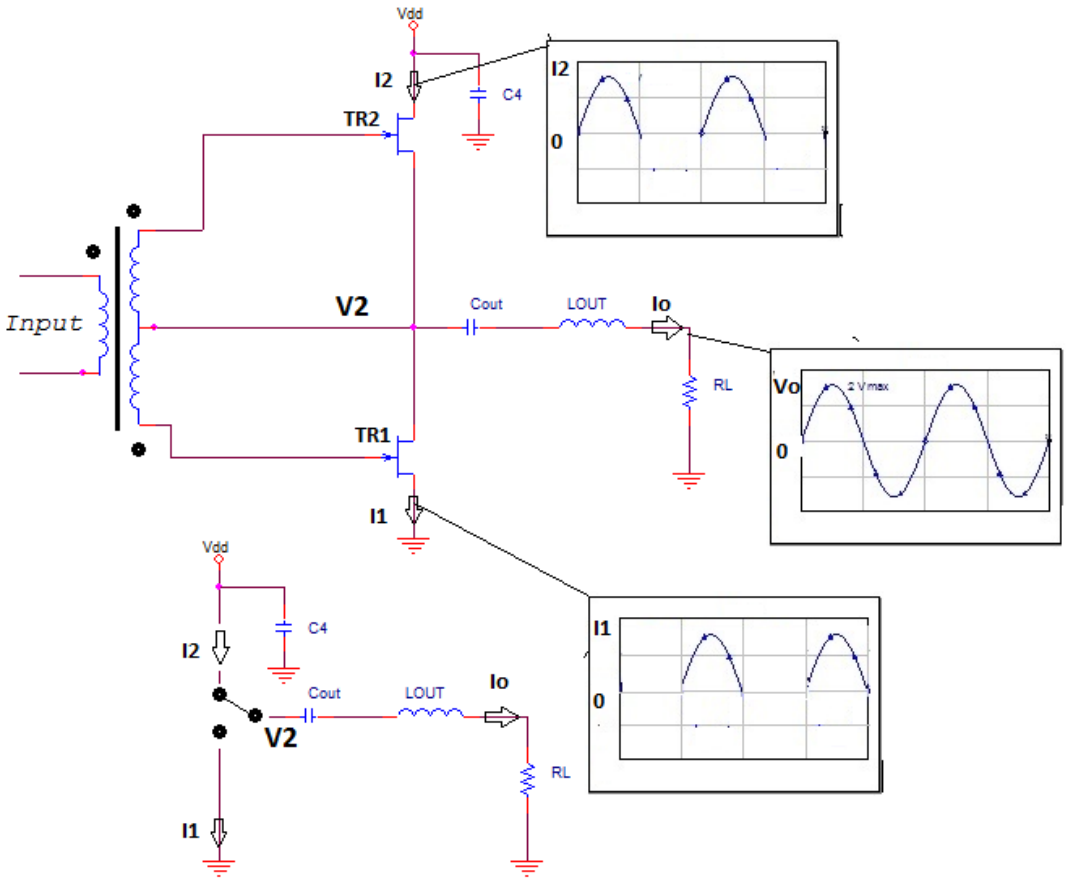

Figure 2-12: Class D Amplifier schematic

As in the Class B circuit the transformer provides gate drive to TR1 & TR2 that is 180° out of phase with one another and this causes the transistors to alternately switch between cut-off and saturation. When the drive is such that TR2 is on then V_{dd} is connected between the source of TR2 and drain of TR1 with TR1 off. During the next half cycle the transistors switch states and the source of TR2 and drain of TR1 are shorted to ground with TR2 off.

The series LC tuned network is designed to be resonant at the switching frequency and must be used to ensure a sinusoidal load current. This is a key issue in this circuit as the LCR branch, with no DC offset due to the blocking capacitor C_{out} is constrained to remain sinusoidal [4].

Assuming the duty cycle is 50% the voltage present at $V_2$is a square wave and is given by

$$V_{2(\theta)} = \begin{cases} V_{dd}, & 0 \leq \theta \leq \pi \\ 0, & \pi \leq \theta \leq 2\pi \end{cases} \tag{2.20}$$

Where $\theta = wt = 2\pi ft$

The output sinusoidal current is given by

$$i_0(\emptyset) = I_{OUT} \sin \emptyset = \frac{2}{\pi} \frac{V_{dd}}{R} \sin(\emptyset) \tag{2.21}$$

2.10 Class E Amplifiers

The class E amplifier is a single ended switch mode amplifier although it is possible to construct push-pull circuit versions rather easily [2]. This high efficiency amplifier was developed in an attempt to ease some of the constraints imposed by the class D amplifier, most notably the sensitivity to frequency and duty cycle variation and to also extend the usable frequency range and operate in a single ended architecture [2].

The amplifier in its simplest form consists of a driver, switch and a load network. As in the Class D configuration the active device performs the function of a switch but in this case the switch is single pole single throw type. Figure 2-13 shows the basic circuit.

The analysis of the circuit proceeds from the following assumptions [2]:

- The RF choke (RFC) is ideal and has no DC resistance but offers infinite impedance to the RF frequency.
- The series resonant tank circuit made up of L_{OUT} and C_{OUT} have a net series reactance jX at the frequency of operation. It is usually not tuned to the frequency of operation.
- The active device is ideal and has zero saturation voltage, zero saturation resistance and infinite off resistance.
- The total shunt capacitance C_p includes the capacitance of the drain or collector and is independent of the voltage.

During the operation of the circuit it is imperative to minimize or eliminate completely the simultaneous condition of voltage across the switch as current is going through the switch. Overlap of voltage and current causes power to be dissipated in the switch and reduces the efficiency of the circuit. It will also cause the active device to heat up which in turn can damage or destroy the device. This condition of zero voltage overlap is known as Zero Voltage Switching, ZVS [2]. As long as the condition is met the class E architecture can theoretically obtain 100% efficiency.

The class E amplifier has both sinusoidal voltage and current waveforms present at the load due to the series LC tank circuit and are given by

$$i_{0UT}(\theta) = \frac{V_O}{R}\sin(\theta + \emptyset) \tag{2.22}$$

$$V_0(\theta) = V_O \sin(wt + \emptyset) = V_O \sin(\theta + \emptyset) \tag{2.23}$$

Where $\theta = wt = 2\pi ft$

And

$$\emptyset = -\tan^{-1}\frac{2}{\pi} = -32.4816° \tag{2.24}$$

The class E configuration has several drawbacks. The flyback like operation of the output circuit raises the peak voltage on the active device to levels as high as $3.65V_{DD}$, often higher than the breakdown voltage of the active device. In addition the series tuned LC network requires inductors with high Q values to obtain high efficiencies. This can be difficult to obtain in semiconductor processes that often have Q values less than 20. Another drawback is the generation of harmonics that may cause the need for added filtering which negates the increases in efficiency gained by operating in this mode in the first place.

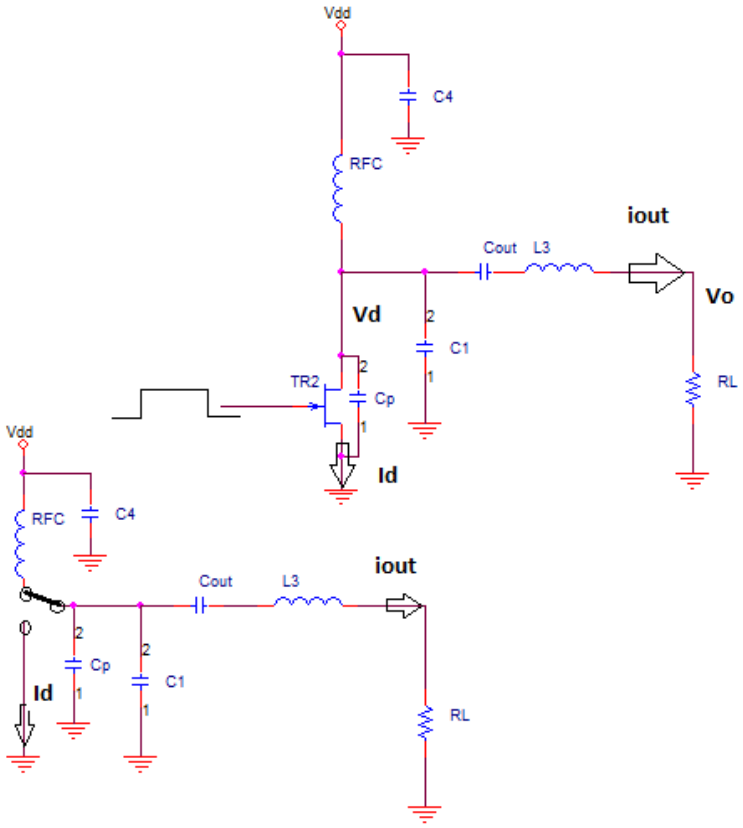

Figure 2-13: Class E Amplifier schematic and simplified switch representation

2.11 Class F Amplifiers

The class F amplifier is characterized by its use of multiple resonators in the output load network. These networks are used to shape the collector or drain voltages and currents to reduce the power dissipated in the active device so as to maximize efficiency.

These types of circuits have also been termed Class C using harmonic injection, optimum efficiency class B, optimally loaded Class B, Class CD, single-ended Class D, multiple-resonator Class C, biharmonic or polyharmonic Class C but recent literature tend to group all high efficiency amplifiers that use multiple resonators in the load network as Class F [2].

The class F circuit contains an output filter that resonates at both the fundamental frequency and at one of the harmonics, usually the second or third. The circuit architecture resembles a Class C amplifier with the addition of a third harmonic parallel resonator L_3C_3 as illustrated in Figure 2-14.

The parallel tuned tank circuit consisting of L_1C_1 resonates at the fundamental frequency and its impedance at this frequency is ideally infinite. The parallel tank circuit consisting of L_3C_3 is tuned to the third harmonic. Because of this the load impedance seen by TR1 is R_L at the fundamental frequency, infinite at the third harmonic and zero otherwise. This shapes the voltage waveform at the drain.

With the presence of the third harmonic in the drain voltage it is possible for efficiencies to exceed that of the Class B or C amplifiers because the fundamental component of the drain voltage can be greater than its peak value [2]. Additionally, the drain voltage is close to zero when the current flows in TR1, helping to achieve near zero IV product. If the third harmonic is 180° out of phase with the fundamental, the drain voltage will be flattened [2].

The drain voltage is given by

$$v_O(\theta) = V_{dd} + V_O \cos\theta - V_3 \cos 3\theta \tag{2.25}$$

Where $\theta = wt = 2\pi ft$

The maximum amplitude of the load voltage, V_0 is equal to

$$V_0 = \frac{9}{8} V_{dd} \tag{2.26}$$

The peak output power is

$$\approx 0.6328 \frac{{V_{dd}}^2}{R} \tag{2.27}$$

And finally the ideal drain efficiency is

$$\eta = \frac{P_o}{P_{DC}} = \frac{9\pi}{32} \approx 88.36\% \tag{2.28}$$

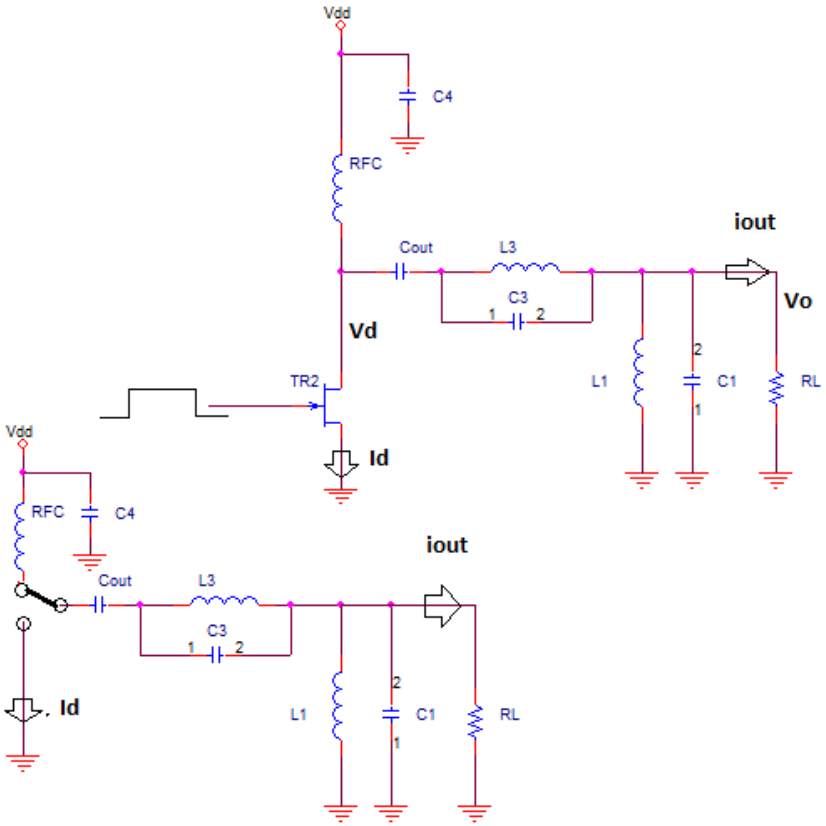

Figure 2-14: Class F amplifier circuit and simplified switch representation

Chapter 3 - **Oscillations in Linear and Nonlinear Systems**

Perhaps the most important requirement in designing a power amplifier is to not design an oscillator. This is the most obvious of statements and certainly will be obvious the moment the circuit is powered up and measurements are made if this unfortunate set of circumstances materializes. Power amplifiers by nature of their design form feedback paths through unintended components or through parasitic components or board layout routings that may cause oscillations to occur.

Oscillations can occur at frequencies that are related to the frequency of operation or may be at harmonics or subharmonics of it. They can have complex current and voltage waveforms that may cause spurious modulations, noise, distortion of the intended signal or signals and possible damage or destruction to the active device.

Some types of oscillations occur only under a specific set of operating conditions such as specific gate or drain bias levels, drive levels, source or load impedances, specific frequencies or under varying temperatures. Often these types of oscillations are referred to as spurious oscillations.

The mechanisms that cause or support these oscillations may coexist in the same circuit simultaneously or may be produced under differing sets of operating conditions which makes the construction of a mathematical model for the oscillation extremely difficult if not impossible. Adding insult to injury the elimination of one form of oscillation can cause a different type to appear.

3.1 Feedback Instability

Excessive positive feedback sources are detrimental to the stability of an amplifier and may cause it to oscillate. These sources can come from areas such as lead inductances or transistor parasitic elements such as C_{DG} . Capacitive and magnetic coupling between input and output circuits can also disrupt stability, and in RFIC circuits planar inductors in close proximity to one another can as well.

To analyze these effects it is necessary to create a circuit model that includes the effects of the parasitic resistances, capacitances and inductances of not only the circuit being designed but also of the layout that it will be integrated into. It is of course very difficult and time consuming to design a model to encompass all of these effects, especially if couplings between inductors are included that would then necessitate the use of EM (Electromagnetic) simulators.

An additional limitation is performing this analysis by linear methods. An RF power amplifier is always a nonlinear system [2]. Depending on the class of operation the degree of nonlinearity can vary substantially. A class E switch mode amplifier operates in a highly nonlinear mode whereas a class A amplifier may operate linearly under most drive conditions but will exhibit nonlinear effects at high signal levels. In addition to this, transistor models are derived from extracted parasitic values taken under linear operating conditions and these same values can vary significantly at cutoff and saturation loadline extremes.

Oscillations due to feedback can exist with or without RF drive applied or may start or stop the moment the RF drive is applied. It may stop when the drive is interrupted or it may continue. An oscillation may be present over a range of gate and drain bias levels and be at virtually any frequency or amplitude value from very small to very large. In some cases the signal is added to the frequency of interest. The behavior is governed by the active device used and it is the transistors changing characteristics through voltage and current excursions that set this behavior [2].

3.2 Power Supply Decoupling

It is essential to employ good DC power supply decoupling techniques to eliminate feedback paths from traveling along the DC supply buses from adjacent stages, especially higher power stages leaking back in to lower power ones. In order to be effective decoupling it must be broadband and cover from very low to very high frequencies. This is necessary because bias supplies can contain a broad range of frequency components from all of the circuits it is supplying. Ceramic chip capacitors with the smallest footprint practical for the design are the best choice. Inductors should offer as large an impedance to the RF frequency as possible with low DC resistance.

It is also imperative to control ground return lengths and place the bypass components as close to the amplifier as physically possible. Capacitor ground pads should have several vias placed directly in the pad so as to eliminate any added inductance from traces returning to gnd. Inductors should be placed perpendicular to each other so as to avoid coupling and magnetically shielded types used where possible. Ground returns should be on planes and in the case of multilayered MCMs (Multi Chip Modules) there should be separate ground planes for analog, digital and rf grounds.

Modeling the de-coupling circuits in the same manner as the circuit being designed is good practice to help identify and eliminate potential sources of instability caused by power supply coupling. In cases where the manufacturers model is difficult to obtain an alternate approach is to measure S-parameters on a test substrate and build up a library of files for future use.

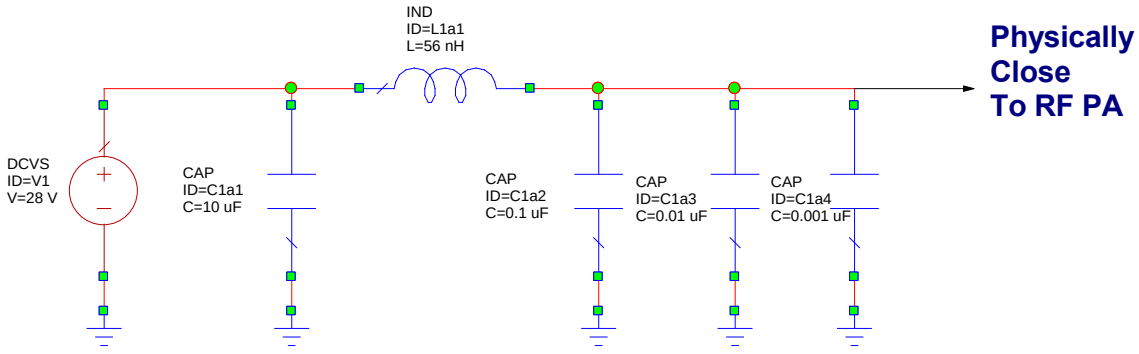

Figure 3-1: Power supply decoupling broadband example

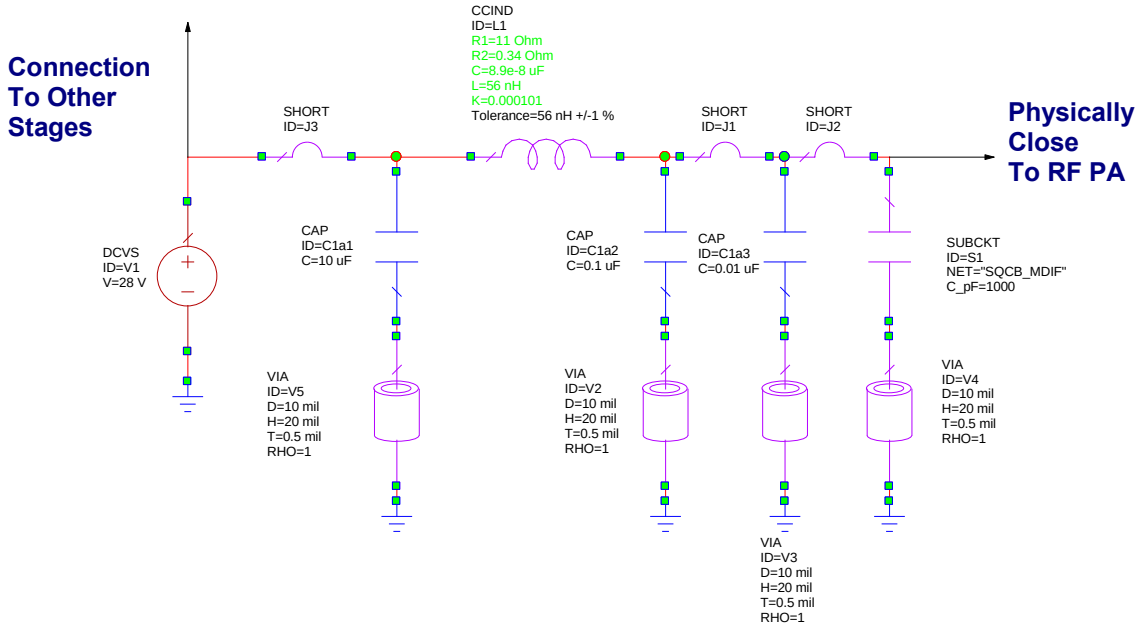

Figure 3-2: Power supply decoupling broadband example modeled

3.3 Bias Network Instability

Transistor bias networks are another potential cause of circuit instabilities. In addition to following the techniques previously described for power supply decoupling, gate bias networks also require additional effort to eliminate nonlinear positive feedback paths. Experience has shown the existence of a nonlinear oscillation mechanism that is dependent on the impedance seen by the drain [2]. The impedance presented to the drain circuit coupled with the parasitic capacitance present from drain to gate can create a positive feedback.

A positive feedback path from the drain to the gate of the transistor may change the gate bias and thus the drain current. This form of oscillation appears lower in frequency than the intended frequency of operation [2]. One way to eliminate this type of oscillation is to insert a small series resistance in the gate circuit. This value should be less than 10 ohms and will degrade gain and efficiency to a degree but the benefits can be worth the small loss incurred.

3.4 Parametric Oscillation

Oscillations can be generated by periodically varying circuit parameters of reactive devices such as inductors and capacitors, this is known as the theory of circuits with variable parameters [2]. The capacitance of RF power transistors vary considerably as the voltage across the devices change from RF cycle excursions or from mode of operation due to amplifier class. The most significant change occurs near zero volts thus having more effect on the switch mode amplifiers and the class C type.

A parametric oscillation usually occurs at a subharmonic of the operating frequency, f/k , where k is an integer, usually $k = 2$ or $k = 3$ but it is not a requirement that the oscillation frequency be an integer submultiple of f [2].

One way to mitigate these effects is to add some capacitance in parallel with the transistor drain to help “swamp out” the effects of the active devices inherit nonlinear capacitance.

3.5 Thermal Feedback Instability

Depending on the class of operation, RF power transistors can dissipate an appreciable amount of heat. The temperature at which the semiconductor junction operates is dependent on the dissipated power and how well the thermal resistances of the transistor, heatsink, and various mechanical interfaces are able to transfer this heat out of the transistor. It is important to control the junction temperature variation to acceptable limits as the transistor characteristics change considerably from heating effects.

When operating temperature is not controlled within acceptable bounds a thermal feedback loop can develop that can in consequence change the voltage across the device or the current through it thus changing its electrical characteristics and possible causing oscillations to occur.

Chapter 4 - **Linear Stability Analysis**

Stability analysis of amplifiers is perhaps the most important step in the design process and one that should be given considerable attention. In designing a particular amplifier there are many important parameters that the designer must take into account. These include the following:

- Band of operation
- Linearity required
- Output power required
- Available power supplies
- Efficiency requirements
- Gain required
- Heat sinking available
- Transistor technology to use

Once the design parameters have been adequately specified the designer sets to work on a design that will accomplish the task. He or she selects an amplifier class that is appropriate for the signal type and designs to the specifications. But the job is not complete until a thorough analysis is made as to the stability of the amplifier.

The widely accepted method to check stability of a complicated N-node network operating in its linear region is by examining its S-parameters obtained by reducing the complicated network to a two port network between input and output and requiring that $K > 1$ and $|\Delta_s| < 1$ at all frequencies [5].

These stability conditions are

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_S|^2}{2|S_{12}||S_{21}|} > 1 \tag{4.1}$$

Along with the fulfillment of any one of the following expressions

$$|\Delta_S| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{4.2}$$

Or the following

$$1 - |S_{II}|^2 > |S_{12}S_{22}| \; for \; I = 1 \; or \; 2 \tag{4.3}$$

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta_S|^2 > 0 \tag{4.4}$$

$$B2 = 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta_S|^2 > 0 \tag{4.5}$$

A related stability measure is the geometric stability factor. This measure computes the distance from the center of the Smith Chart to the nearest unstable point. $Mu1$ computes this point in the output load plane and $Mu2$ computes in the input source plane.

$$Mu1 = \frac{1 - |S_{II}|^2}{|S_{22} - \Delta_S S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{4.6}$$

$$Mu2 = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta_S S_{22}^*| + |S_{21}S_{12}|} > 1 \tag{4.7}$$

These conditions can also be derived in terms of port parameters.

$$K = \frac{2Re\{\gamma_{11}\}Re\{\gamma_{22}\} - Re\{\gamma_{12}\gamma_{21}\}}{|\gamma_{12}\gamma_{21}|} > 1 \qquad (4.8)$$

Where γ can be Y,Z or H parameters.

All of these equations are in the commercially available software packages such as Agilent Design System (ADS), Ansoft Designer, Eagleware, Microwave Office and many others. They are all mathematically equivalent and have as their underlying requirement the condition that under steady state, small signal, analysis a passive load presented at one port does not cause a negative real part to be presented to a source at the other port [5].

The conditions require that $K > 1 \; and \; G_{11} > 0$ are necessary to ensure that the real part presented to a source is positive irrespective of the load. That this will guarantee stability does **not** always hold true [5]. Conditions can occur whereby $K > 1$ exists and the circuit is unstable and $G_{11} < 0$ and the circuit is stable [5]. In this chapter, we investigate this problem by analyzing four cases comparing the K/B1 results to that obtained by analytical methods, transient analysis and the Normalized Determinant method. In two of the four examples, the K/B1 analysis incorrectly indicates the stability of the circuit. We will begin by reviewing Pole Zero analysis and the conditions for stability and then describe a new method known as *Normalized Determinant function.* Finally these tools will be used to analyze the four examples.

4.1 Pole Zero Analysis

The transfer function for a system is a means for determining the system response characteristics without having to solve complex differential equations. The transfer function is a rational function in the complex variable $s = \sigma + j\omega$. The general form of the transfer function is

$$H(s) = \frac{b_m s^m + b_{m-1} s^{m-1} + \ldots + b_1 s + b_0}{a_m s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + a_0} \tag{4.9}$$

It is often advantageous to write the transfer function in factored terms

$$H(s) = \frac{N(s)}{D(s)} = K \frac{(s - z_1)(s - z_2) \ldots (s - z_{m-1})(s - z_m)}{(s - p_1)(s - p_2) \ldots (s - p_{n-1})(s - z_n)} \tag{4.10}$$

The numerator function contains the roots or zeroes of the function which and are found by

$$N(s) = 0 \tag{4.11}$$

The denominator function contains the poles which are found by

$$D(s) = 0 \tag{4.12}$$

The poles of $H(s)$ are the characteristic roots of the system and from analyzing the roots the stability of the system can be determined. The conditions for stability for LTIC systems (Linear Time Invariant Continuous time) are the following:

1. A system is asymptotically stable if and only if all the poles of its transfer function $H(s)$ are in the LHP (Left Half Plane). The poles may be repeated or unrepeated [11].
2. A system is unstable if and only if one or both of the following conditions exist (i) at least one pole of $H(s)$ is in the RHP (Right Half Plane); (ii) there are repeated poles of $H(s)$ on the imaginary axis [11].
3. A system is marginally stable if and only if there are no poles of $H(s)$ is in the RHP (Right Half Plane), and there are some unrepeated poles on the imaginary axis [11].

The pole zero analysis is the most thorough and complete way to determine circuit stability and is the final word when stability is in question. Pole zero analysis has the disadvantage that it can be slow and require considerable computing resources when using it to analyze circuits with hundreds or more nodes because of the large matrices involved.

4.2 Normalized Determinant Function

The normalized determinant function is a frequency domain method developed to determine the number of zeroes in the circuit determinant that have positive real roots without building the large matrices required from pole zero analysis. The transient response is determined by the roots of the system. When taking the determinant the roots are the zeroes of the function [5].

NDF is based on the Principle of the Argument theorem of complex theory which states the following: The total change of the argument (phase) of a function $F(s)$ along a closed contour C on which the function has no zeroes and inside which it is analytic except for poles, is equal to

$$\emptyset_D = 2\pi(N_z - N_p) \tag{4.13}$$

Where N_z is the number of zeroes and N_p is the number of poles function $F(s)$ inside C [5].

The NDF is defined as the following

$$NDF = \frac{\Delta(s)}{\Delta_0(s)} \tag{4.14}$$

The determinant, $\Delta(s)$, is the determinant of the circuit being analyzed whereas the companion determinant, $\Delta_0(s)$, is the determinant of the circuit with all of the dependent active generators being set to zero [5].

Normalizing the circuit determinant to $\Delta_0(s)$ allows for the following properties:

1. The denominators of $\Delta(s)$ and $\Delta_0(s)$ are equal and cancel out [5].
2. The NDF has no poles in the RHP, this is due to the fact that the companion determinant $\Delta_0(s)$ has no dependent active generators and is therefore passive and none of its zeroes lie in the RHP [5].
3. The value of the NDF function approaches 1 as ω approaches ∞ or as σ approaches ∞. This is because both determinants are of the same order of s [5].
4. The system response is a real function of time thus $NDF(-\omega) = NDF^*(\omega)$ [5].

The NDF reduces to

$$NDF = \frac{\Delta(j\omega)}{\Delta_0(j\omega)} \tag{4.15}$$

along the imaginary axis.

The system is unstable if, on a polar plot, the NDF encircles the origin clockwise as this indicates that there are zeroes in the determinant. If there is an encirclement of the origin on the polar plot more analysis is needed to determine the exact frequency. The frequency of abrupt phase transitions of 180° or more seem to come reasonable close to the pole zero analysis results.

A drawback to the NDF approach is that the software used must be able to control the dependent sources of the $\Delta_0(s)$determinant. This can be an issue for active S-parameter files, compiled linear models and some foundry design kits that do not allow access to controlled sources.

4.3 Nyquist Stability Analysis

Nyquist stability analysis operates in a similar fashion to the NDF analysis discussed in section 4.2, in that it makes use of the principle of argument theorem developed by Cauchy. Nyquist applied this theorem to the open loop system transfer function to obtain stability information on the closed loop system transfer function. In addition to stability information a key result of this analysis is that it can be used to determine the relative degree of system stability by generating phase and gain stability margins.

The analysis is based on Cauchy's principle of argument theorem which states the following: Let $F(s)$ be an analytic function in a closed region of the complex plane s except at a finite number of points that are the poles of $F(s)$ [10]. $F(s)$ is also analytic at every point on the contour [10]. Then as s traverses the s plane contour in the clockwise direction the function $F(s)$ encircles the origin in the $Re\{F(s)\}, Im\{F(s)\}$ plane in the same direction N times with N given as

$$N = Z - P \tag{4.16}$$

where Z and P represent the number of zeroes and poles of the function $F(s)$ inside the contour as illustrated in Figure 4-1. The value for Z and P also includes repeated roots.

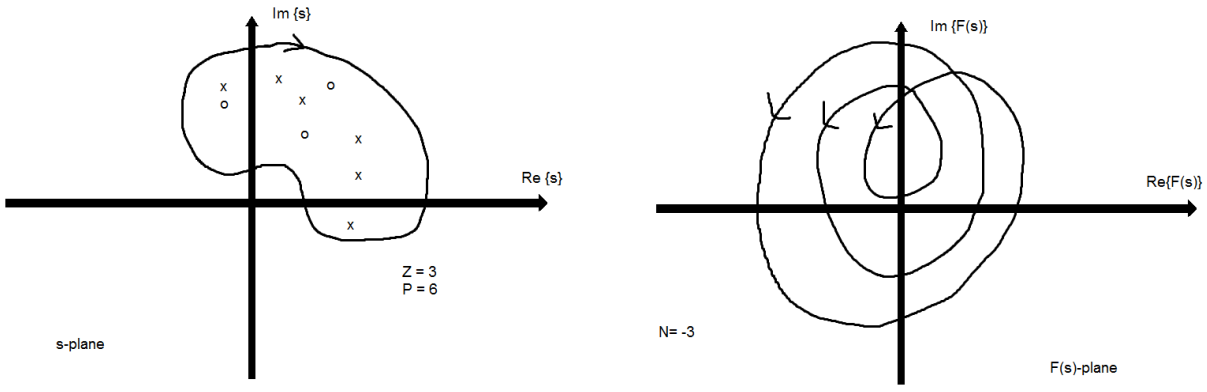

Figure 4-1: Cauchy Principle of Argument Theorem

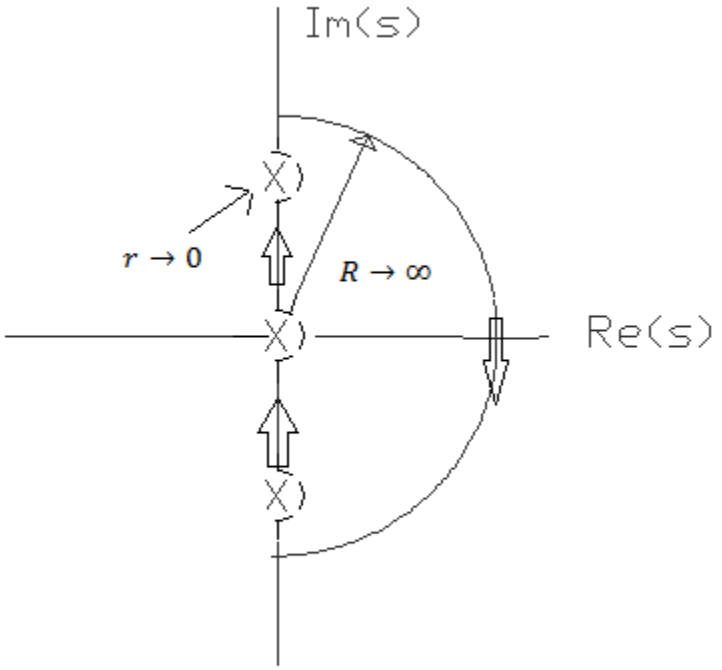

Figure 4-2: s travel contour in clockwise direction

The stability criterion states that the number of unstable closed loop poles is equal to the number of unstable open loop poles plus the number of encirclements of the origin.

The Nyquist criteria allows for an analysis of stability of the point where two networks are connected together by treating the connection node as a feedback point and using methods of control system analysis to determine stability. As illustrated in Figure 4-3 the signal flow graph interface between the two S-parameter blocks, labeled S and S' creates a feedback loop.

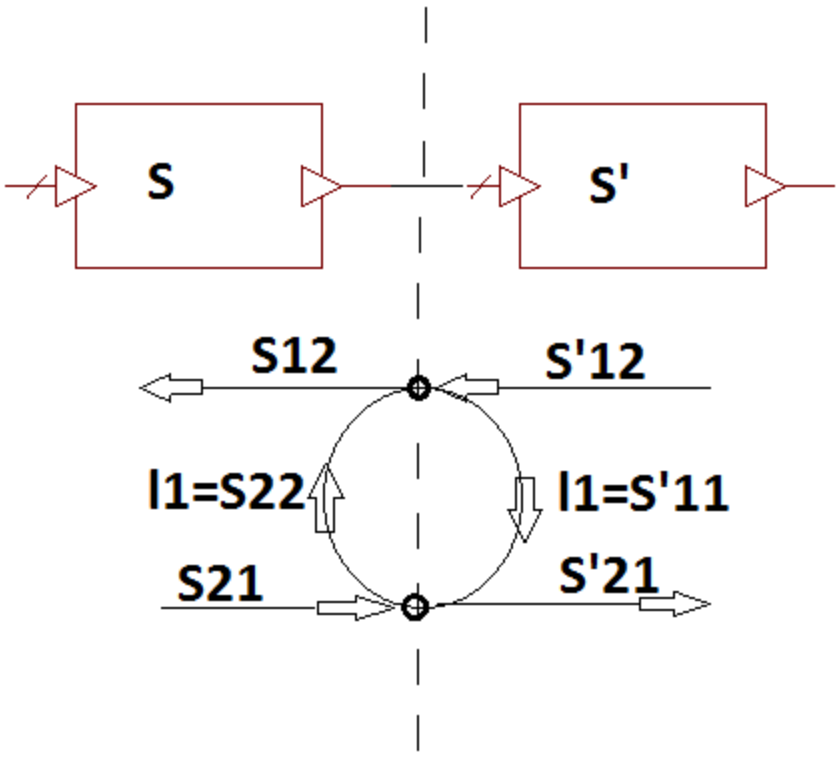

Figure 4-3: Signal Flow graph diagram of interface of two S-parameter blocks

This system can be represented in control system theory as an amplifier with an open loop gain, $G(s)$ and a feedback block $H(s)$ as depicted in Figure 4-4. The transfer function for the system is thus

$$M(s) = \frac{G(s)}{1 + H(s)G(s)} \tag{4.17}$$

with

$$G_N = H(s)G(s) \tag{4.18}$$

The closed loop system poles are found by solving the denominator function

$$1 + H(s)G(s) = 0 \tag{4.19}$$

The system is unstable when the denominator term is equal to zero. This occurs when $G_N = -1$.

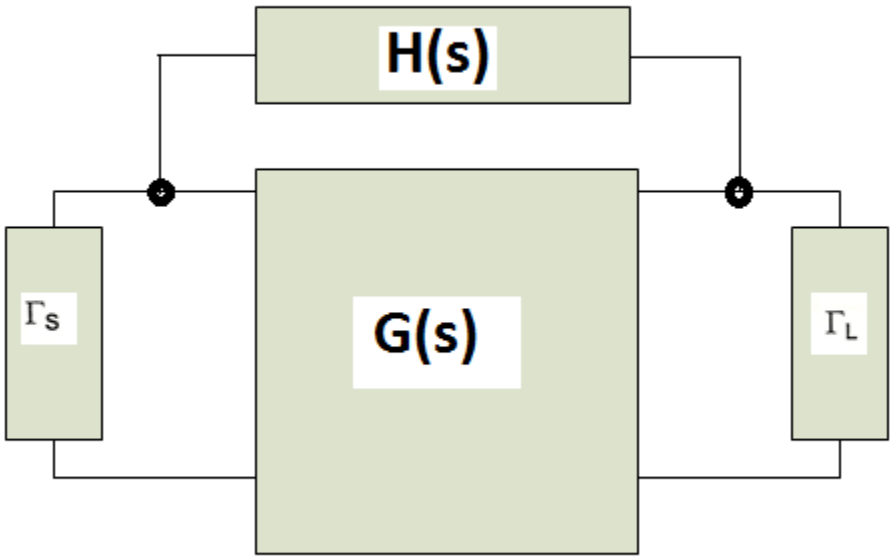

Figure 4-4: Nyquist control system representation

Various simulation tools plot the G_N function differently. Some plot the $-G_N$ and then determine stability by looking to see if the $(-1 + j0)$ plot is encircled, others plot the $1 - G_N$ and then check see if the origin is encircled and still others plot the G_N value and check to see if the $(1 + j0)$ point is encircled so it is imperative that the simulator documentation is checked carefully to determine the method used.

Microwave office uses the gamma probe in conjunction with the Nyquist analysis to determine stability and plots the $-G_N$ function so that the $(-1 + j0)$ point, if encircled in a clockwise

sense, will indicate an unstable system [9]. Figure 4-5 shows the connection of the gamma probe between two transistors represented by linear S-parameter files. The input and output reflection coefficient, Γ, is found by running a frequency swept simulation through the gamma probe. The open loop frequency domain response is given by

$$G = -\Gamma_1\Gamma_2 \tag{4.20}$$

The open loop function G, when plotted on the complex plane will be stable if the -1 point is not encircled in a clockwise sense.

The analysis shows the circuit is stable over the range of frequencies simulated, in this case from 10Mhz to 5 GHz as illustrated in the polar plot of Figure 4-6.

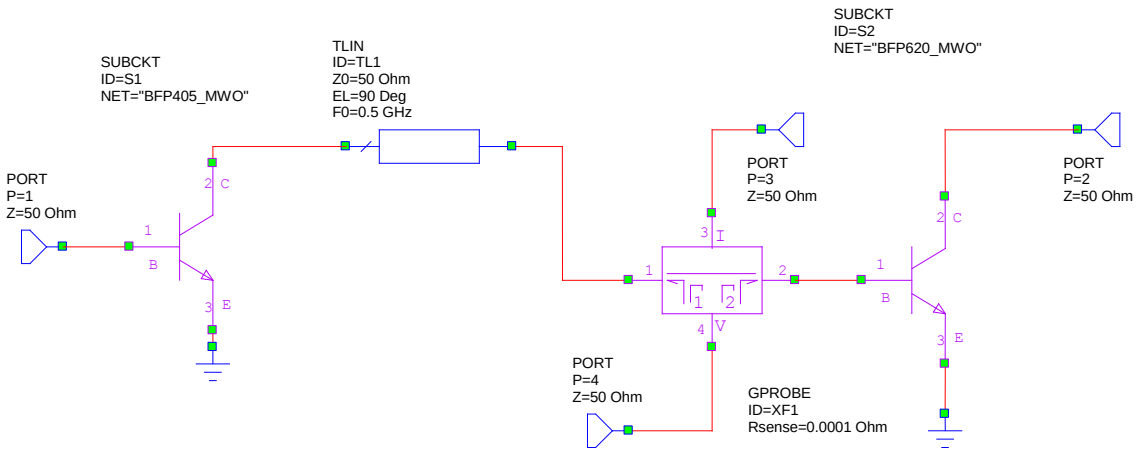

Figure 4-5: Nyquist stability using the gamma probe

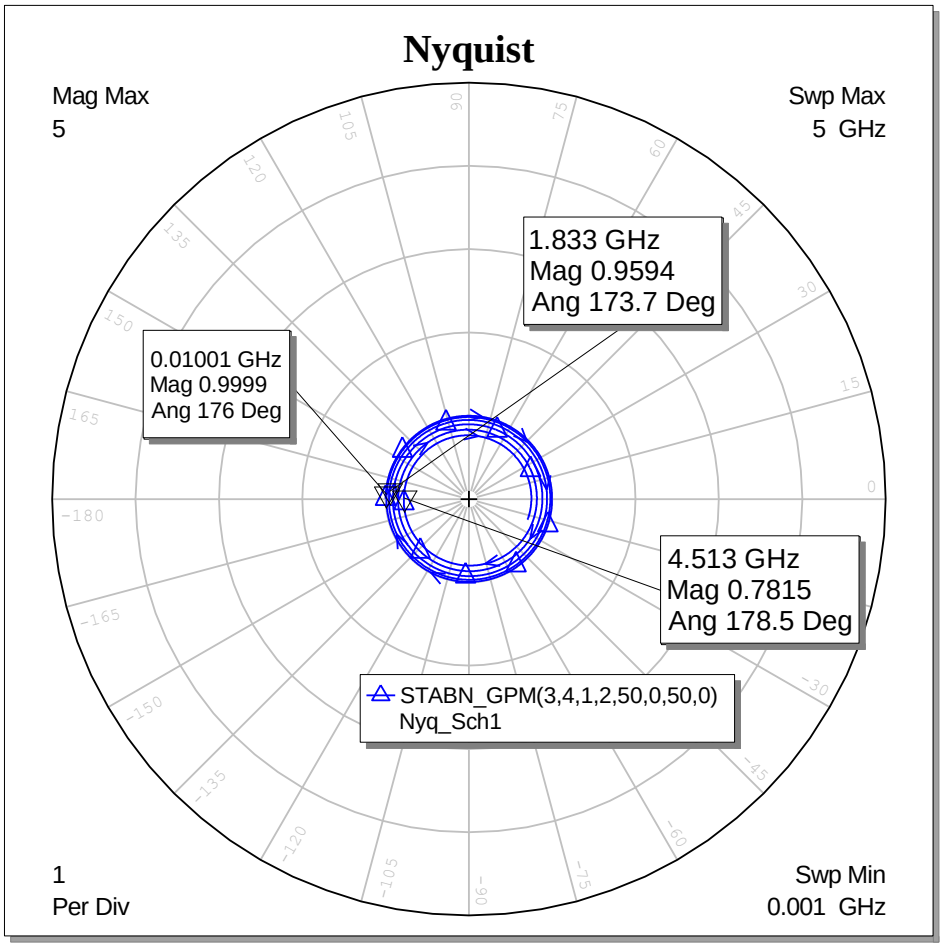

Figure 4-6: Polar plot of Nyquist analysis

The Nyquist analysis also gives an indication of how close to the unstable region a system is by calculating a gain and phase margin with respect to the $(-1 + j0)$ instability point as shown in Figure 4-7.

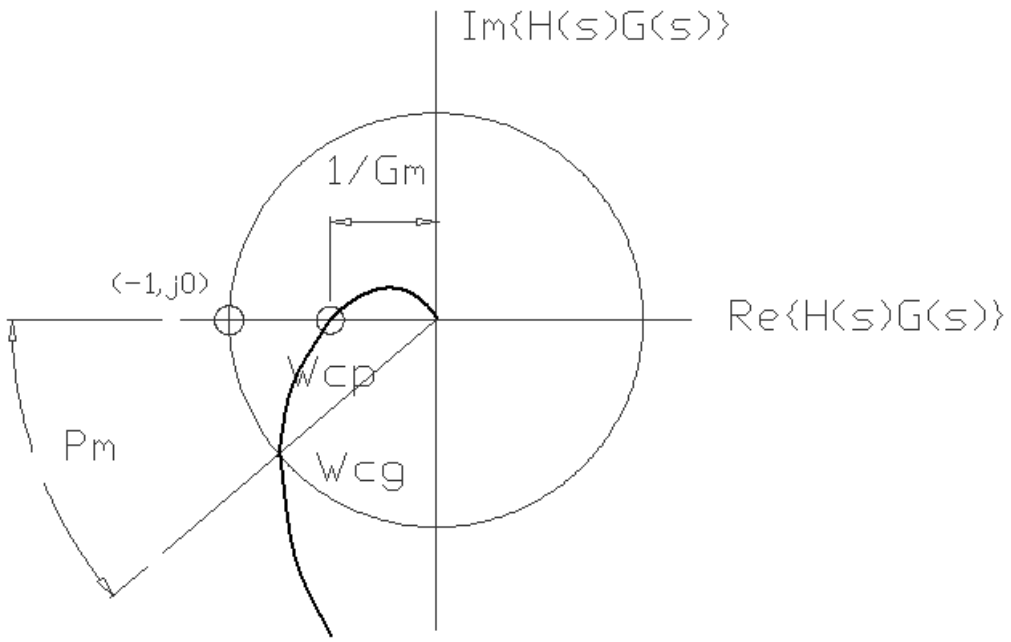

Figure 4-7: Gain and Phase stability margin

The phase margin is defined as

$$P_m = 180 + arg\{G(jw_{cg})H(jw_{cg})\} \tag{4.21}$$

The gain margin in dB is defined as

$$Gm[dB] = 20log\frac{1}{|G(jw_{cg})H(jw_{cg})|} \tag{4.22}$$

4.4 Example 1: K/ B falsely predicting Stability

The examples that follow in section 4.4 thru 4.7 are based on work by Aryeh Platzker and Wayne Struble [5]. This thesis expands upon this work by including the geometric stability measures $Mu1$ and $Mu2$ and the results of transient analysis for all four cases. In addition to this another root is discovered in all four cases not identified in the original analysis.

The circuit shown in Figure 4-8 is that of a ring oscillator. Ring oscillators are devices constructed of an odd number of cascaded inverters with the last device fed back to the first device. The oscillation occurs because the last output of the inverter chain is the logical not of the first inverter. This feedback causes oscillation at a frequency related to the inverse of an integer multiple of inverter delay.

Four cases will be analyzed as shown in Table 4-1. These cases will check for stability using K, $B1$, $m\mu1$, $m\mu2$, NDF and transient analysis under four sets of circuit element values indicated in the table. The remaining circuit values will stay fixed to the schematic values indicated in Figure 4-8.

Case	R_2	Y_s	Y_1
1	50Ω	20mS	20mS
2	5Ω	20mS	20mS
3	5Ω	$150mS \| 500pH$	$100mS \| 1250pH$
4	5Ω	$50mS \| 500pH$	$100mS \| 1250pH$

Table 4-1: Element values for Ring Oscillator Example

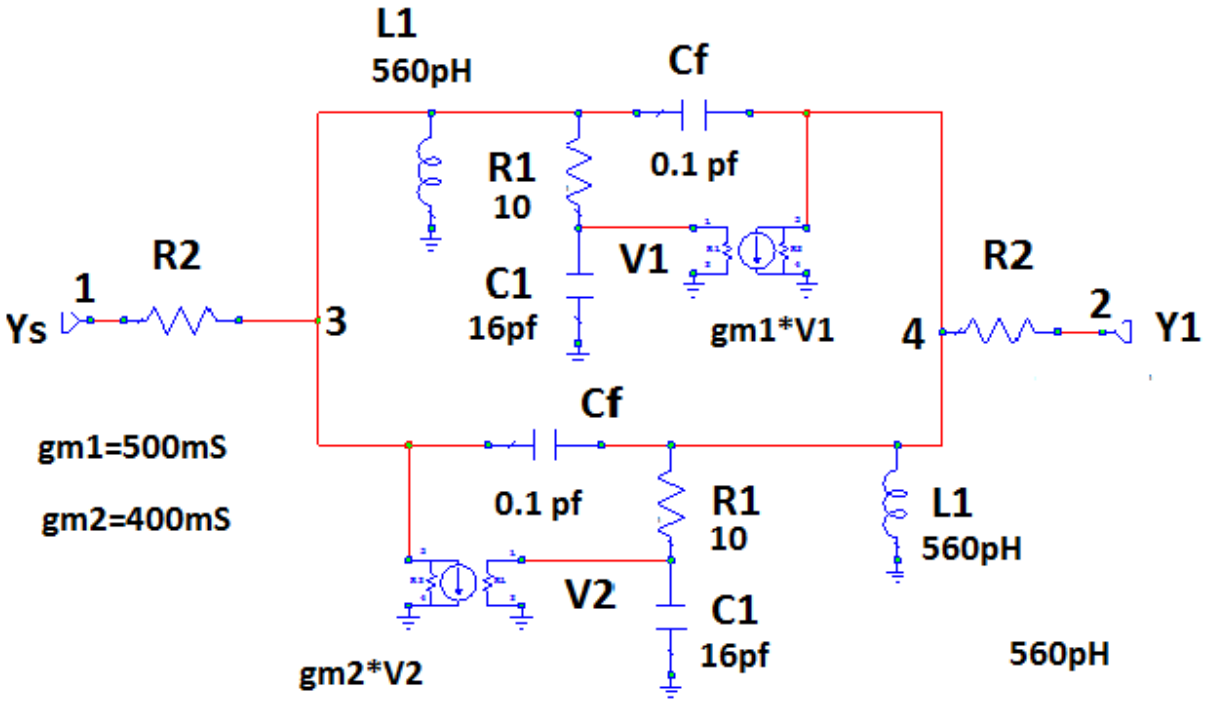

Figure 4-8: Ring Oscillator Schematic

From the nodal equations for admittance the Y matrix of the circuit can be developed as

(4.23)

$$Ymatrix = \begin{bmatrix} G_2 + Y_s & 0 & -G_2 & 0 \\ 0 & G_2 + Y_1 & 0 & -G_2 \\ -G_2 & 0 & T_1 & T_2 \\ 0 & -G_2 & T_3 & T_4 \end{bmatrix}$$

Where the equations that make up the matrix are

$$T1 = G_2 + \frac{1}{sL} + \frac{sC_1}{1 + sC_1R_1} + 2sC_f \tag{4.24}$$

$$T2 = -2sC_f + \frac{gm_2}{1 + sC_1R_1} \tag{4.25}$$

$$T3 = -2sC_f + \frac{gm_1}{1 + sC_1R_1} \tag{4.26}$$

$$T4 = G_2 + \frac{1}{sL} + \frac{sC_1}{1 + sC_1R_1} + 2sC_f \tag{4.27}$$

$$G2 = \frac{1}{R_2} \tag{4.28}$$

This then yields to the equation for the determinant

$$\Delta = (G_2 + Y_s)(G_2 + Y_1)(T_1T_4 - T_2T_3) - G_2^2\{(G_2 + Y_s)T_1 + (G_2 + Y_1)T_4 + G_2^4\} \quad (4.29)$$

From here the zeros of the determinant must be solved. See appendix A for the Maple results showing the calculation of the determinants zeros.

Case 1 has $R_2 = 50$ and $Y_{s=}20mS$ and $Y_{1=}20mS$. Table 4-2 shows the values of the zeros calculated for the circuit values given in case (1). All values are $\sigma + j\omega$ in units of 10^9. From the Pole/Zero analysis it is confirmed that there are indeed zeros in the RHP (right half plane) indicating that the circuit is unstable. From this the frequency of oscillation can be determined by

$$f_{osc} = \frac{im_{root}}{2\pi} \quad (4.30)$$

-298.9277	-39.63539	-2.558709	$4.250831 \pm i8.844$
			-6.25

Table 4-2: Calculated Zeros of Determinant in units 10^9

But in running a simulation of the stability factor K and the auxiliary stability factor B1 an interesting thing happens, they both **falsely** indicate stability as does the stability measures $m\mu 1$ and $m\mu 2$. From equation 4.30 the circuit should oscillate at 1.4075 GHz. The transient simulation shows the frequency of oscillation at 1.11 GHz. The schematics for the four cases can be found in Appendix E. In all circuit types, $4.7V$ zener diodes where added to limit oscillations from growing to unbounded amplitude.

Figure 4-9: Transient Analysis Case 1

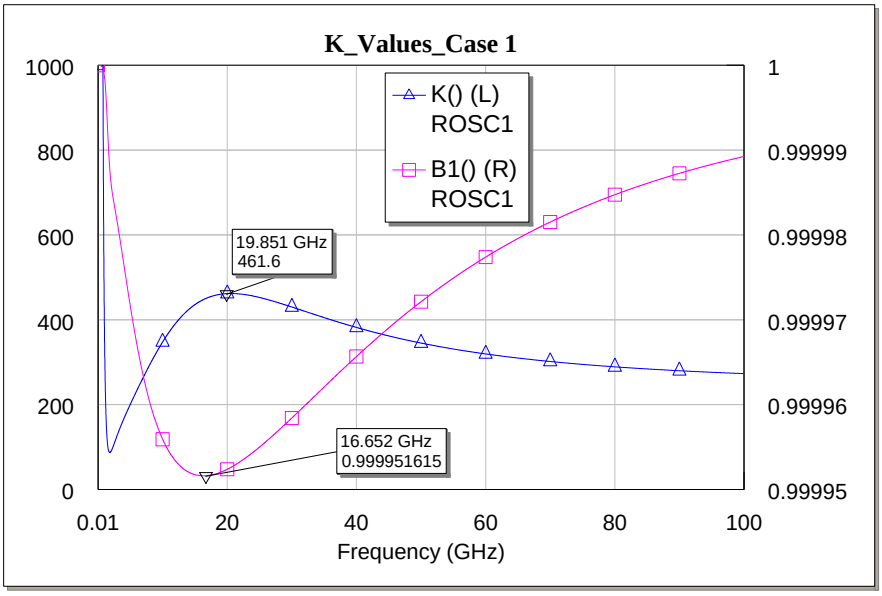

Figure 4-10: K Stability measurement for Case 1

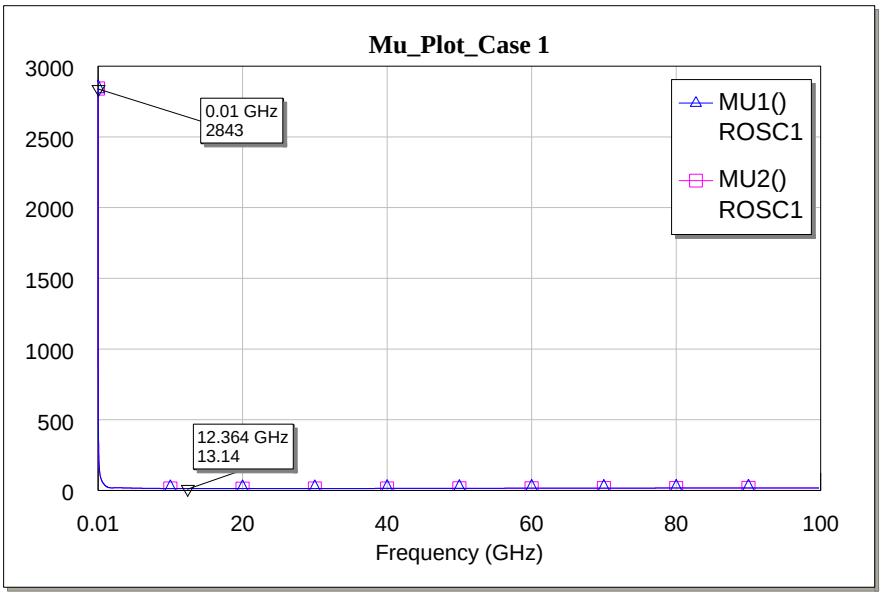

Figure 4-11: Mu Stability Measurement 1

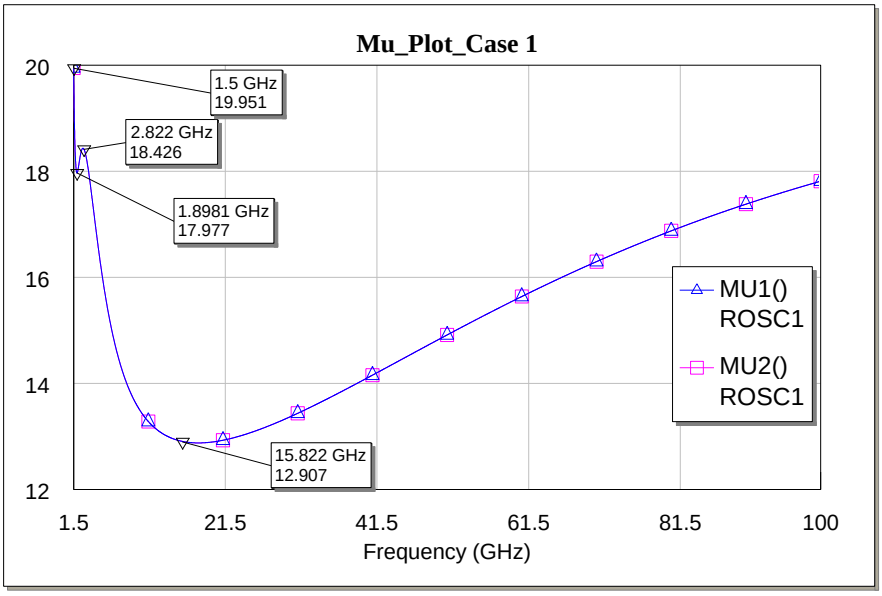

Figure 4-12: Mu Stability Measurement 2

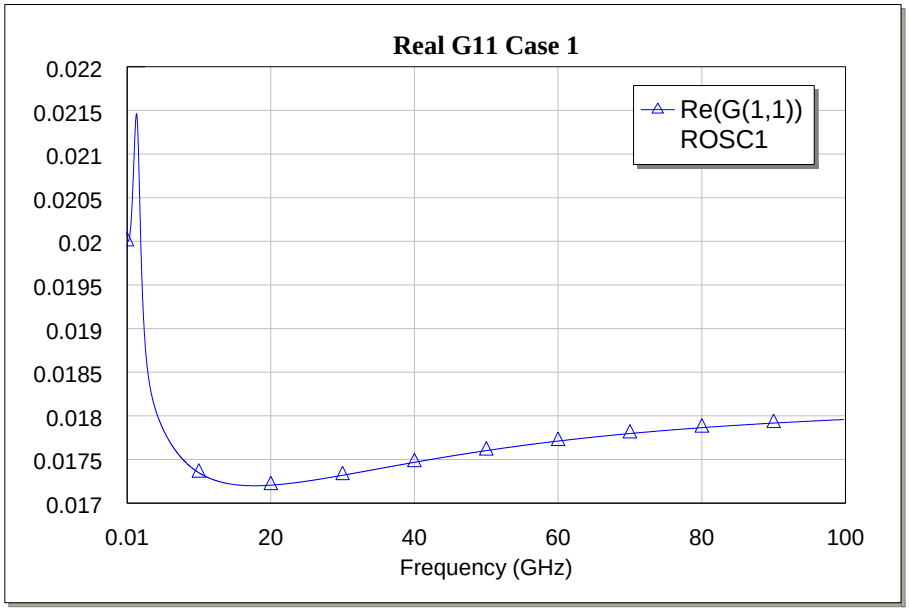

Figure 4-13: G11 Simulation

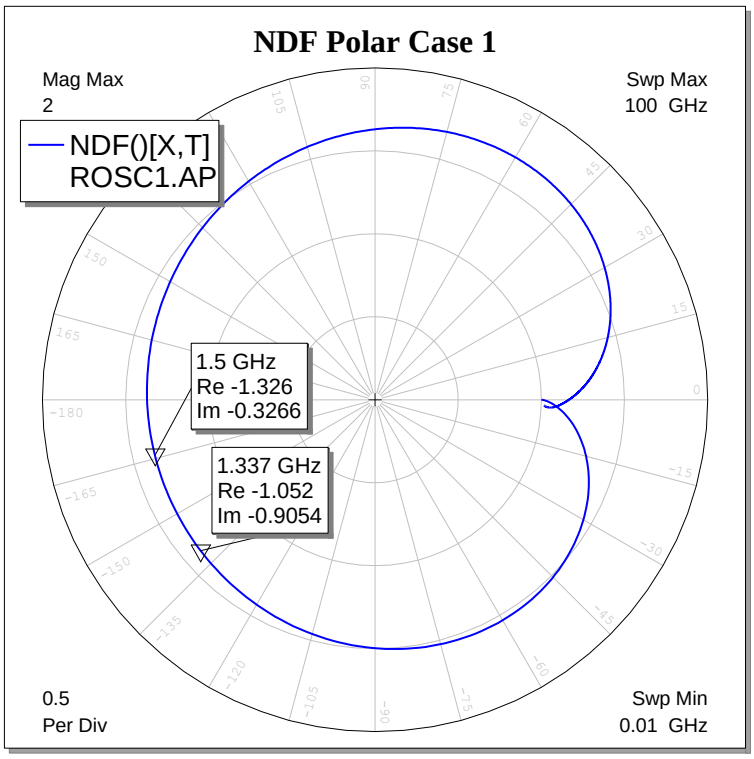

Figure 4-14: NDF Plot Case 1

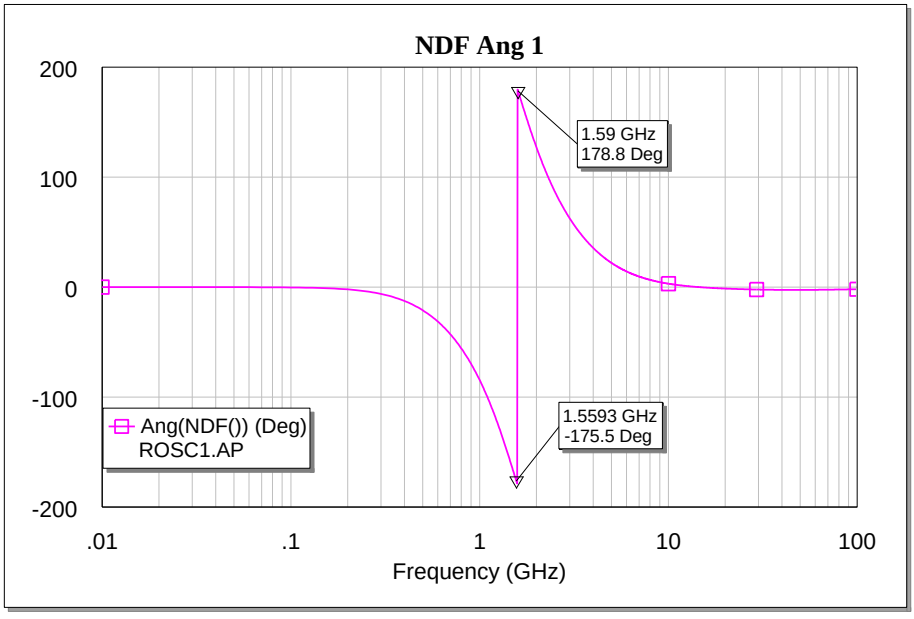

Figure 4-15: NDF phase plot for case 1

As shown in Figure 4-14 the NDF analysis correctly predicts that the circuit will oscillate. The NDF indicates the circuit will oscillate at 1.59 GHz and the transient simulation shows the oscillation occurring at 1.11 GHz. The pole/zero analysis indicates oscillation occurring at 1.4075 GHz. As shown there is some discrepancy as to the actual oscillation frequency but no disagreement to the fact that the circuit is unstable under these circuit values. Conversely the traditional stability measurements all indicated the circuit was stable. The K stability measure gives the widest margin of stability of all the measures but even the Mu measure gives quite a bit of margin up to 100GHz.

4.5 Example 2: K/ B correctly predicts instability

In example 2 the value for R2 is changed from 50Ω to 5Ω and $Y_{s=}20mS$ and $Y_{1=}20mS$. In looking at the Pole/zero analysis the roots change very little from condition 1 but in this case K, $B1$ and $m\mu$ all predict correctly that the circuit is unstable. See appendix B for detailed analysis of how to calculate the zeros from the determinant for this case. All table values are $\sigma + j\omega$ in units of 10^9.

-309.3992	-37.16814	-2.539824	$3.766541 \pm i8.7194$
			-6.25

Table 4-3: Pole Zero analysis for case 2 in units 10^9

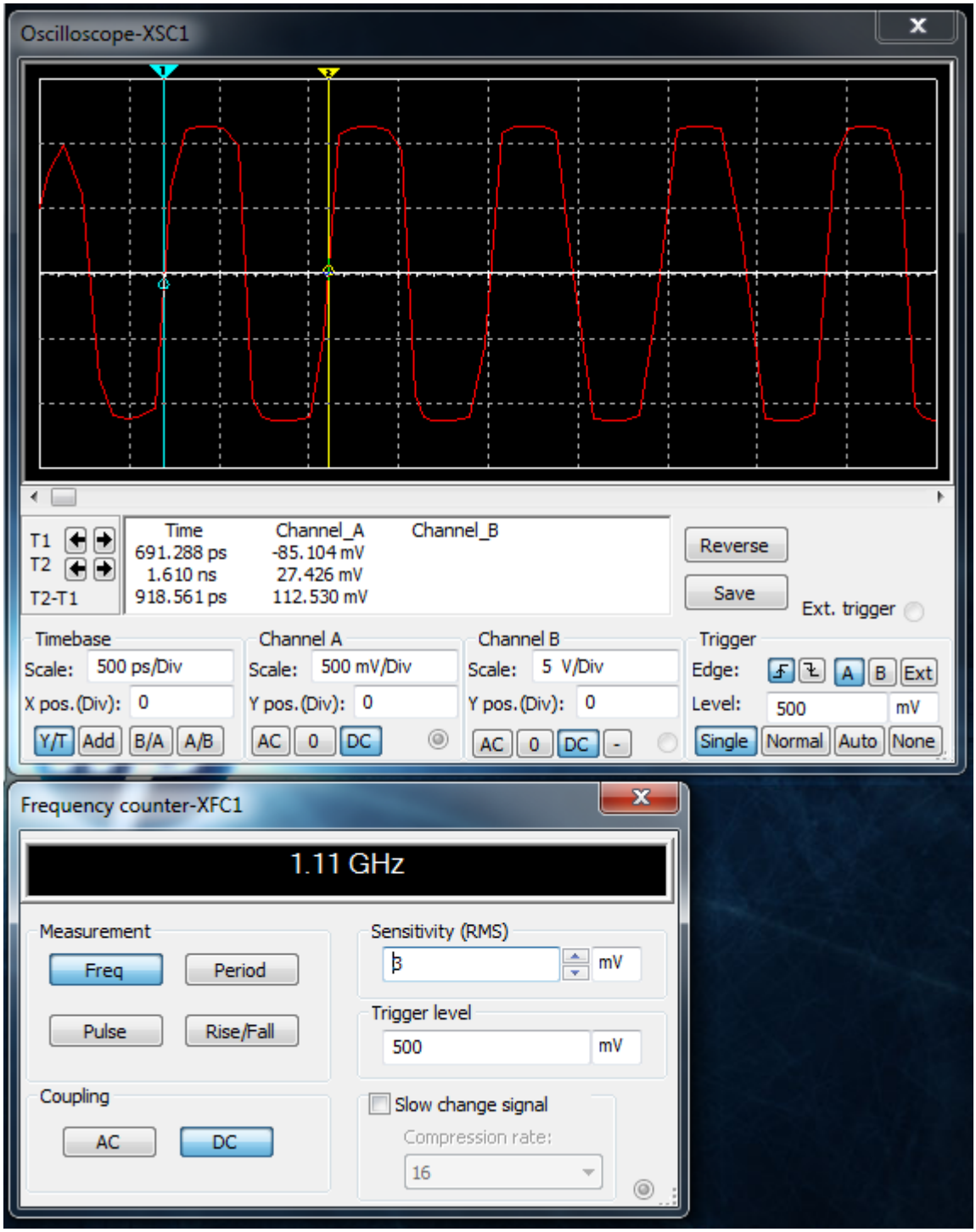

Figure 4-16: Transient Analysis Case 2

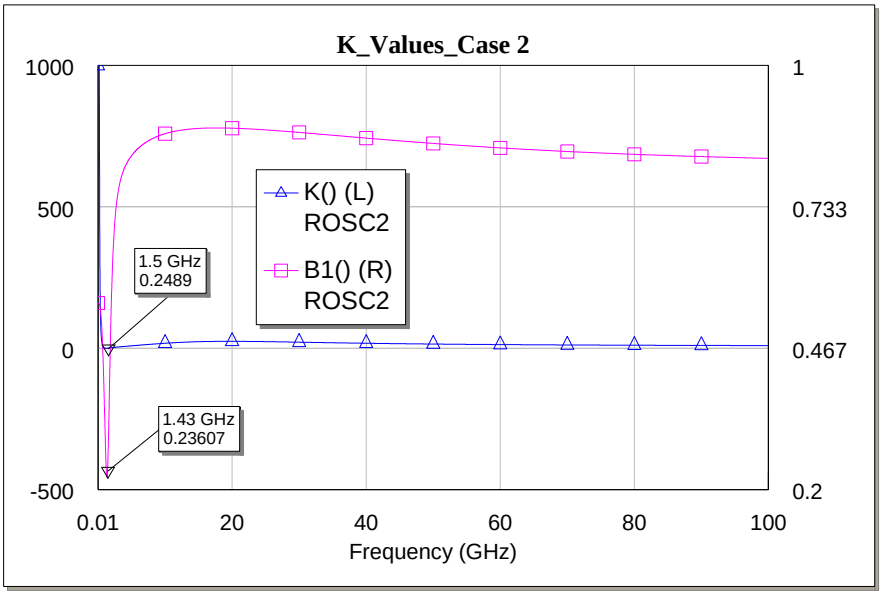

Figure 4-17: K Values for Case 2

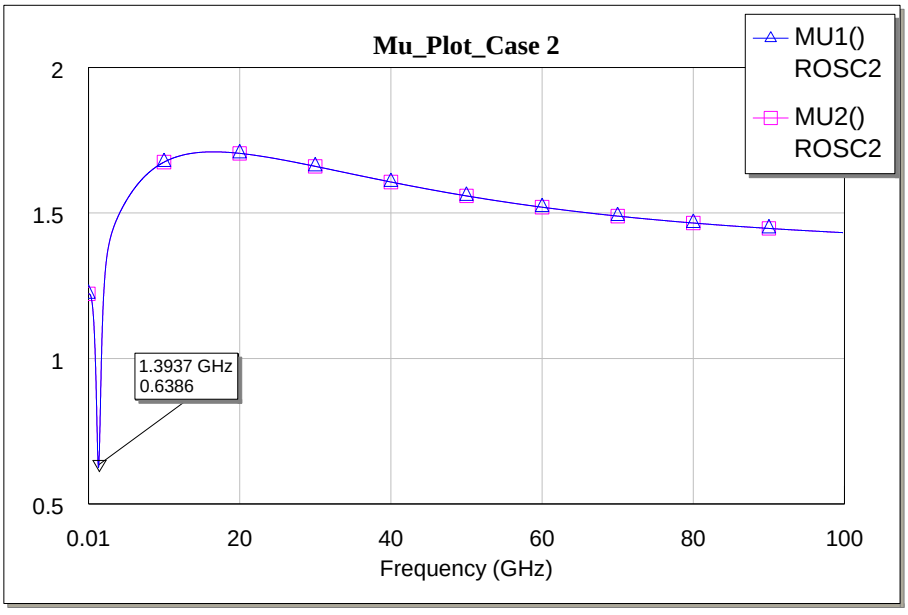

Figure 4-18: Mu values for Case 2

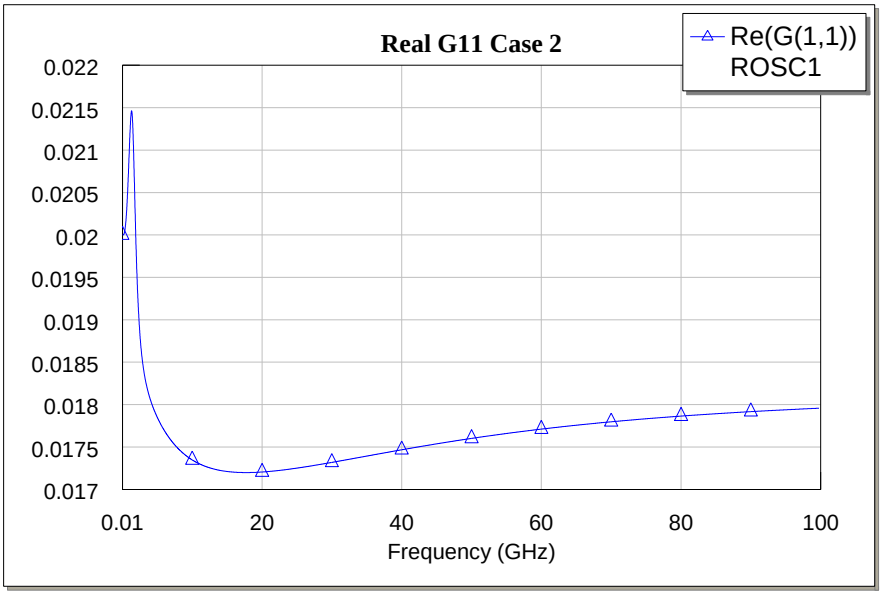

Figure 4-19: Real G11 for Case 2

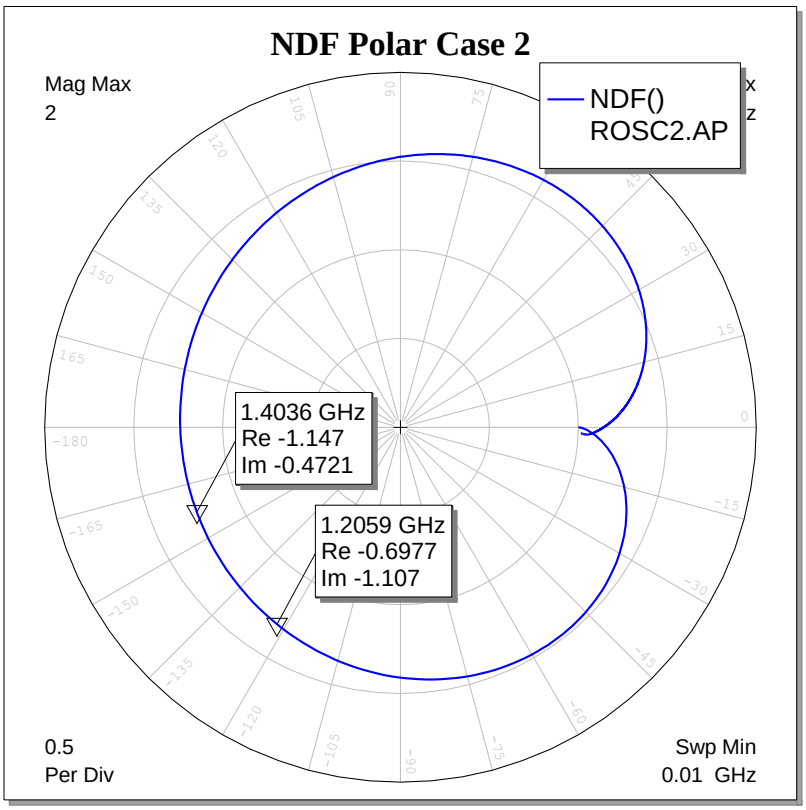

Figure 4-20: NDF for Case 2

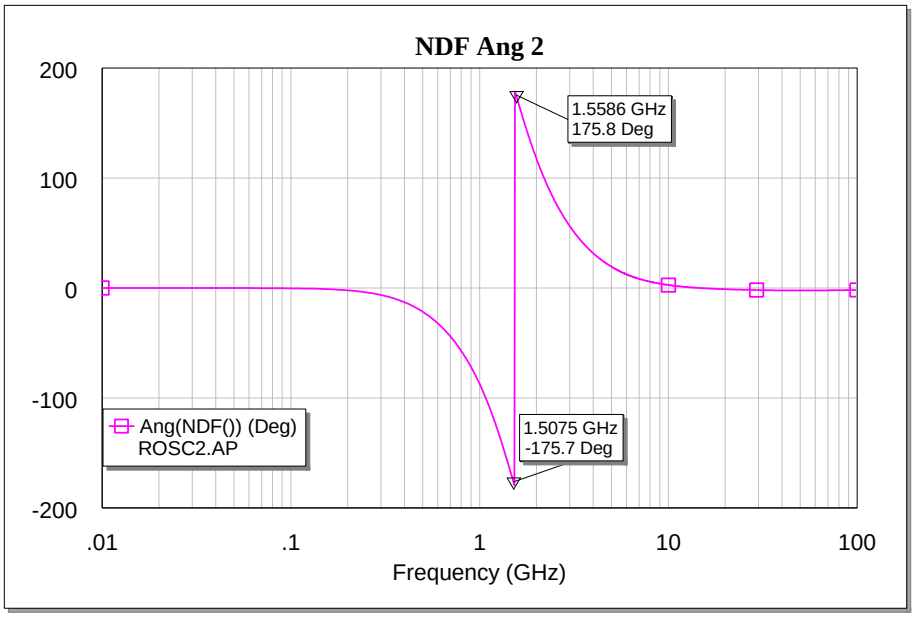

Figure 4-21: NDF phase plot for case 2

As in case 1 the NDF analysis correctly predicts that the circuit will oscillate. The NDF indicates the circuit will oscillate at 1.5075 GHz and the transient simulation shows the oscillation occurring at 1.11 GHz. The pole/zero analysis indicates oscillation occurring at 1.38877 GHz. As in case 1 there is some discrepancy as to the actual oscillation frequency but no disagreement to the fact that the circuit is unstable under these circuit values. In this case however the standard stability measures, K, $B1$ and $m\mu 1$ and $m\mu 2$ all correctly predict instability.

4.6 Example 3: K/ B correctly predicts instability

In example 3 the value for R2 remains at 5Ω and in addition $Y_s = 150_{ms} \| 500_{pH}$ and $Y_1 = 100_{ms} \| 1250_{pH}$. In looking at the Pole/zero analysis the majority of the roots are stable and fall in the LHP (Left Half Plane) but there are two that fall in the RHP (Right Half Plane). See appendix C for detailed analysis of how to calculate the zeros from the determinant for this case. All values are $\sigma + j\omega$ in units of 10^9.

-445.8921	-29.21557	-5.748229	-2.94421	-1.831058	$0.07404047 \pm i8.167585$
-6.25					

Table 4-4: Pole Zero Analysis Case 3 in units 10^9

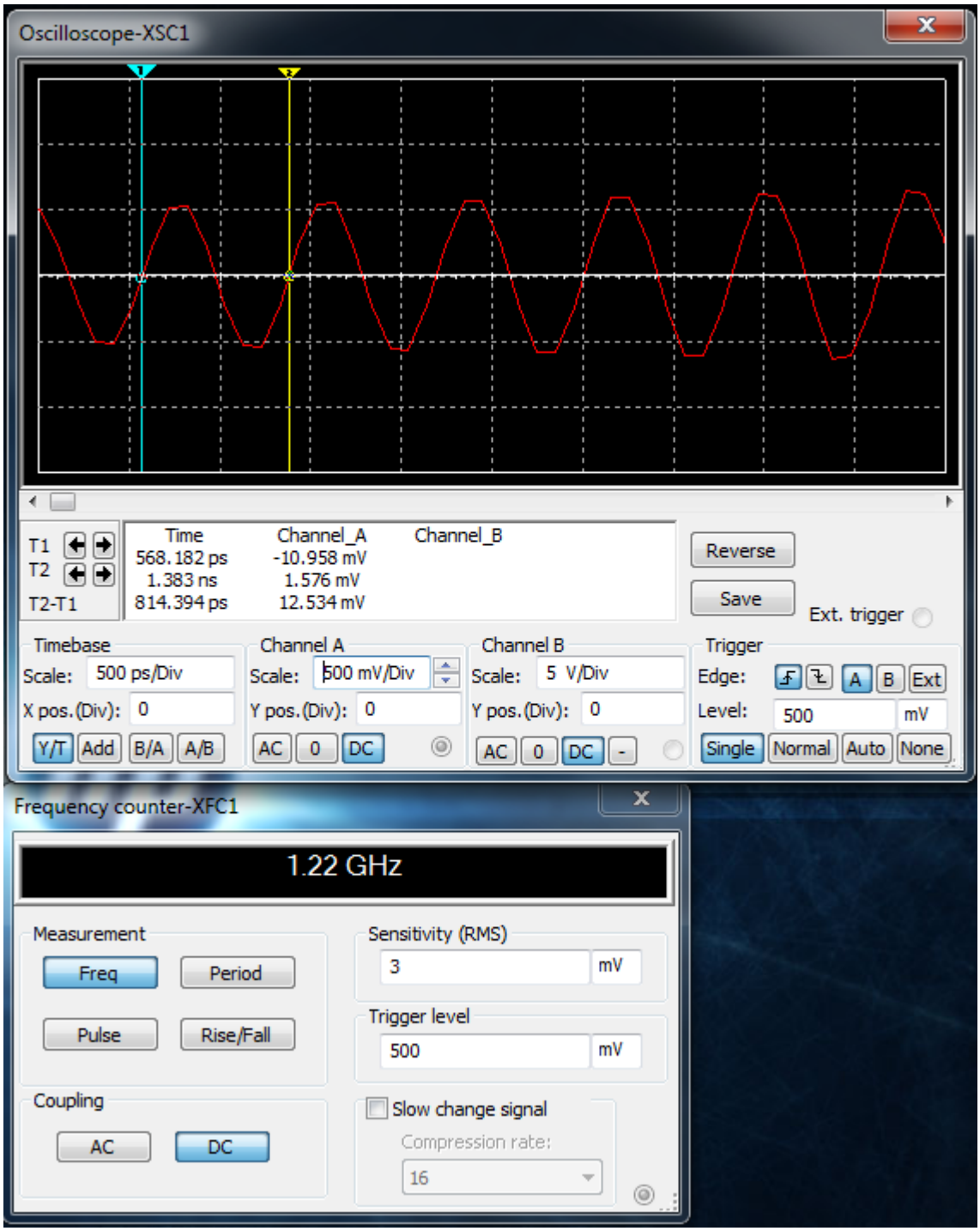

Figure 4-22: Transient Analysis Case 3

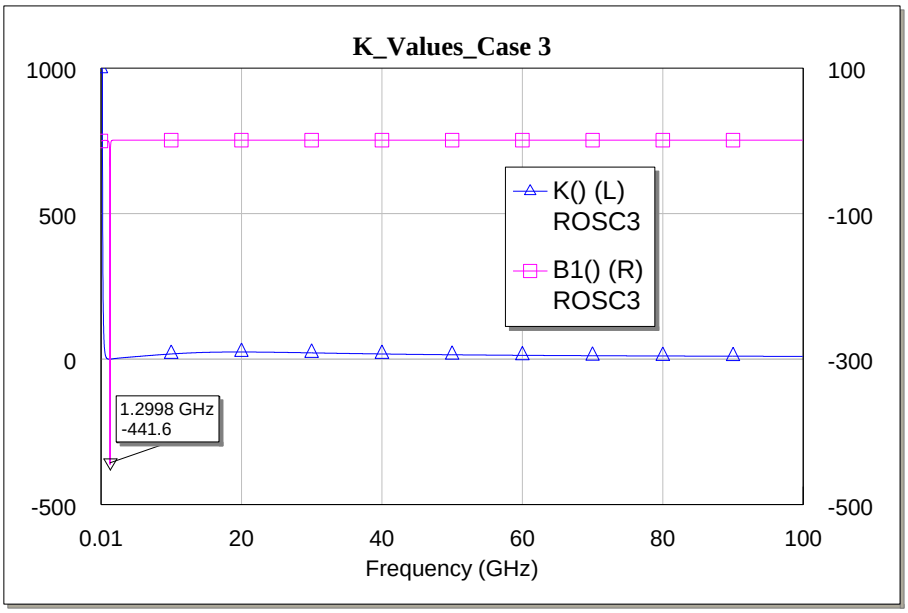

Figure 4-23: K Values for Case 3

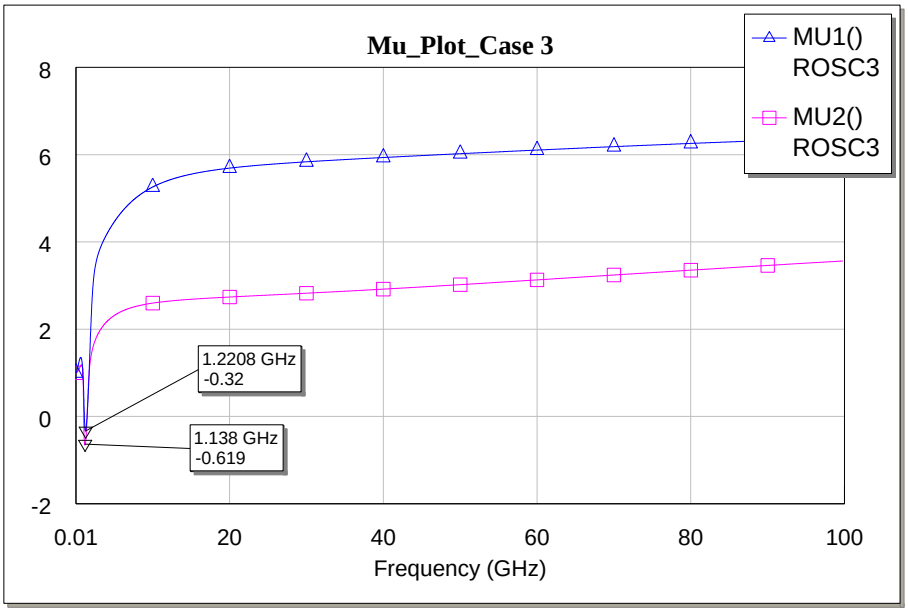

Figure 4-24: Mu Values for Case 3

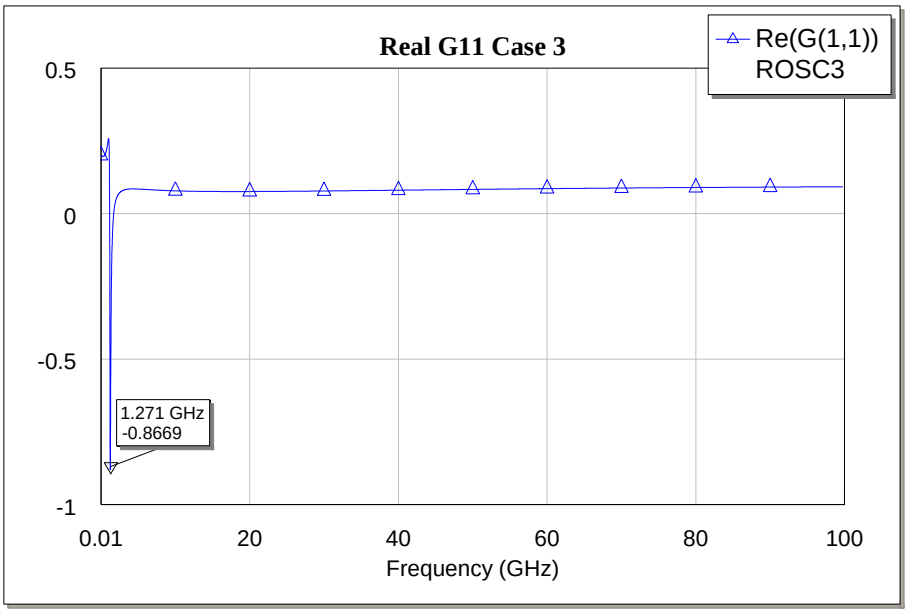

Figure 4-25: G11 Values for Case 3

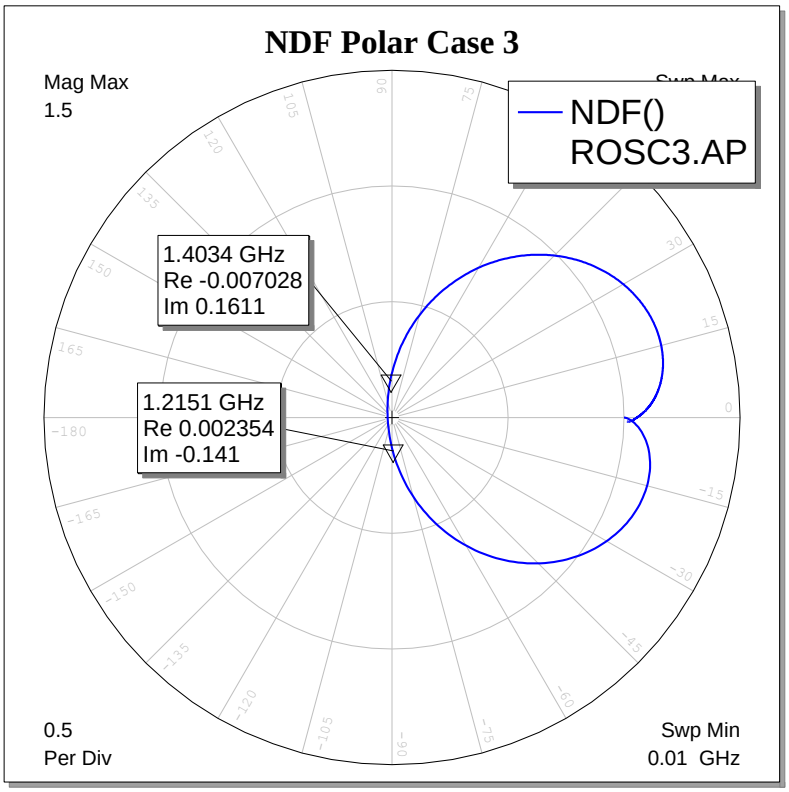

Figure 4-26: NDF Plot for Case 3

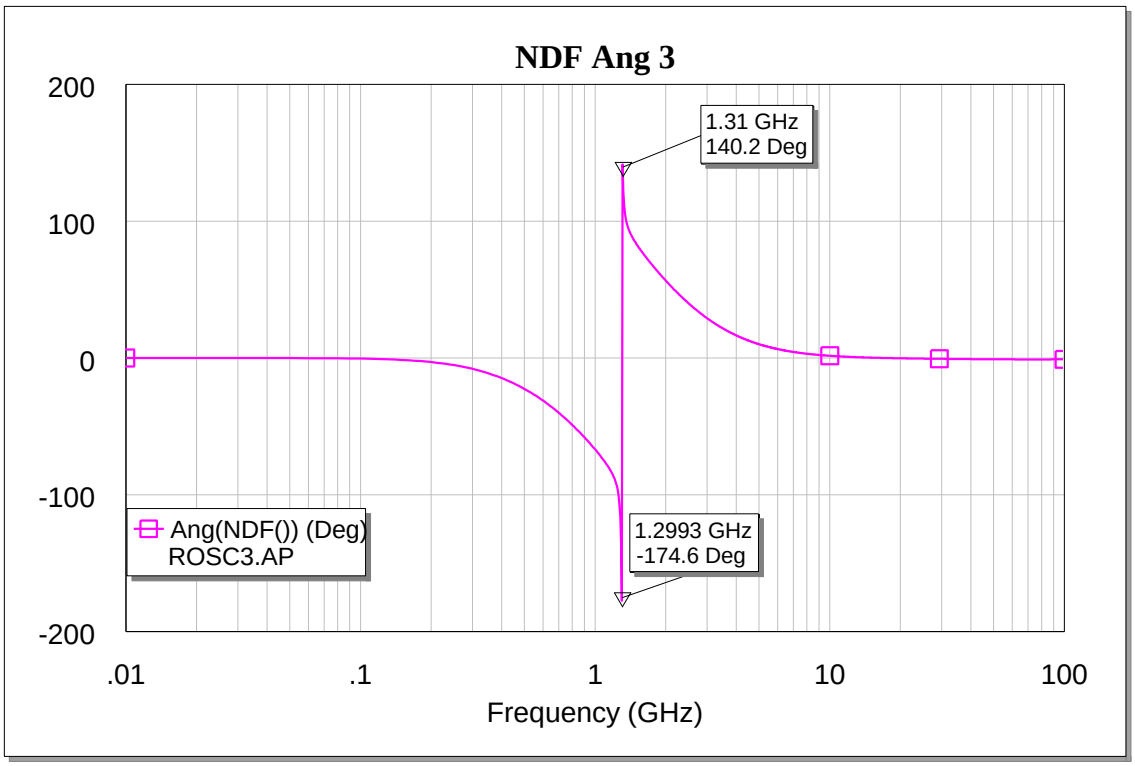

Figure 4-27: NDF phase plot for case 3

As in case 2 the NDF analysis correctly predicts that the circuit will oscillate. The NDF indicates the circuit will oscillate at 1.2993 GHz and the transient simulation shows the oscillation occurring at 1.22 GHz. The pole/zero analysis indicates oscillation occurring at 1.2999 GHz. In this case the frequency of oscillation indicated in the NDF, transient and pole/zero are much closer than the first two cases. Additionally the standard stability measures, K, $B1$ and $m\mu 1$ and $m\mu 2$ all correctly predict instability.

4.7 Example 4: K/ B incorrectly predicts instability

In example 4 the value for R2 remains at 5Ω and in addition $Y_s = 50_{ms} \| 500_{pH}$ and $Y_1 = 100_{ms} \| 1250_{pH}$. In looking at the Pole/zero analysis all of the roots are stable and fall in the LHP (Left Half Plane) but the traditional measures all indicate instability. See appendix D for detailed analysis of how to calculate the zeros from the determinant for this case. All values are $\sigma + j\omega$ in units of 10^9.

-385.2614	-36.56534	-7.886135	-2.96513	-1.83377	$-0.167599 \pm i8.46737574$
					-6.25

Table 4-5: Pole Zero Analysis Case 4 in units 10^9

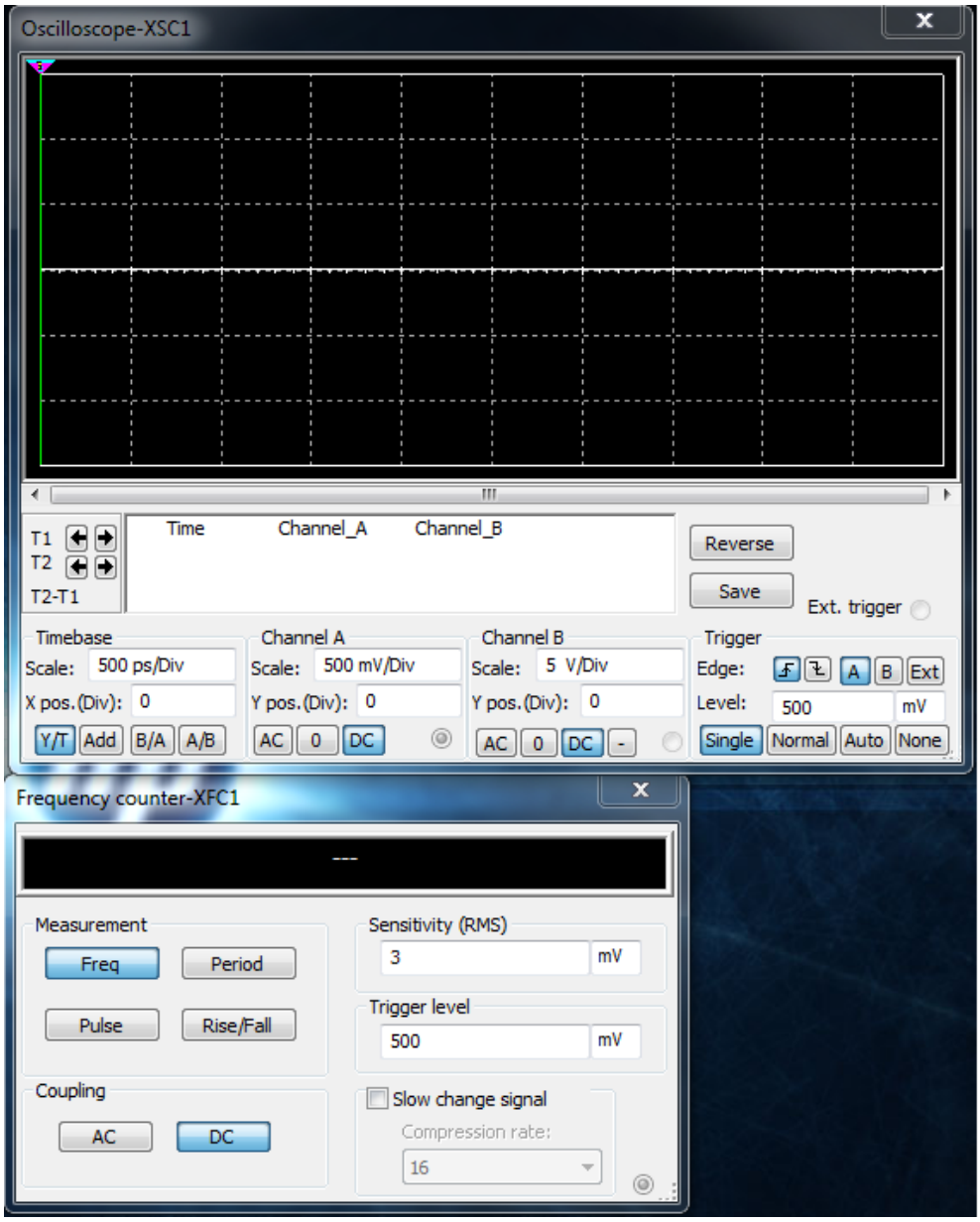

Figure 4-28: Transient Analysis Case 4

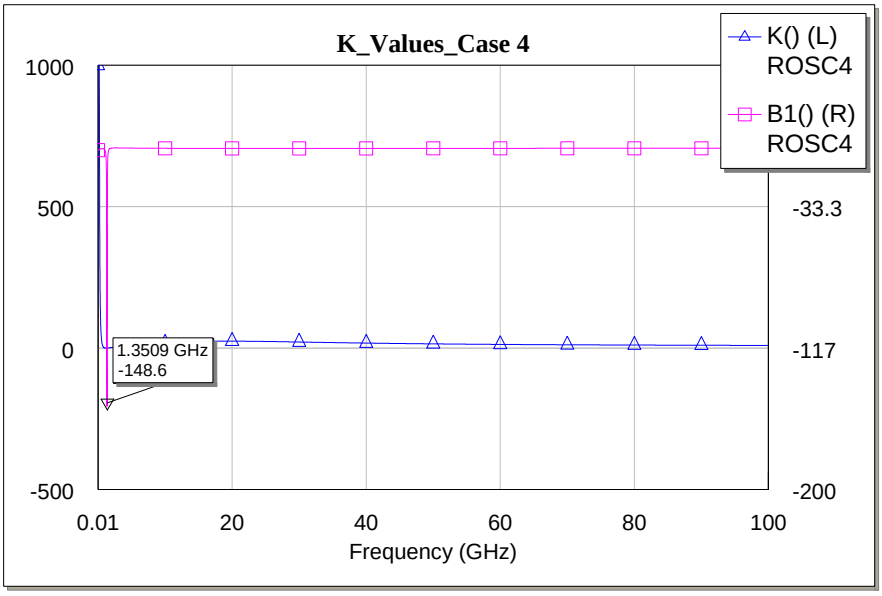

Figure 4-29:K Values for Case 4

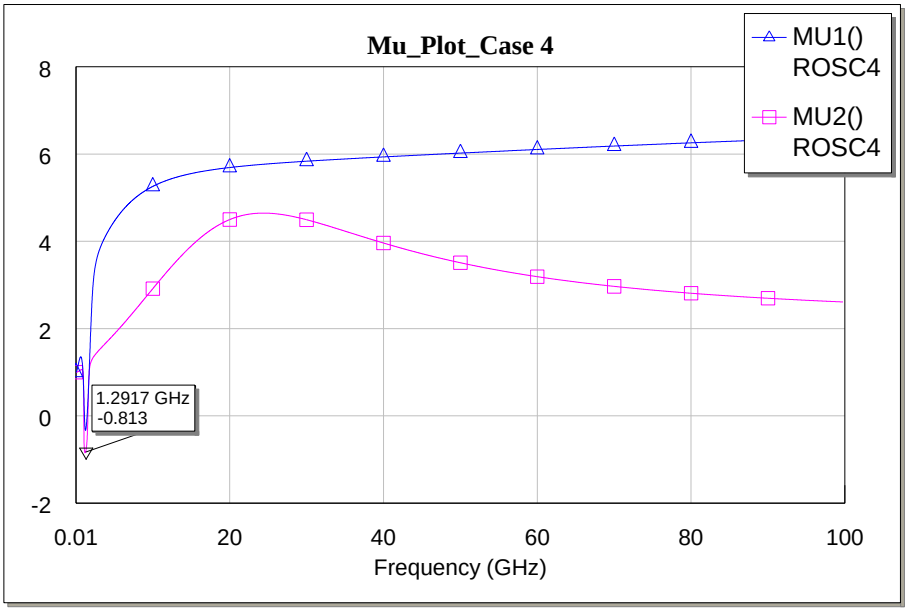

Figure 4-30: Mu values for Case 4

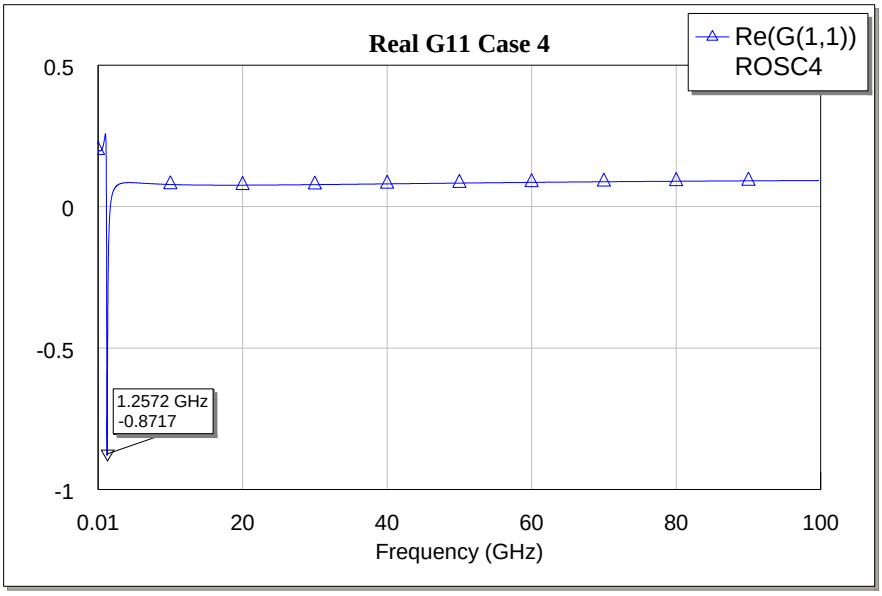

Figure 4-31: G11 values for Case 4

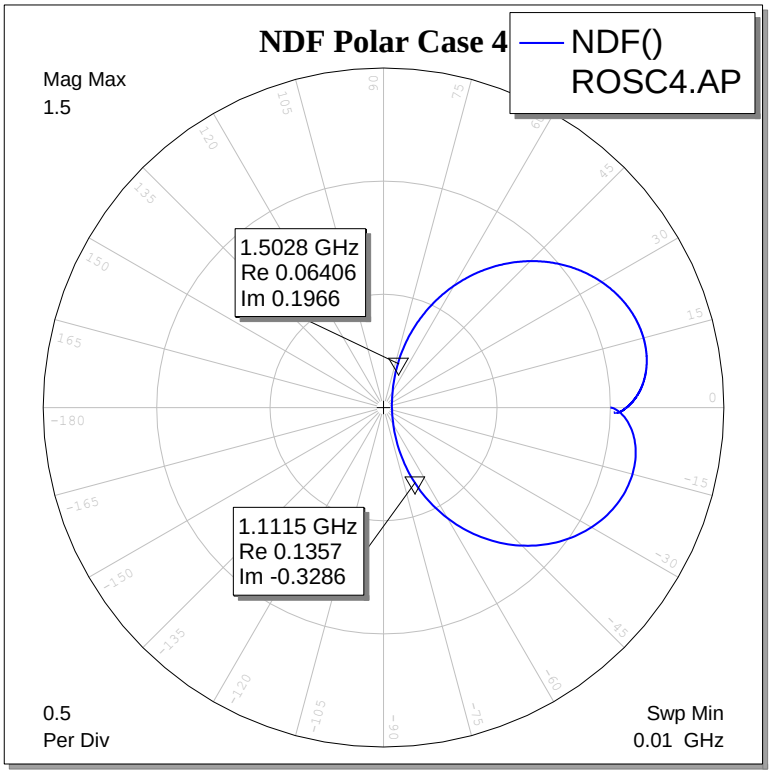

Figure 4-32: NDF Values for Case 4

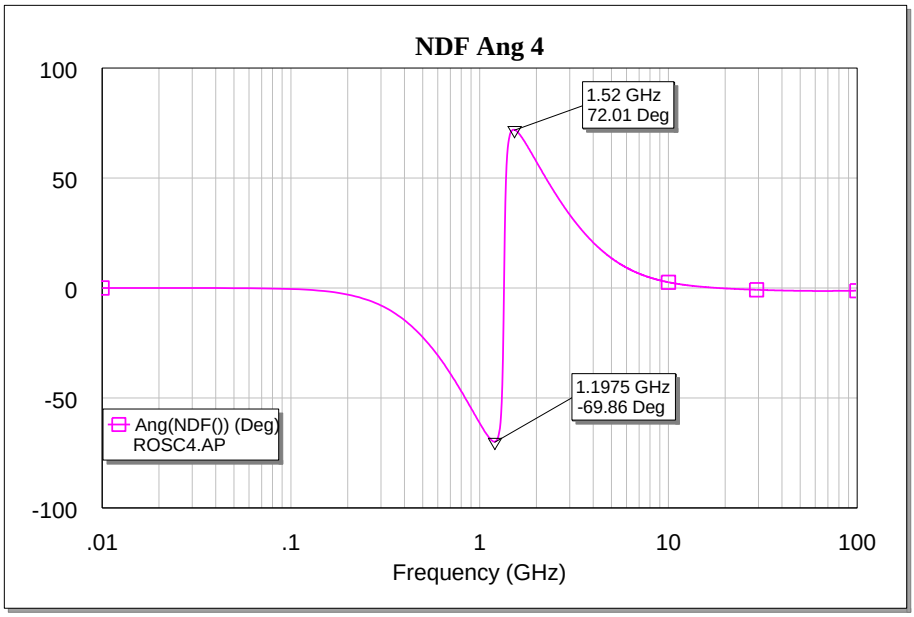

Figure 4-33: NDF phase plot for case 4

In the final case the NDF simulation, by inspection of the polar plot, the pole/zero analysis and transient simulation shows that the circuit is stable and does not oscillate but the standard stability measures all indicate instability occurring from 1.2572 GHz to 1.3509 GHz depending on the stability measure used.

The four case examples show that using the traditional stability measures K, $B1$ and $m\mu 1$ and $m\mu 2$ are flawed and should not be relied upon exclusively as proof of circuit stability. To determine the stability of the unloaded linear Two-Port network the circuit can either be assessed by a careful analysis of the characteristic roots from the circuit determinant, but this is likely to be impractical for large circuits with many nodes, or through an NDF analysis as previously shown. The requirement that $K > 1$, and $B1 > 0$ then insures that no combination of output source and source loading can cause instability.

Chapter 5 - **Nonlinear Stability Analysis**

Power amplifiers are nonlinear devices that can exhibit undesired effects that may be a function of the signal power applied, the frequency of operation, bias conditions, temperature and source and load attached in addition to the effects outlined in chapter 3. These effects may be manifested as spurious oscillations, bifurcation effects or chaos phenomenon. Bifurcation occurs when a particular parameterized value becomes structurally unstable [10]. Linear stability analysis does not include harmonics or the effects of compression and intermodulation that must be accounted for in a physical device.

The goal of the nonlinear stability analysis is to perform a large-signal analysis that will uncover the presence of unstable operation at a particular stage and to provide information that can aid in designing a circuit to eliminate or stabilize it.

5.1 Large Signal S-parameters

Large signal S-parameters are used to compute the equivalent of an S-parameter that one is often familiar with but to do so under large signal excitation conditions. When these are generated in conjunction with nonlinear device models the effects of compression and intermodulation can now be evaluated in the simulation. The measurement also allows for the selection of harmonic frequencies to evaluate the conversion loss or gain in mixers and multipliers [9]. Like the small signal analysis outlined in chapter 4 to check stability of a complicated N-node network by examining the S-parameters obtained by reducing the complicated network to a two port network, the same may be done here under large signal conditions. S-parameters taken under large signal conditions are often referred to as *HOT S- Parameters.* The same requirement that $K > 1$ and $|\Delta_s| < 1$ at all frequencies is checked [18].

5.2 Auxiliary Generator method

The Auxiliary generator method is a method that allows for the detection of oscillation conditions by examining the complex large signal admittance at sensitive nodes in the circuit. In this approach the oscillation startup condition occurs when the conditions of (5.1) are met.

$$Re(Y_T) < 0 \; and \; Im(Y_T) = 0 \tag{5.1}$$

In simulation this is done by connecting a voltage generator in series with an ideal filter to the node of interest and examining the total admittance, Y_T . The preferred connection points are device terminals that contain feedback points such as on the base or gate of a transistor. The ideal filter is implemented through an ideal impedance block, Z1P1, as shown in Figure 5-5. It presents a perfect short to the generator frequency and a small band of frequencies around its center point that is defined in the simulation by variable block 4 shown in Figure 5-1. All other frequencies, including the harmonics, appear as open circuit at this connection point.

Figure 5-1: Simulation conditional statement

The simulation is designed to sweep through a band of frequencies defined in the parameter sweep block and collect auxiliary generator voltage and current values. The ratio of the phasor current I_{AG} entering the node and the generator voltage V_{AG} represents the total admittance function at the node. This is shown mathematically as

$$Y_T(V_{AG}, \emptyset_{AG}, \omega_{AG}) = \frac{\bar{I}_{AG}}{V_{AG} e^{j\emptyset} AG} = Y_L(\omega_{AG}) + Y_N(V_{AG}, \emptyset_{AG}, \omega_{AG}) \quad (5.2)$$

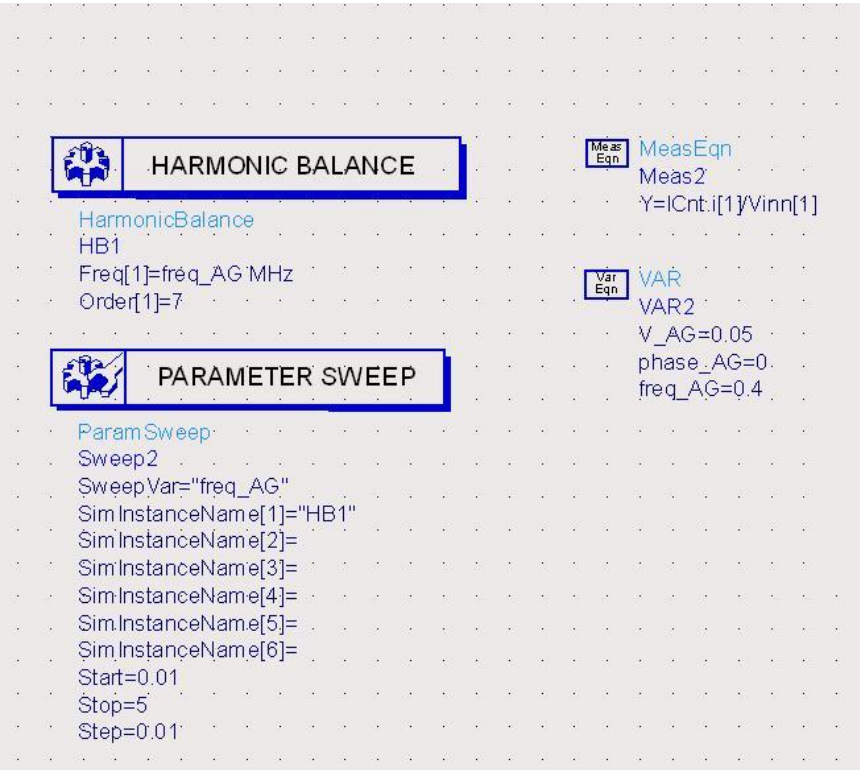

Figure 5-2: Simulation control equations

The circuit in Figure 5-5 is shown to illustrate the method. In this circuit a nonlinear element is implemented in the circuit by a voltage controlled current source containing the polynomial value of $i_{nl} = -0.2v_{C1} + 0.0375v_{C1}^3$.

By plotting the total admittance expression and examining the real and imaginary components for the oscillation start up condition required from (5.1) the conditions for oscillation are met at a frequency of approximately 1.570 MHz as shown in Figure 5.3. The oscillation occurs because of a sufficient amount of energy is delivered by the nonlinear element to compensate for that dissipated at the load resistor. This manifests itself as an oscillation at the resonant frequency of the circuit [10].

The solution to the steady state oscillation in many cases can be found from numerical solutions in the frequency domain using harmonic balance simulations. All commercial simulation packages today contain harmonic balance simulators. The circuit of Figure 5-3 is simulated with Agilent ADS utilizing this method. The results of a transient analysis to confirm the oscillatory condition and frequency of oscillation is contained in appendix F

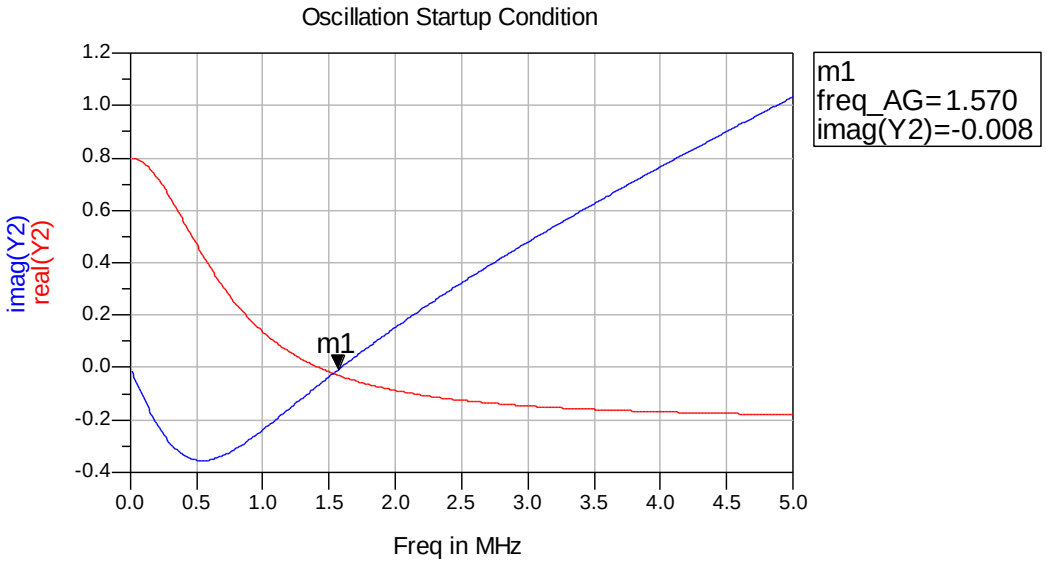

Figure 5-3: Auxiliary Generator Oscillation Startup Condition

When plotting the total admittance, Y_t, it is often convenient to plot the imaginary component of Y_t against its real component as shown in Figure 5.6. Once this is done a family of constant amplitude curves with variable frequency,$\_AG$, can be plotted to obtain a good estimate of the oscillation frequency.

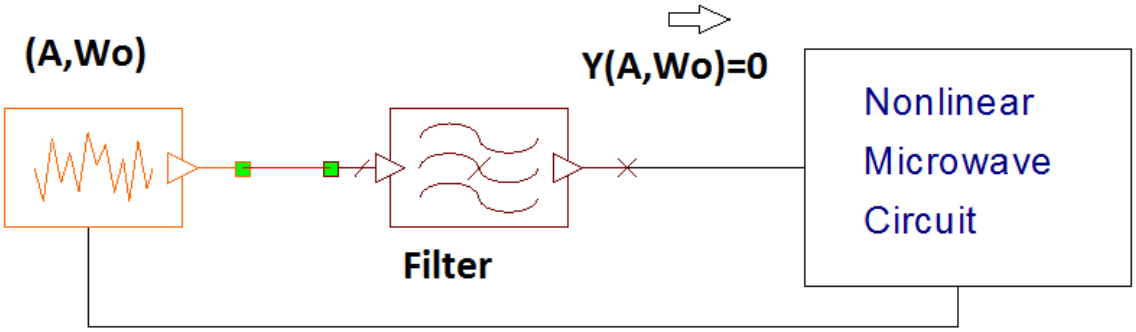

Figure 5-4: Auxiliary generator Block Diagram

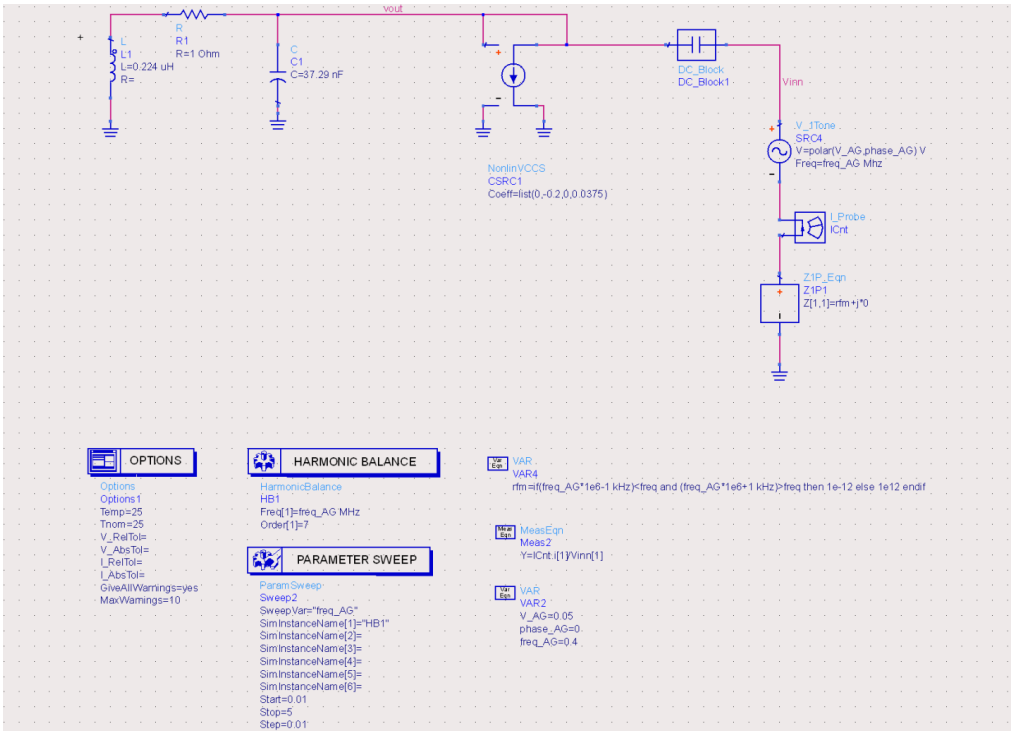

Figure 5-5: Auxiliary generator simulation schematic

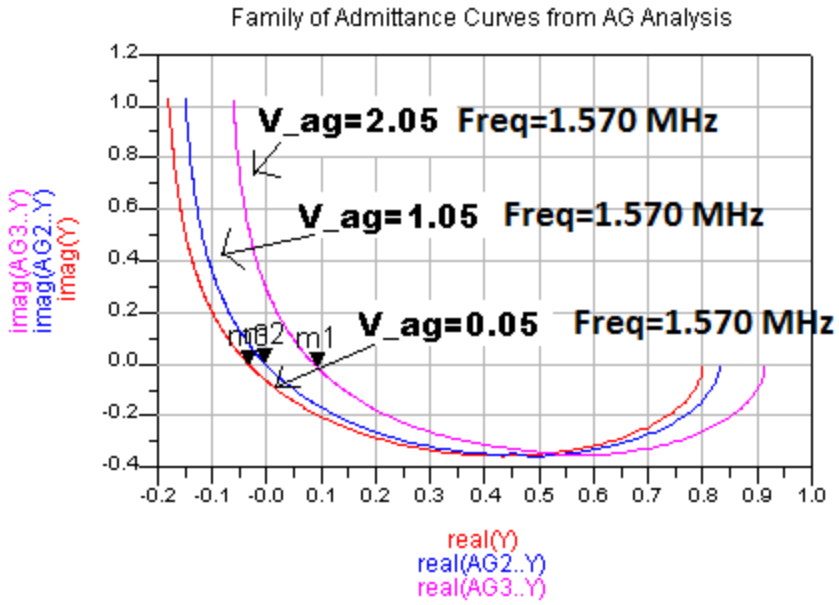

Figure 5-6: Simulation results for three V_ag values

Using the auxiliary generator method the frequency and amplitude of the generator is used to find the conditions necessary for the circuit to oscillate. Since a harmonic balance simulation is used with the auxiliary generator, the circuit is not allowed to converge to a DC solution that often times occurs in harmonic balance simulations due to bias sources that force the simulation to a mathematical solution without physical existence [10].

An extension of this process for amplifier design could include optimization goals that would be controlling circuit values for stabilization networks such that the condition for oscillation is avoided over the frequency range $freq\_AG$ and the amplitude V$_AG$. In this case the goal would become

$$Re(Y_T) > 0 \tag{5.3}$$

Chapter 6 - **Characteristics of GaN**

The 1 Watt pulse modulated power amplifier with internal blanking switch was designed in a popular Gallium Nitride (GaN) HEMT foundry process. The HEMT (High Electron Mobility Transistor) transistor is so named because of its superior transport properties of electrons in a well of lightly doped semiconductor material [17]. This is a three metal interconnect process on Silicon Carbide (SiC) that enables high power density, greater than four times the power density of GaAs and ten times the thermal conductivity. The process is designed for high gain and high power operation to 6GHz.

This technology is ideally suited in the design of FET limiters, FET switches, high power FET amplifiers, broadband amplifiers, high efficiency amplifiers and in any application where high circulating currents and voltages are present. The excellent thermal conductivity of SiC makes for an efficient thermal conduit through the substrate to the backside metalization to remove heat.

An added benefit of the GaN process is that it is has extremely low parasitic gate capacitances that enable it to switch extremely fast. This is possible in part because much smaller devices can be built for a given power when compared to a competing GaAs technology. In addition the GaN technology has a much greater drain to source breakdown voltage which lends itself well for high efficiency designs that develop drain voltages in excess of $3.65V_{DD}$ as is the case in class E operation as was outlined in chapter 2.

Some of the key features of the GaN HEMT process is illustrated in Table 6-1.

FET Supply	V_d	28	V
Gain	dB	19	3.5 GHz
Gate Length		0.4	um
Power Density	W	4	W/mm
Efficiency	PAE	60	% @ 3.5 GHz
MIM capacitor	Breakdown	150	V
TaN resistors	Sheet resistance	12	Ohms/sq
Substrate thickness		100	um
Reticule size		10 X 10	mm

Table 6-1: GaN features from popular foundry [19]

Chapter 7 - **Thermal Analysis**

GaN based MMIC's are designed for high power applications with power densities on the order of 4 Watts/mm of transistor periphery while maintaining good reliability for junction temperatures up to 225° C. This being said though it is imperative to remove as much heat as possible thru good heat sinking techniques and to do a comprehensive analysis of the temperature generated and where the heat is concentrated so that thermal feedback instabilities, as outlined in chapter 3, don't occur. Increased die temperature also reduces reliability. For this design the specification called for a die temperature of < 180° C.

7.1 Thermal Fundamentals

If a semiconductor material is mounted to a block of material attached to an infinite heat sink and the assumption is made that power in the device is flowing uniformly into the upper surface of the block, with a isothermal upper and lower surface, then this type of heat flow will occur in a vertical manner and is known as columnar heat flow as depicted in Figure 7-1 [12]. The temperature difference between the top and bottom surface is

$$\Delta T = \frac{PH}{KA} \tag{7.1}$$

Where K is the thermal conductivity, P is the power, H is the die thickness and A is the die area.

The thermal resistance is analogous to electrical resistance and is defined as

$$R_\theta = \frac{\Delta T}{P} = \frac{H}{KA} \qquad (7.2)$$

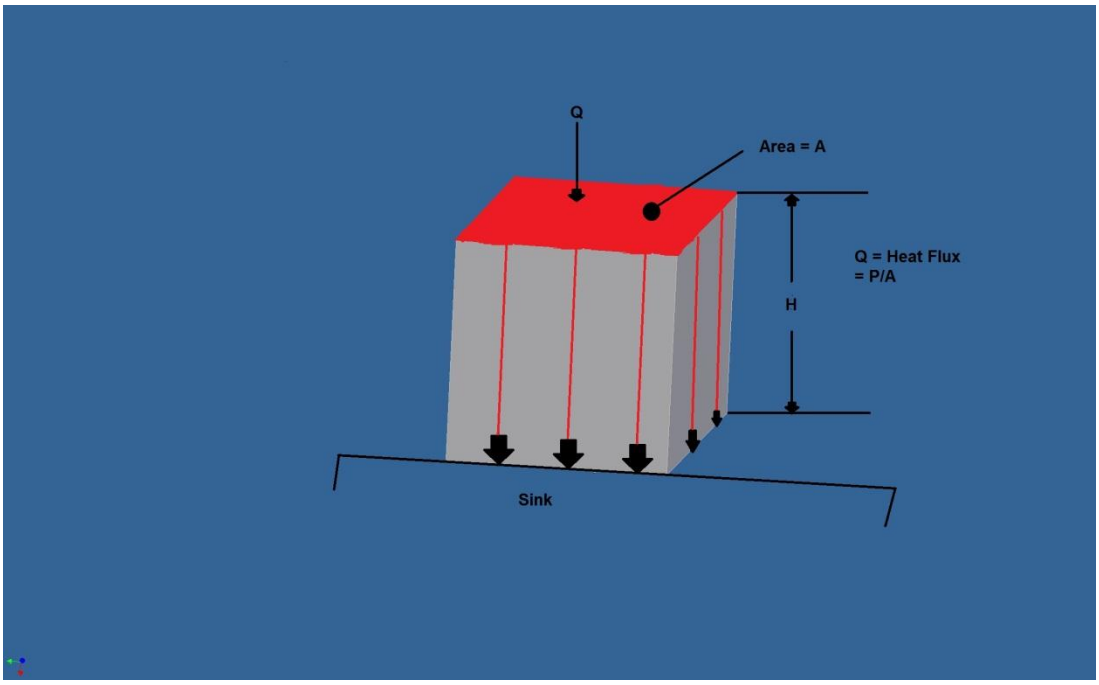

Figure 7-1: Columnar heat flow

Spreading is a heat flow characterized by a heated area that is much smaller than the die itself. This is illustrated in Figure 7-2 and the following expression is derived in [12]. A constant heat flux applied to a circle of diameter d has a thermal resistance of

$$R_\theta = \frac{1}{\pi K d} \qquad (7.3)$$

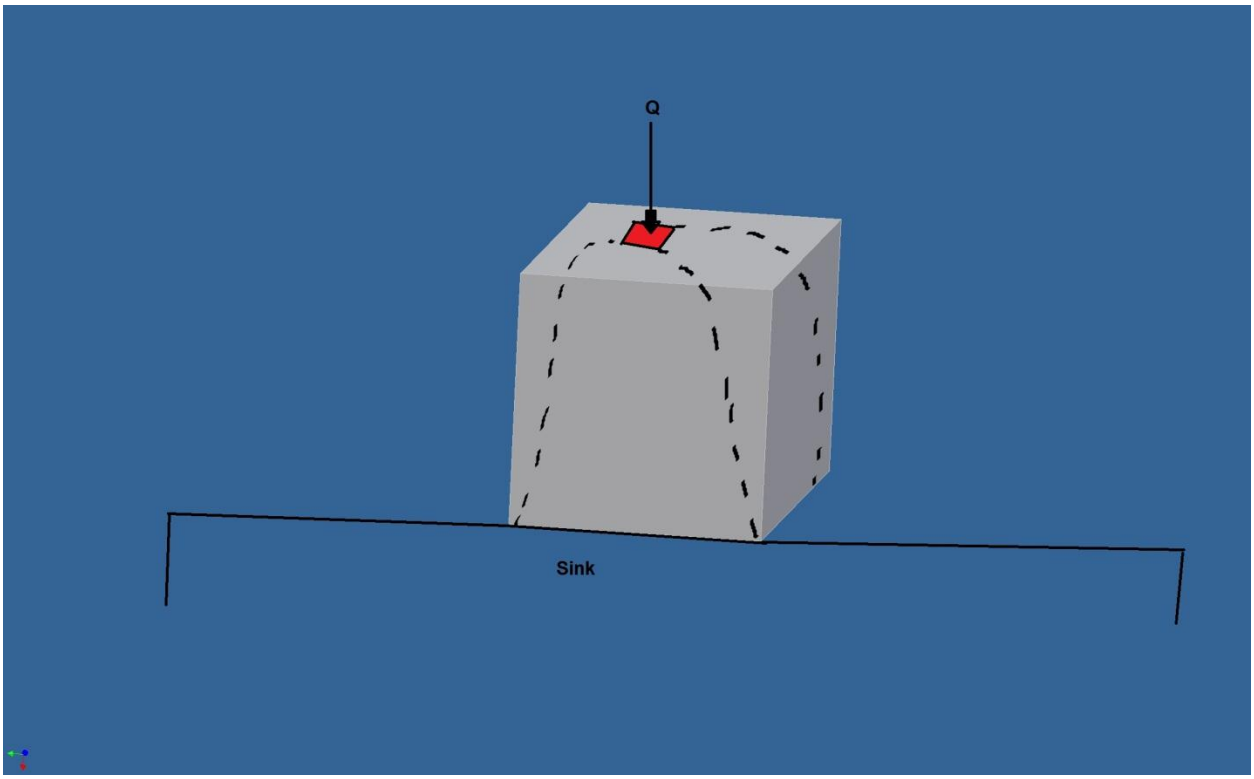

Figure 7-2: Spreading heat flow

Determining heat flow in a FET structure is much more complex, as shown in Figure 7-3 and involves both columnar and spreading types of heat flow. Ways to determine the heat signature and thermal resistance require one of the following methods [12]:

1. Solving three dimensional partial differential equations.
2. Numerical solution of the partial differential equations.
3. Approximate analytical methods.

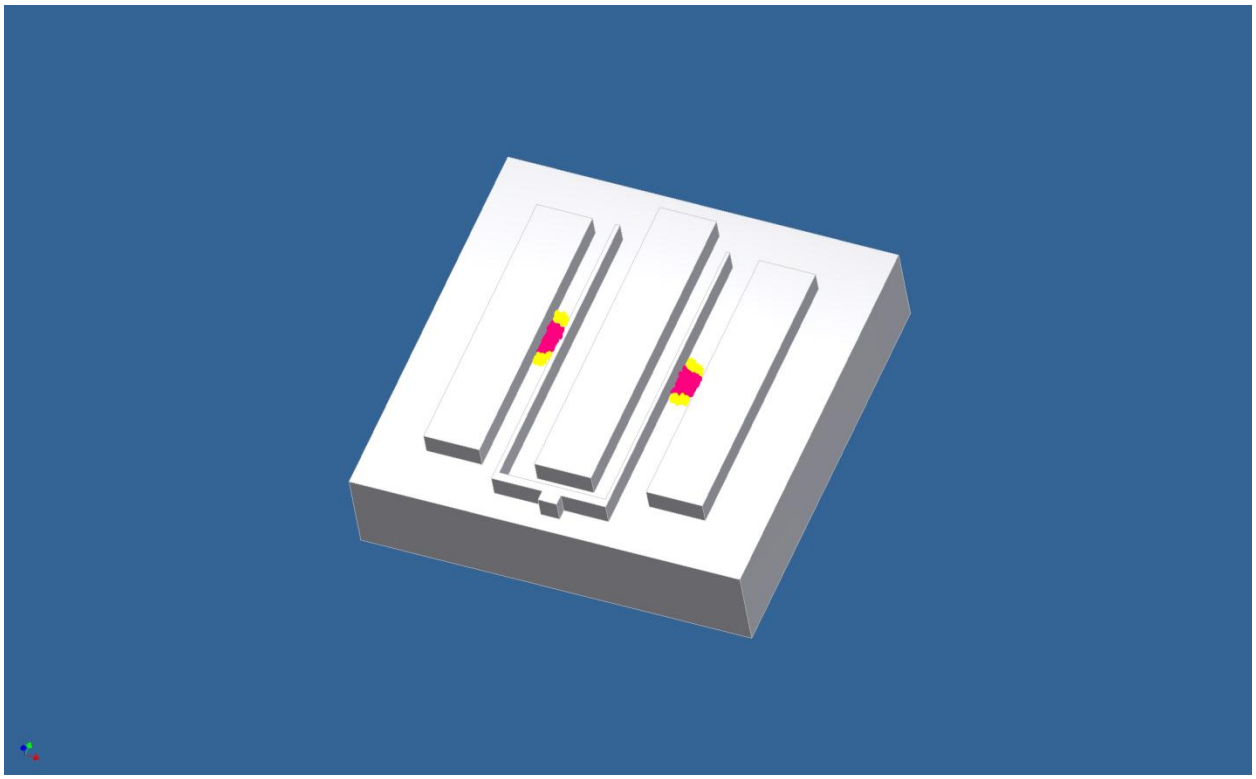

Figure 7-3: FET heat profile structure

7.2 Failure Mechanisms and Junction Temperature

The design of a MMIC is not complete without performing a thermal analysis of the die to determine if the device will function normally over some period of time and under some set of operating conditions. Depending on the application that the die are used in this can be of paramount importance especially if the components are to be used in military, aviation or space circuits where the requirements for predicted life might be 100 years or more. For these high reliability applications the cost of the components come at a steep premium because of the requirement to do burn-in and extended life tests.

Semiconductor die must be used according to the design intent or the device may be degraded or fail much sooner than it would normally have. This is the case when peripheral devices or systems around the device fail such as a cooling system or an improperly filtered or regulated power supply. The designer has no control over situations such as these.

Another failure class the designer has no control over arises from problems in the manufacturing process that may include such things as poor wire bond connections, cracked or chipped die, poor bond pad areas or week connecting metal, contamination and electrostatic discharge. These types of failures can be minimized by prescreening the MCM (Multi-chip Module) assembly by conducting burn in cycles under bias conditions that could include temperature cycling and vibration. Caution should be used though as burn in tests do not guarantee long life and devices exposed to too high of a temperature for too long a period could have their useful life reduced [14].

Temperature activated changes may occur after many hours use and include FET contact degradation, metal migration, and changes to the channel under the gate [12]. Temperature activated change is defined by the reaction rate shown in (7.4)

$$RR = A\, exp\left(\frac{-E_a}{kT}\right) \tag{7.4}$$

Where A is a constant, E_a is the activation energy in electron volts, k is Boltzmann's constant and T is the temperature in Kelvin. The activation energy, E_a, indicates the ease of which a reaction is effected by temperature. A low activation energy indicates relatively short life devices where a high activation energy indicates a long life device. Devices with activation energies less than $1eV$ are considered "short" life devices [12].

Chapter 8 - **Design of a pulse modulated 1-Watt S band Power Amplifier**

8.1 Prior Art

The lions share of the work that exists for pulsed amplifiers in the S-band region involves high power amplification that would be typically used in applications such as radar systems with the goal of generating hundreds of watts of RF pulsed power with pulse widths in the microsecond range. Often this work is designed to replace vacuum tube circuits for increased reliability and maintainability [16]. This is illustrated by Bulent Sen, Mehmet Kayhan, Hakan Boran and Necati Bilgin and many others.

The application for this design requires a S-band MMIC (Microwave Monolithic Integrated Circuit) operating at low RF power, 1 -2 watts and switching speeds as fast as ten nanoseconds with rise and fall times in the single digit nanosecond range. An additional requirement is for increased on- off isolation of > 35 dB.

8.2 Design Challenges

The 1 watt pulse modulated S-band amplifier was designed in a popular GaN HEMT process and measures 2800 um x 2800 um. The initial design challenge comes with matching the input and output of the device under pulsed conditions. The optimum match for a specific parameter, such as gain, power output, input return loss and efficiency changes under pulsed conditions. The simulator only performs load and source pull measurements under CW conditions so the matched obtained may not be the best. A separate 4 gate 150 um device was included in the die design in the event that a pulsed load pull may be required.

The narrow modulation pulse width of 10 nanoseconds and fast rise and fall times present both a design challenge and a measurement challenge. The best pulsed power meters are generally only good to a pulse width of ten nanoseconds.

8.3 Design Specifications

The design specifications for the 1W GaN pulse modulated amplifier are detailed in Table 8-1.

Logic Level Low	-4.5 V± 0.5V
Logic Level High	0 V ± 0.1 V
Rise Time (10-90% det. RF mag.)	2.5 ns maximum
Fall Time (90-10% det. RF mag.)	2.5 ns maximum
Pulse Width	10 to 40 ns
Return Loss	>15 dB
Output power @ 1dB compression	1-2 W
Power Flatness	1dB
Harmonic Power level	23dBc
Band of operation	S-band
Power Added Efficiency (PAE)	20% min
Channel Temperature	<180°

Table 8-1: GaN 1W pulse modulated amplifier design specifications

8.4 Class of Operation

The RF transistor required for this application would have to be able to supply a minimum of 1W of RF to the load from a minimum DC power supply voltage of 24V. Since this application requires extremely fast pulse switching times and rise and fall times it is necessary to not pick a transistor that is too large for the application as it would incur greater parasitic capacitances and degrade the performance of the amplifier. An approximate expression for the size needed utilizing I_{dss} and V_{dg} is shown in (8.1).

$$P_{RF} = \frac{I_{dss} * V_{dg}}{8} \tag{8.1}$$

By performing a DCIV simulation on the 150 um by 4 gate device in the design kit the I_{dss}value is found to be 409 mA as shown in Figure 8.1. The value for V_{dg} will vary slightly according to the class of operation but assuming a value of -2.2V for class AB operation the transistor should supply 1.33W of RF power. This value is only approximate but gives a good starting point for the large signal simulations that follow.

As previously stated in chapter 2, class AB is a compromise between Class A mode of operation and Class B mode. The output is zero for part of the input sinusoid but less than one-half of the sinusoid. Using this device in the class AB mode sets the quiescent current at approximately 98.6 mA. The amplifier is running in this class so that an improvement in efficiency over class A may be obtained. A current mode amplifier is required for this application because of the fast switching speeds involved. The amplifier must be turned off quite abruptly and this would not be possible in a switch mode operation where the energy of resonant tank circuits would have to be dissipated in extremely short intervals.

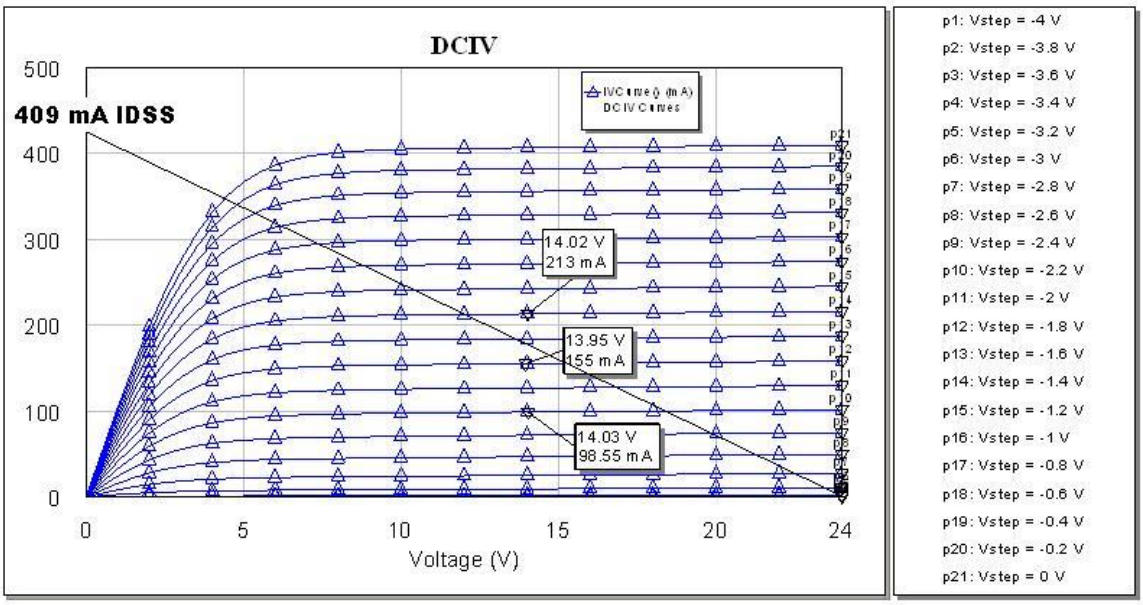

Figure 8-1: DCIV Bias point for the 600um transistor

8.5 Modulator Design

The modulator is designed to supply 24-28V of pulsed DC to the drain of the 600 um RF amplifier transistor at pulse widths of 10 ns and rise and fall rates of 2 ns. This is accomplished in the following manner (refer to Figure 8-2):

1. Transistor X9 receives a transmit enable pulse whose levels are 0 and -5V respectively. This transistor is a custom designed 1 gate by 50 um total periphery device. This device does not exist in the design kit. It is purposely designed to be as small as possible so as to reduce the gate to source capacitance as small as possible for high switching speed performance.
2. Upon application of a -5V logic level the device is in cutoff and its drain voltage rises to the DC level of 24-28V.
3. A high voltage level at X9 is applied to the gate of X7. Since its source is at the DC level of 24-28V the difference in voltage between gate to source is zero thus turning on the switch and supplying drain voltage to the RF amplifier transistor X36.
4. Transistor X18 is enabled between on pulses to remove any voltage present between pulses due to parasitic capacitance of X7 or other stray capacitances that may be present on this node.
5. When the transmit enable pulse is 0V transistor X9 conducts dropping the voltage on R1 close to zero volts. This voltage is impressed on the gate of X7 negatively biasing the transistor well past it's cutoff point.
6. Transistor X7 is cutoff removing the 24-28V bias from RF amplifier transistor X36.
7. Transistor X18 conducts bringing any residue bias present to 0 V.

Figure 8-3 thru 8-4 show the transient switching voltage present at RF transistor X36 and the switched RF output level present at the load respectively.

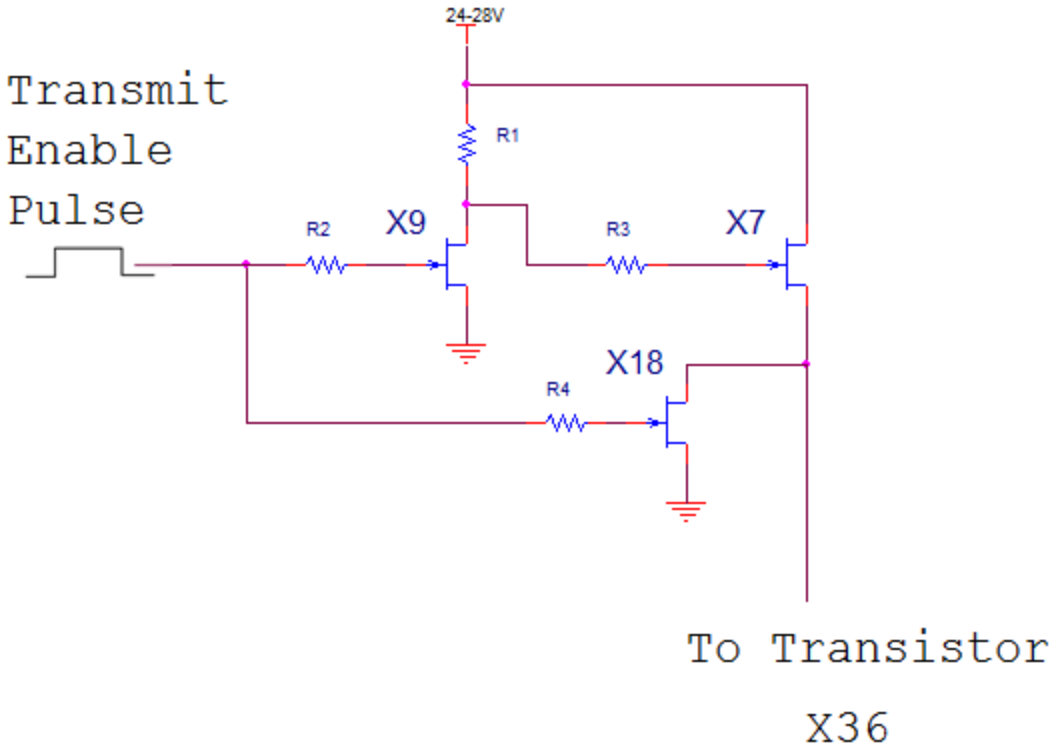

Figure 8-2: Simplified Pulse Modulator schematic

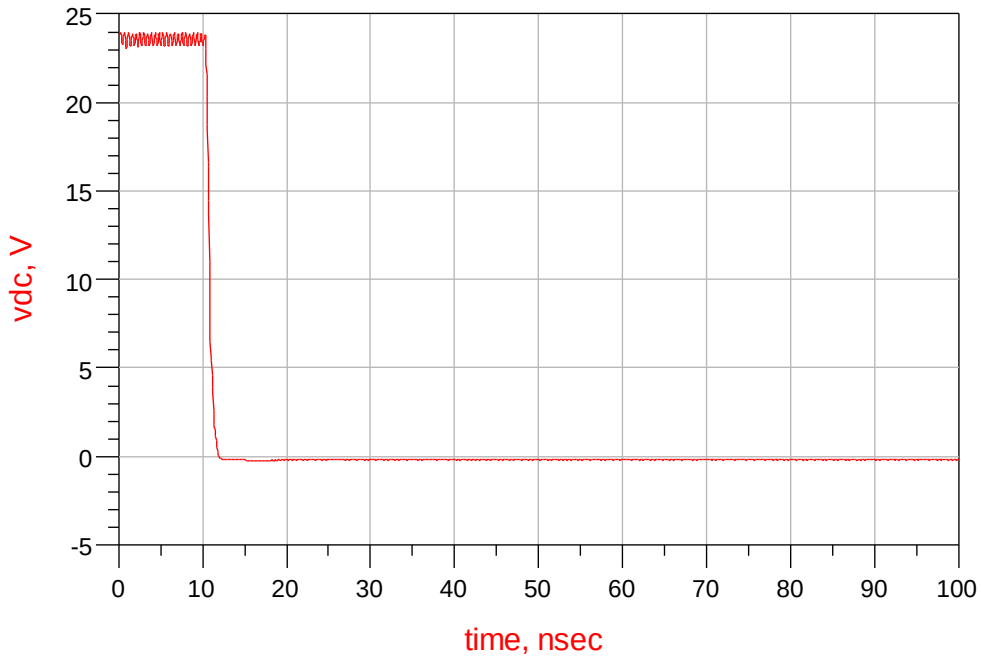

Figure 8-3: Switched DC to RF amplifier transistor X36

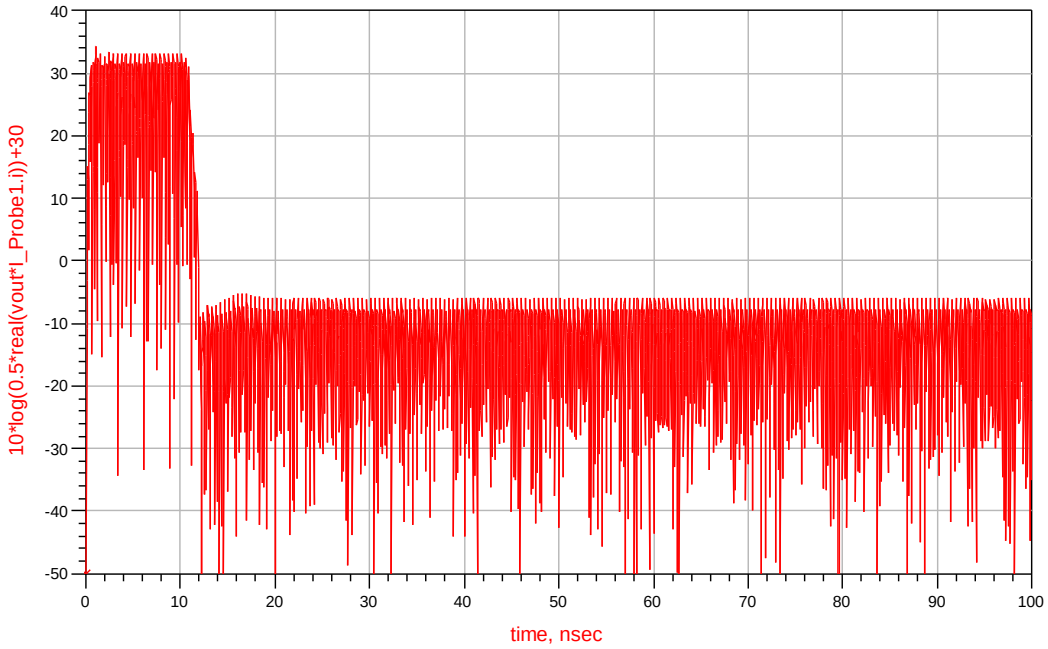

Figure 8-4: Switched RF at amplifier load

8.6 Blanking Switch

The blanking switch is designed to provide a RF short at the input of the amplifier at time intervals in between the pulse modulation. This is enabled at the precise time that X21 in the modulator is enabled. The purpose of this switch is to provide the highest level of on/off isolation possible by creating a reflective load at the input during the pulse off time.

8.7 Matching Network Design

In the preceding chapters the matching networks were excluded from the discussion to simply the stability concepts. It was assumed in those cases that the matching network was in place, functioning normally and not negatively impacting the circuit stability. In most all cases a matching network will be required to transform the impedance presented at the input or output of the amplifier, in many cases this is 50 + j0 ohms, to the conjugate impedance presented by the transistor so that transistor sees maximum excursion of current and voltage and thus maximum power transfer occurs. Ideally this would indicate that no reflection was occurring on the input or output.

Before the matching networks can be designed the amplifier must be initially stabilized. It is impossible to simultaneously match the input and the output if the transistor is not stabilized [4]. In volumes of information on this subject the common method is to apply the stability factor K and auxiliary condition 1 . The K and $B1$ stability factor analysis is quick and lends itself well for optimization but for reasons outlined in chapter 4 this should be followed by a NDF analysis to confirm stability.

The initial circuit without the stability network is shown in figure 8-5. The transistor is connected by source and load pull tuners to the input and output respectively. This is done to bias the gate and the drain to the proper operating point. These tuners can provide any impedance on the Smith chart. A simulation is run and the plot of the K and $B1$ stability factor is shown in figure 8-7. The plot indicates unstable operation to almost 10 GHz.

In order to stabilize the circuit a network was added consisting of C1, 14 pF and R1, 1400 ohms as shown in figure 8-6. These values where obtained by performing a optimization with the goal being for $K > 1$ and $B1 > 0$. The K/B1 analysis was initially run due to the speed at which the analysis and optimization can be performed. Following this initial check additional stability measures were run to verify stability, these include the NDF and Nyquist analysis. Figure 8-7 shows both the pre and post stabilization results. After the network is installed the circuit shows stability to 20 GHz.

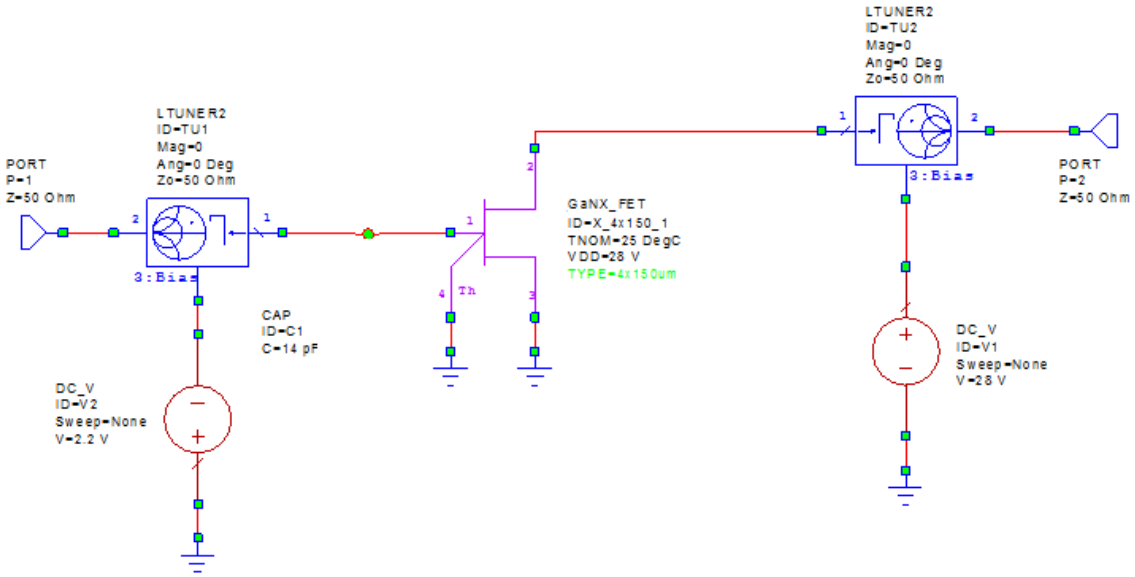

Figure 8-5: Initial Stability Check

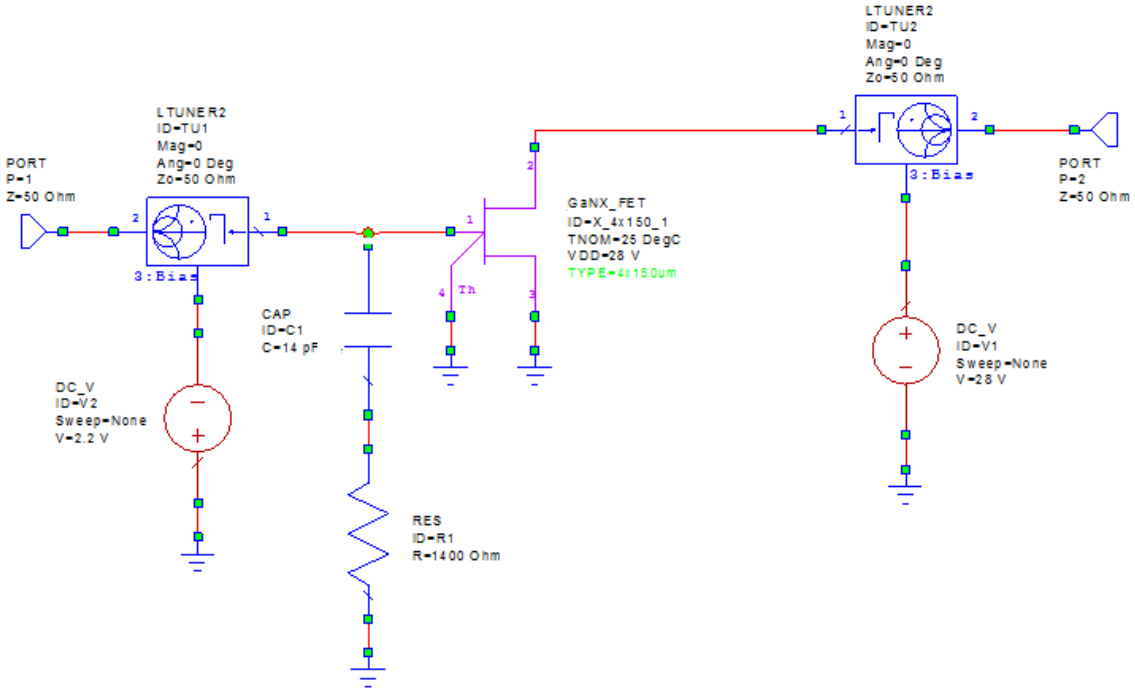

Figure 8-6: Stability network C1 & R1 added

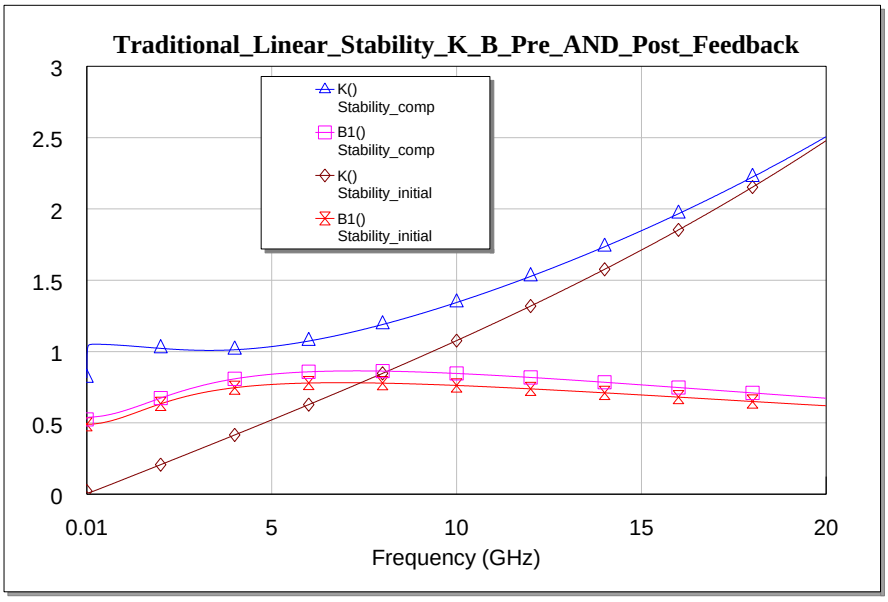

Figure 8-7: Initial and post stability simulation plot

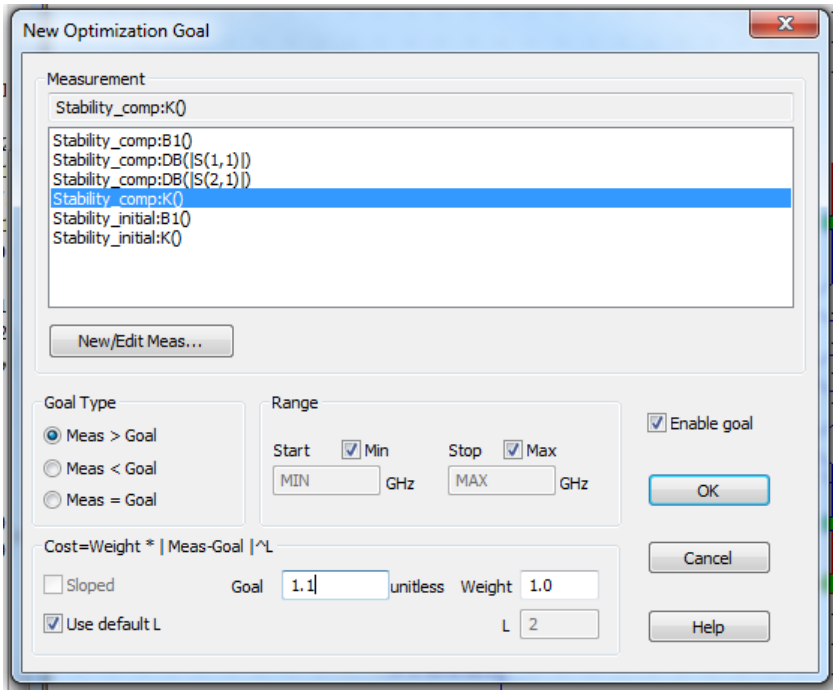

Figure 8-8: Stability optimization simulation

8.7.1 Load Pull

Once the transistor is stabilized the optimum source and load impedances can be found. One way of doing this is with source and load pull contours. Source and Load pull contours represent the impedance boundaries on the Smith chart necessary to obtain the desired performance parameter [4]. These parameters can include gain, power, compression, linearity, efficiency and return loss to name a few.

To develop the contours a load pull simulation is run as shown in Figure 8-9. Many commercial microwave software packages including ADS and Microwave Office will generate the contours. The simulation in this instance is run for $S21$ and $S11$ and indicate that the optimum values for the respective measurements are in two different hemispheres of the Smith chart. In this situation selecting the contour inside p1 indicates a respectable gain of 16.74 dB and a $S11$ value of -21.18 dB, the point selected has the reflection coefficient magnitude of

0.3413 and angle -32.09 degrees. Matching to the complex conjugate of magnitude 0.3413 and angle 32.09 degrees is shown in Figure 8-10.

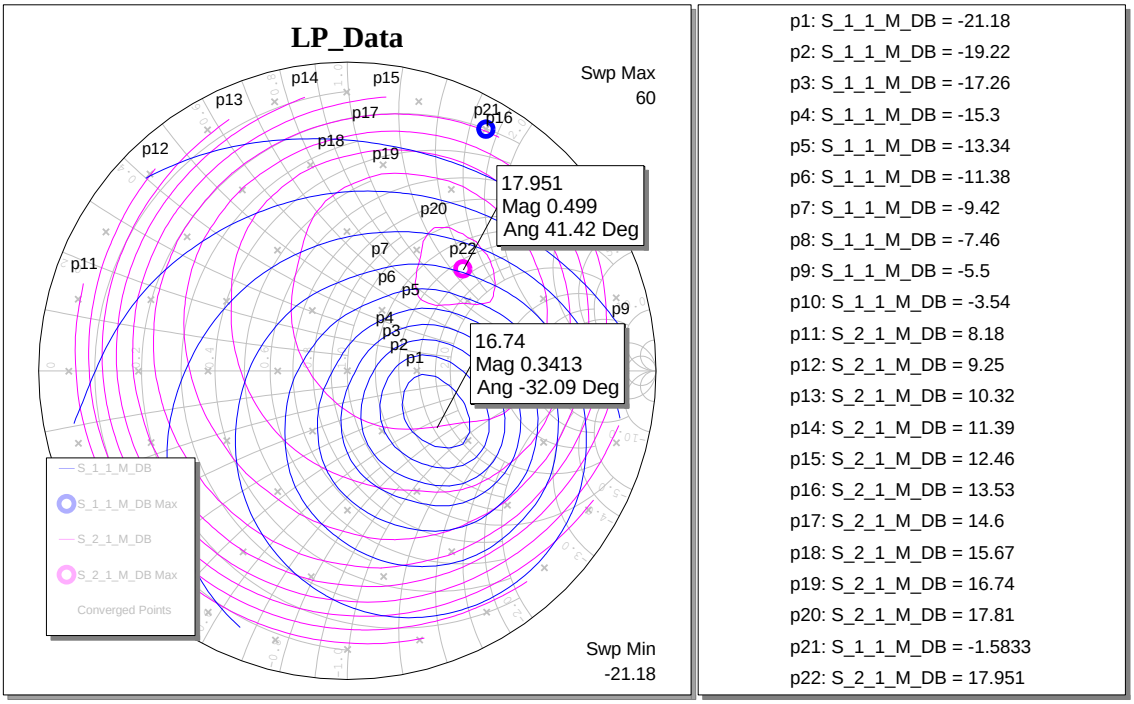

Figure 8-9: Load pull contours for the 1W GaN Pulse modulated amplifier

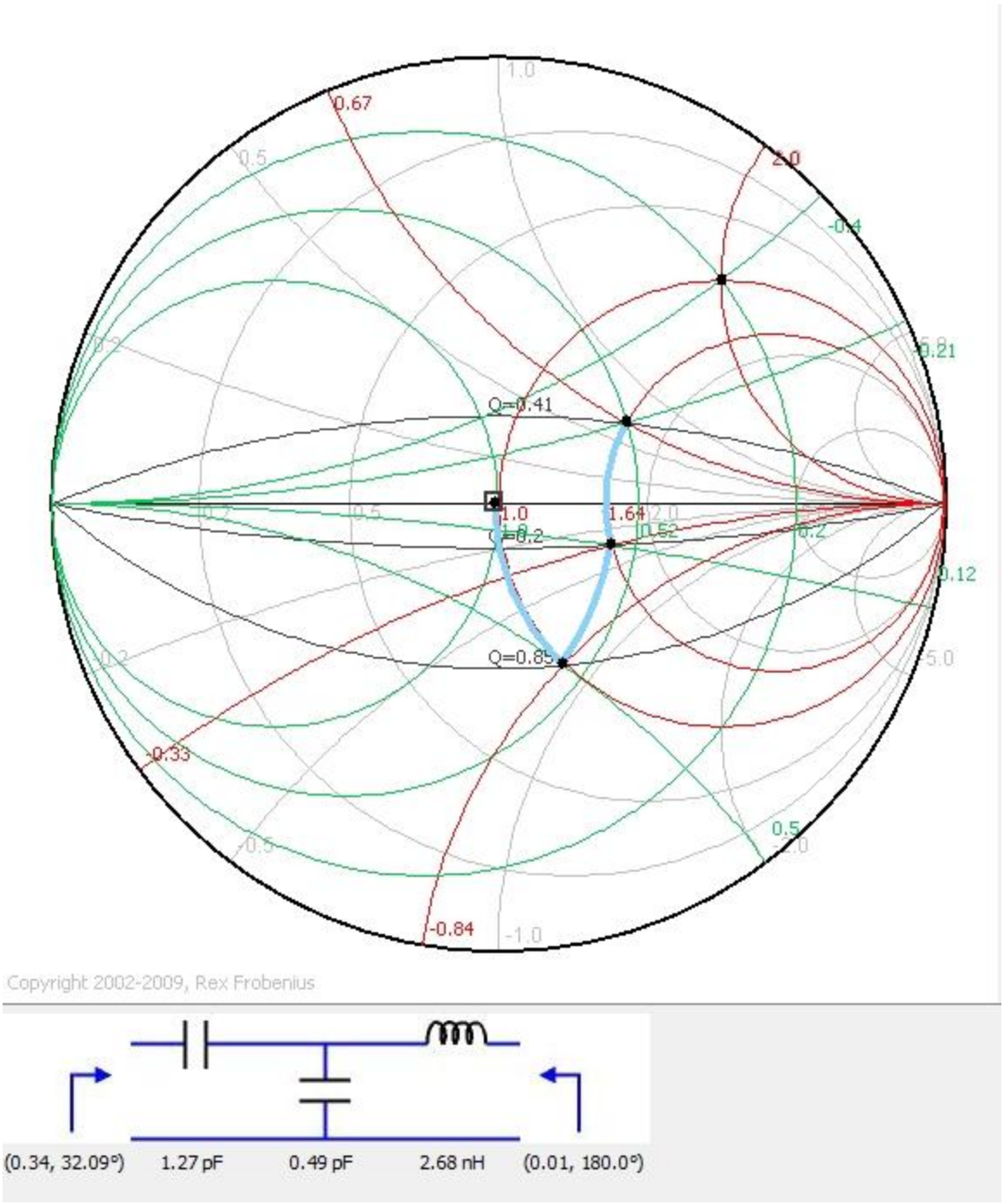

Figure 8-10: Conjugate Load Match

8.7.2 Source Pull

With the output network now synthesized the source can be pulled in the same manner as the output was. In this case the results show $S21$ and $S11$ contours close to each other as indicated in Figure 8-11. The point selected has the reflection coefficient magnitude of 0.6718 and angle 80.84 degrees which is a contour showing a gain of 16.64 and $S11$ of -22.68 dB. Matching to the complex conjugate, 0.6718 and angle -80.84 degrees the synthesized network is shown in Figure 8-12.

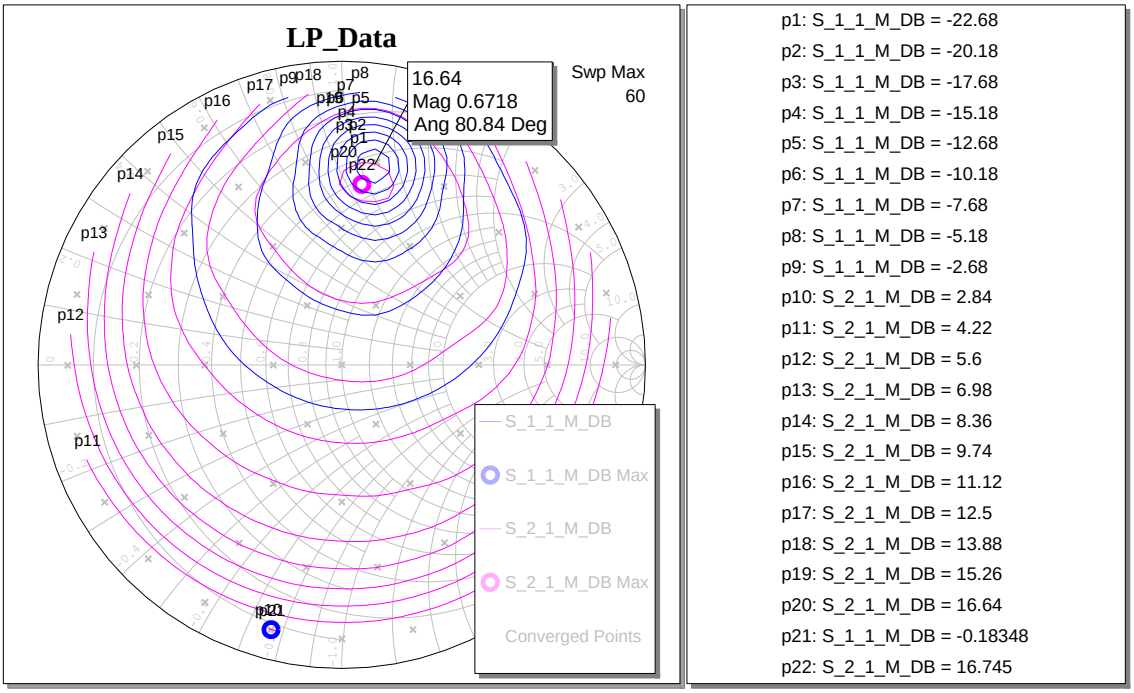

Figure 8-11: Source pull

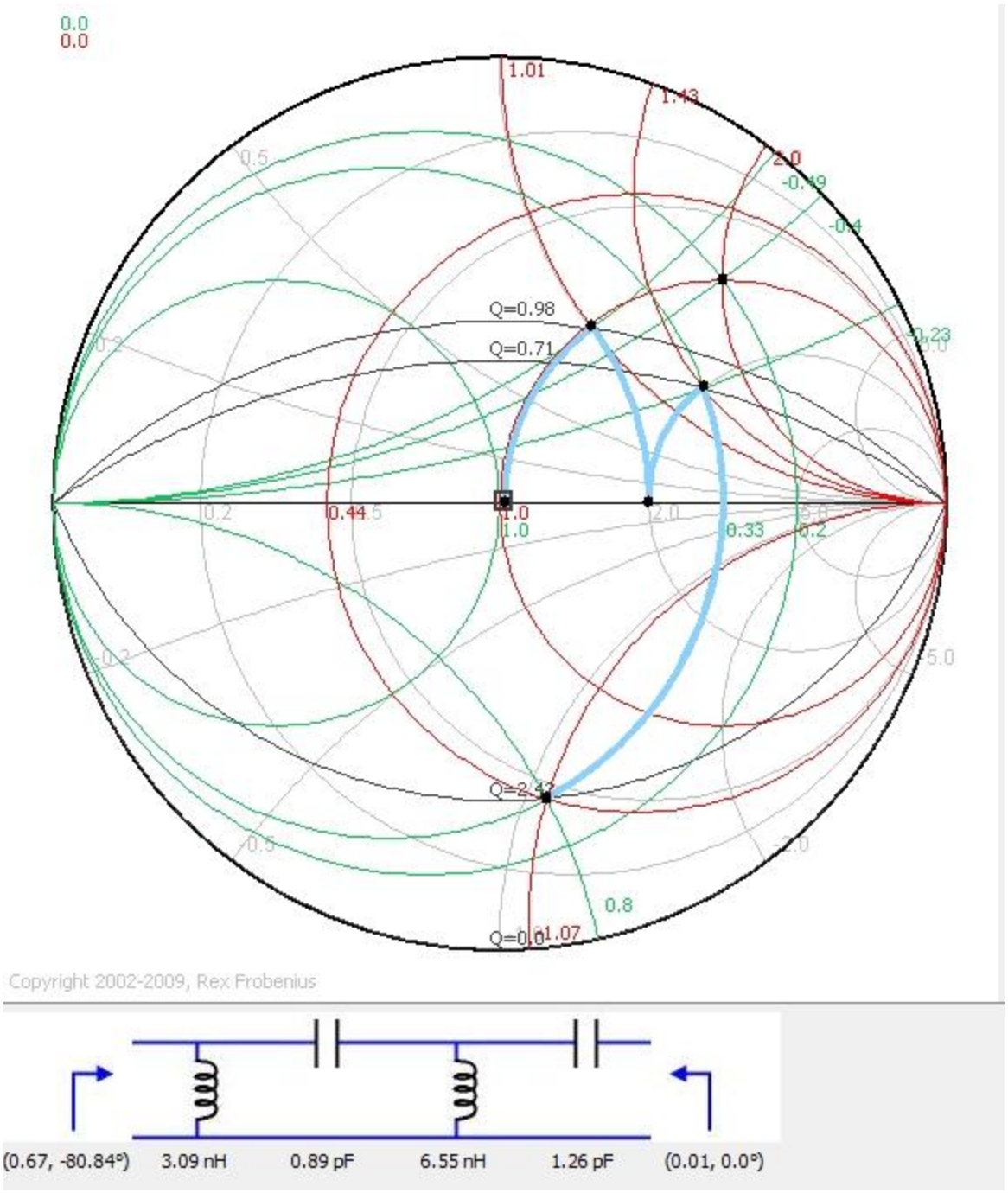

Figure 8-12: Conjugate source match

The complete amplifier with the matching networks added is shown in Figure 8-13. The passive components shown are ideal components and must be replaced with realistic components. For example the inductors that can be fabricated on GaN die typically are limited to <10-15 nH with Q < 20-25. The MRINDSB2 rectangular inductor model performs and analysis of the self and mutual inductances, capacitances and resistances between parallel segments. This is based on a quasi-static model of an arbitrary number of edge coupled microstrip lines [9]. In addition to the inductors the capacitors are replaced with the specific type used in the circuit, in this kit three types are called out depending on the capacitance per unit area and voltage breakdown. Lastly, the via, bond pad and wire bond models should be included in the complete model. The transmission line connections between the components have been omitted for readability.

The final step in the process is to perform an optimization of the circuit using the realistic lumped element models now incorporated to the optimizer goals listed in Table 8-9. Once the optimizer is finished the circuit values have changed, the most notable is of which is L4 which went to a very low value. After removing L4 and optimizing again it was found that it could be removed from the design without degrading any of the performance criteria. The complete design is shown in Figure 8-14 with the S-parameter plots for $S_{11}$and $S_{22}$and the output power plots shown in Figure 8-15 and Figure 8-16 respectively.

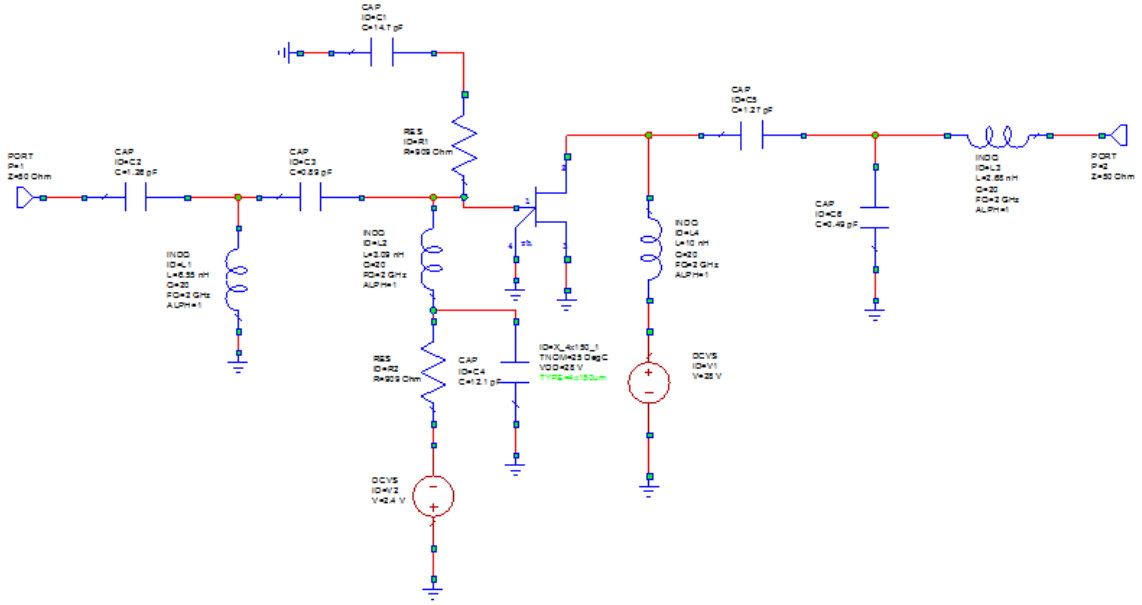

Figure 8-13: 1W amp with matching networks pre-optimization

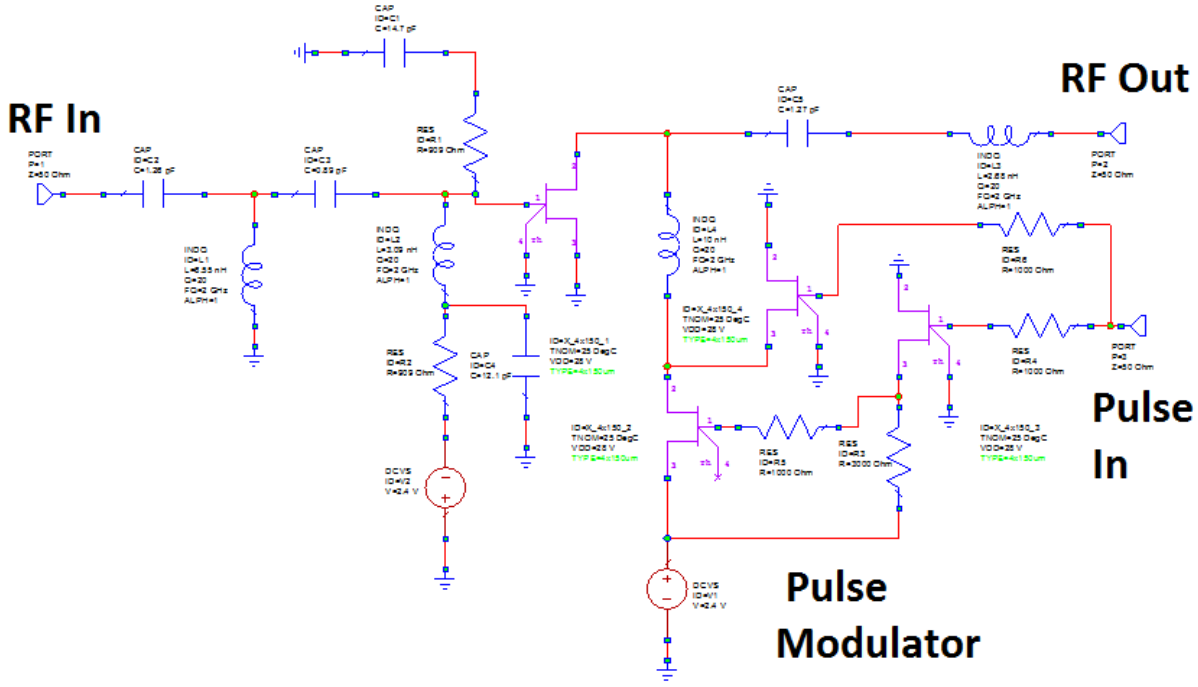

Figure 8-14: 1W amp with matching networks post-optimization

Measurement	Goal
S_{11}	< -15 dB
S_{21}	> 10 dBm
P_o	> 30 dBm
K	> 1.1
$B1$	> 0

Table 8-2: Optimization Goals for complete 1W amp circuit

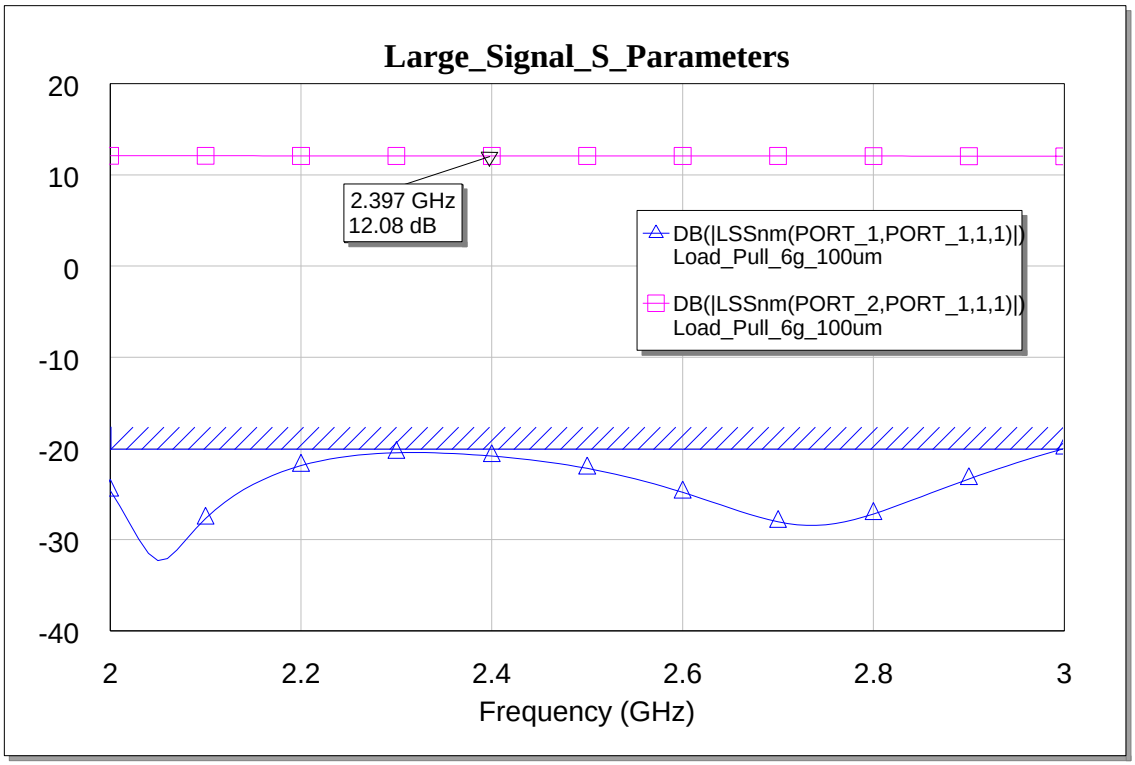

Figure 8-15: S-parameters S11 & S21 for complete 1W amp circuit

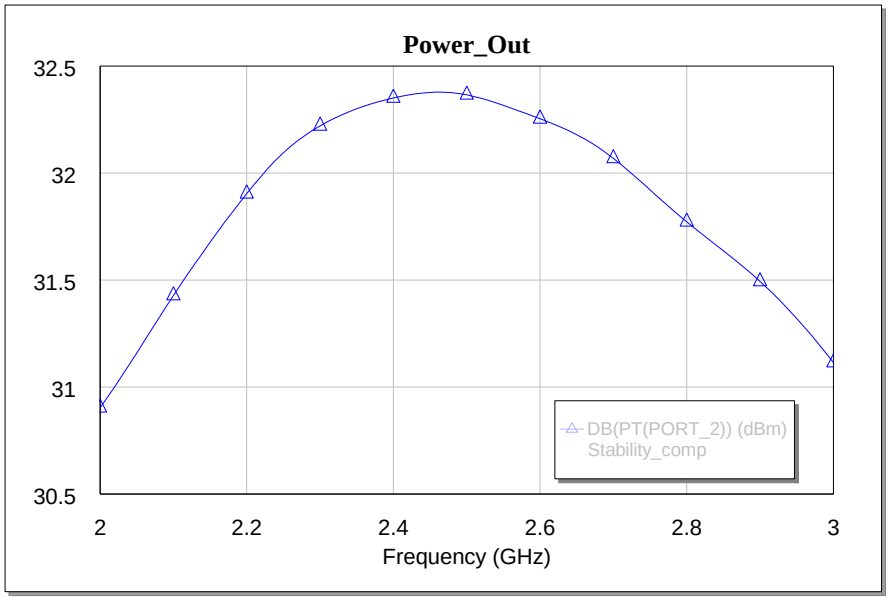

Figure 8-16: Power Output for complete amp circuit

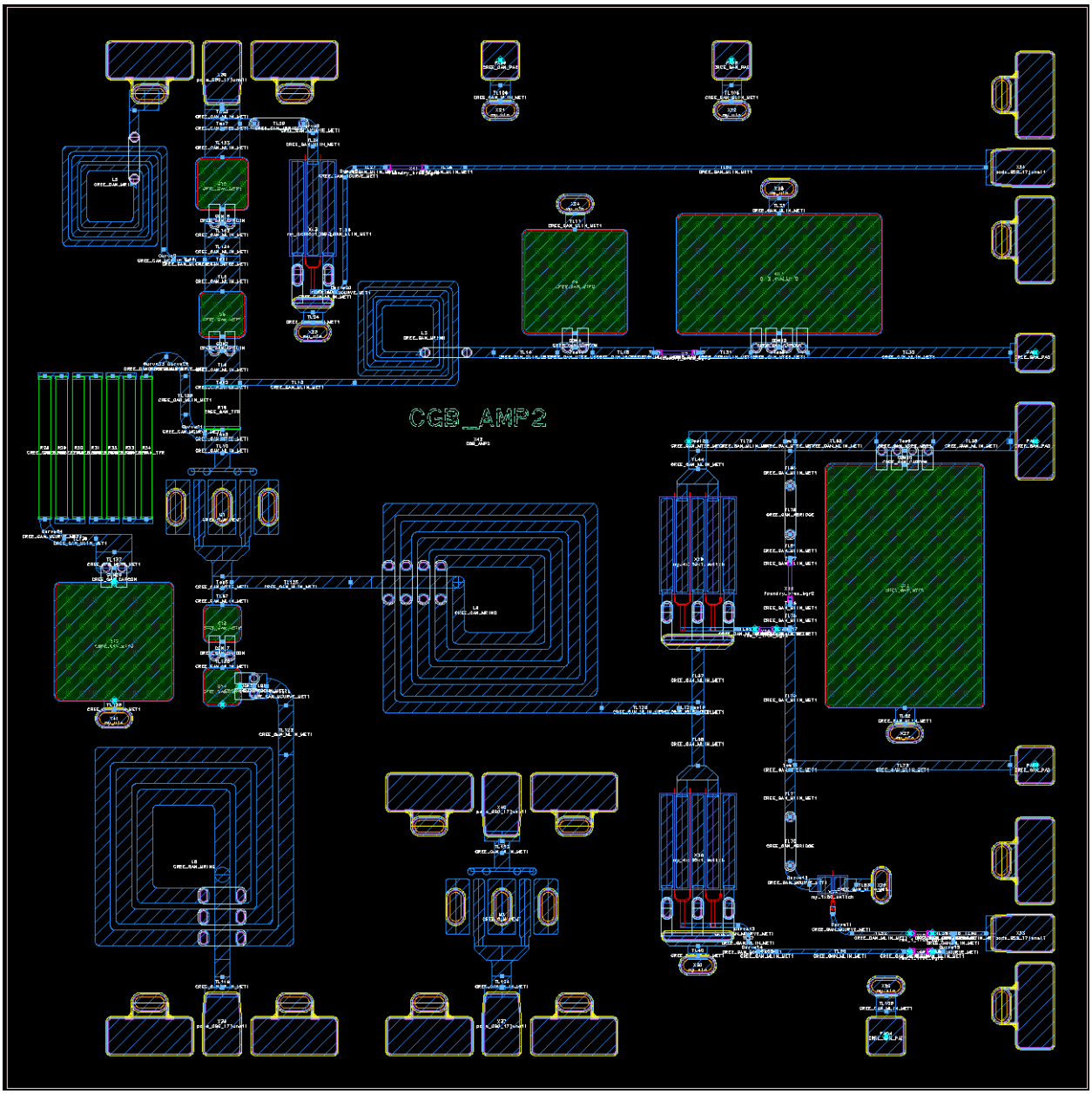

Figure 8-17: Layout of the GaN 1W pulse modulated amplifier

8.8 Stability Analysis

As this thesis has discussed there are many mechanisms that can contribute to or cause oscillations or instabilities in microwave circuits. Some can be severe such as in a steady state oscillations or others can be manifested as spectrum spurs or chaos effects in selected bands. Modern simulation packages have many tools to help in the diagnosis of circuit instabilities and should be used under the constraints outlined in chapters 4 and 5.

8.8.1 NDF Analysis

The NDF analysis is the most reliable of the methods analyzed to determine instability. On the Polar plot the trace must not encircle the origin in a clockwise rotation to be stable. If it does there are poles in the right half plane (RHP). Another way of viewing this is to look at the unwrapped phase on a rectangular plot. The NDF analysis was run from 10MHz to 20 GHz and met the conditions for stability as shown in Figures 8-18 and 8-19 respectively.

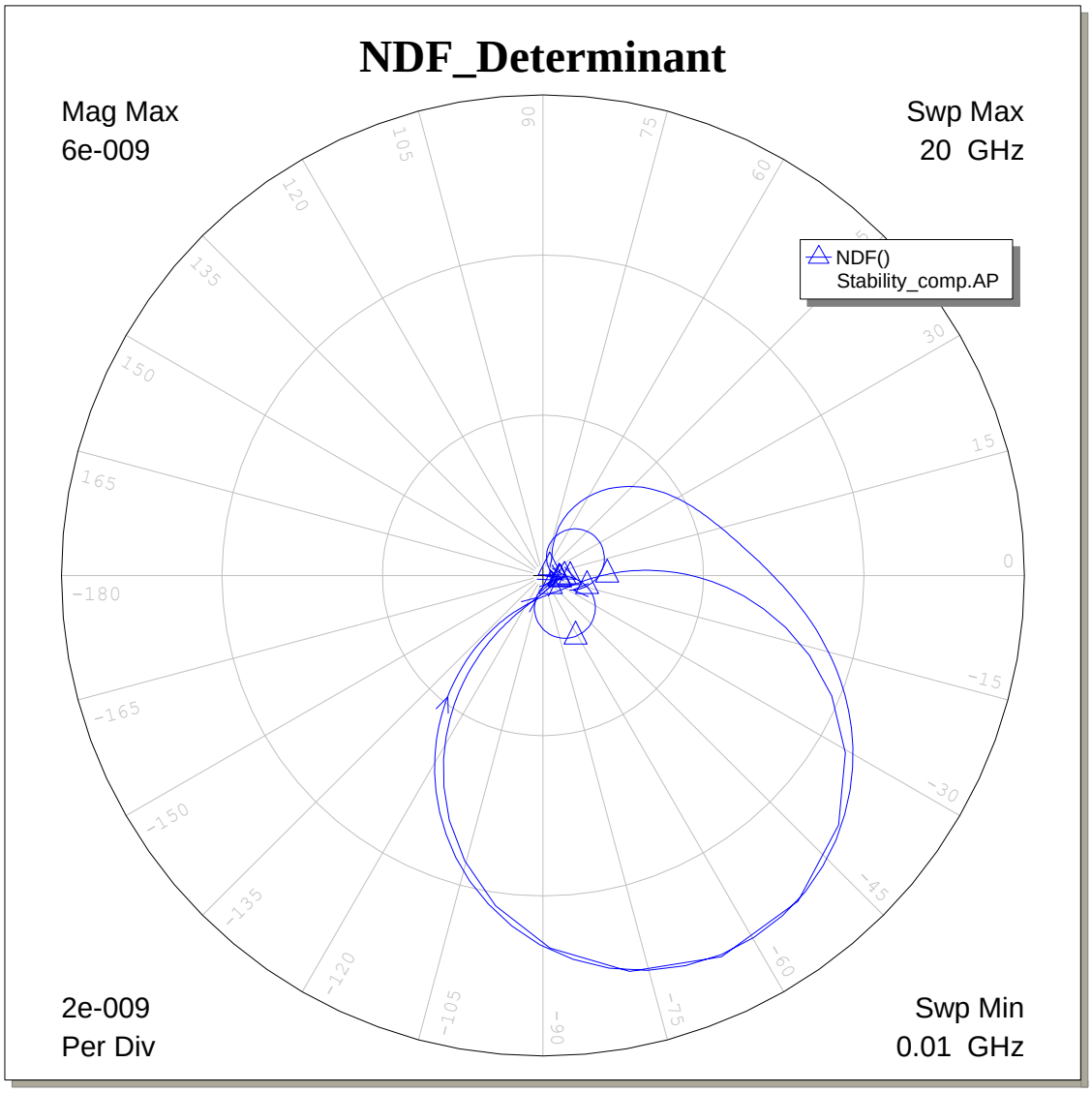

Figure 8-18: NDF Analysis of 1W pulse modulated amplifier

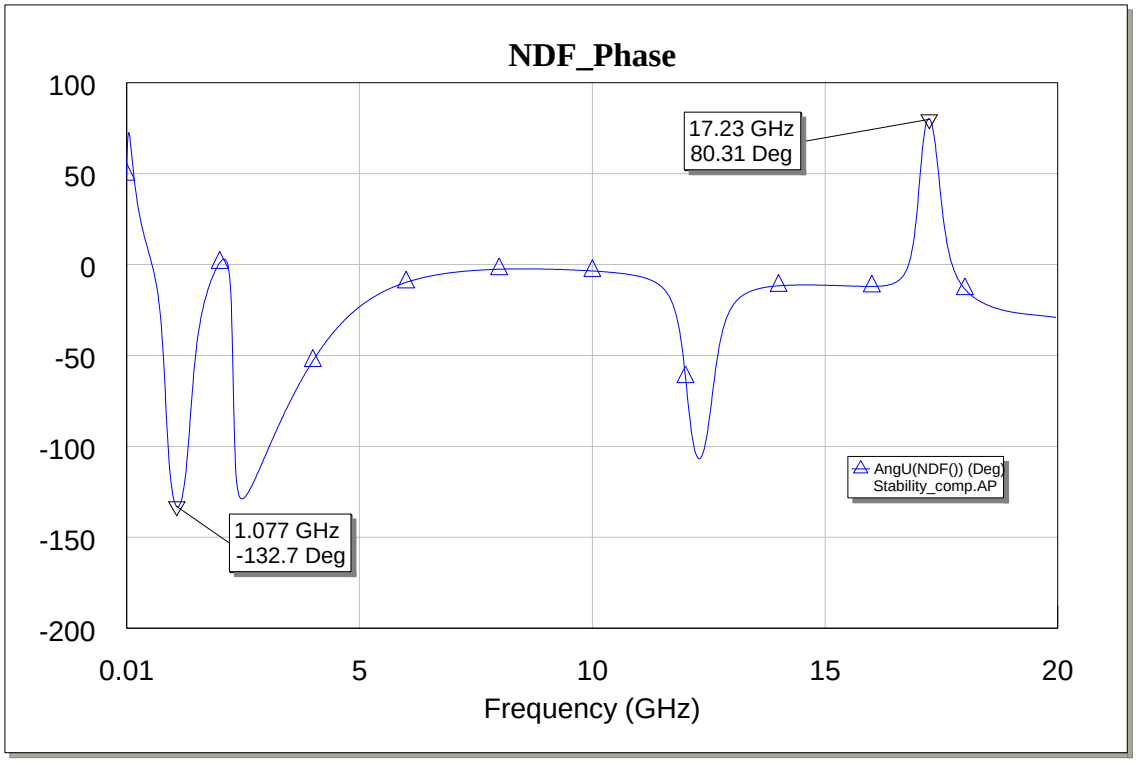

Figure 8-19: NDF phase Analysis of 1W pulse modulated amplifier

8.8.2 Nyquist Analysis

The Nyquist analysis was run from 10MHz to 20 GHz as shown in Figure 8-20. The unstable condition is identified as a clockwise rotation encircling the $-1 + j0$ point. As can be seen the $-1 + j0$ point is not encircled and as so is stable.

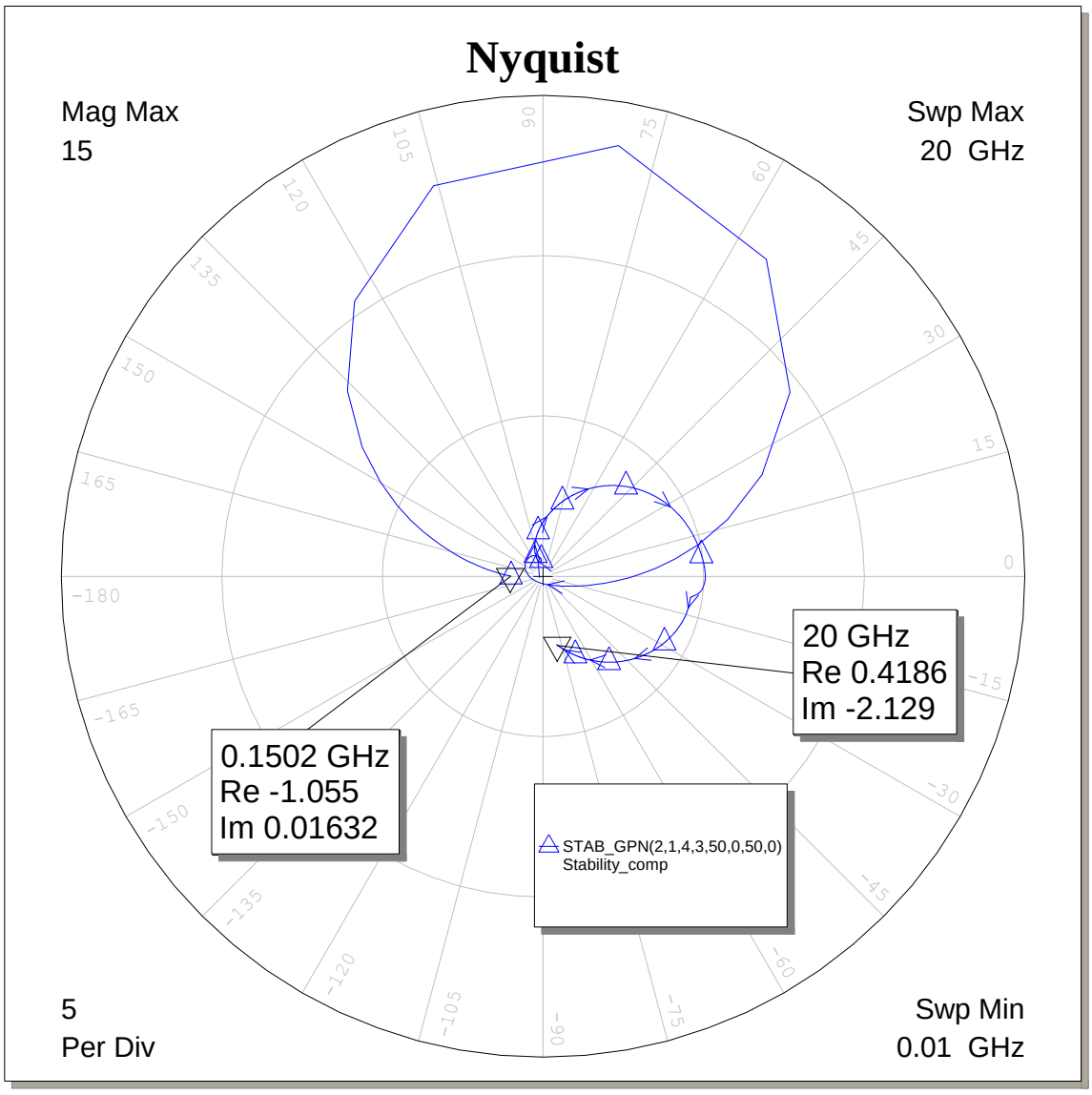

Figure 8-20: Nyquist Analysis of 1W pulse modulated amplifier

8.8.3 K/B1 Analysis

The $K/B1$ analysis is run last. Since stability was guaranteed by the NDF and Nyquist analysis and plots from Figures 8-21 thru 8-23 shows that $K > 1$, and $B_1 > 0$, this now insures that no combination of output load and source loading can cause instability.

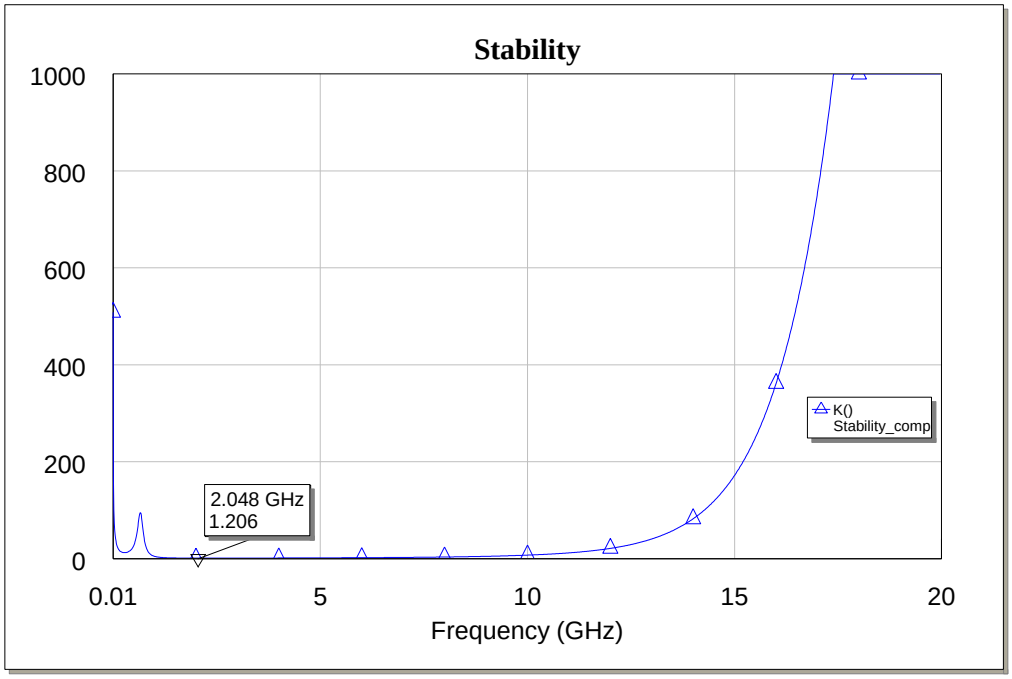

Figure 8-21: K Analysis 1 of 1W pulse modulated amplifier

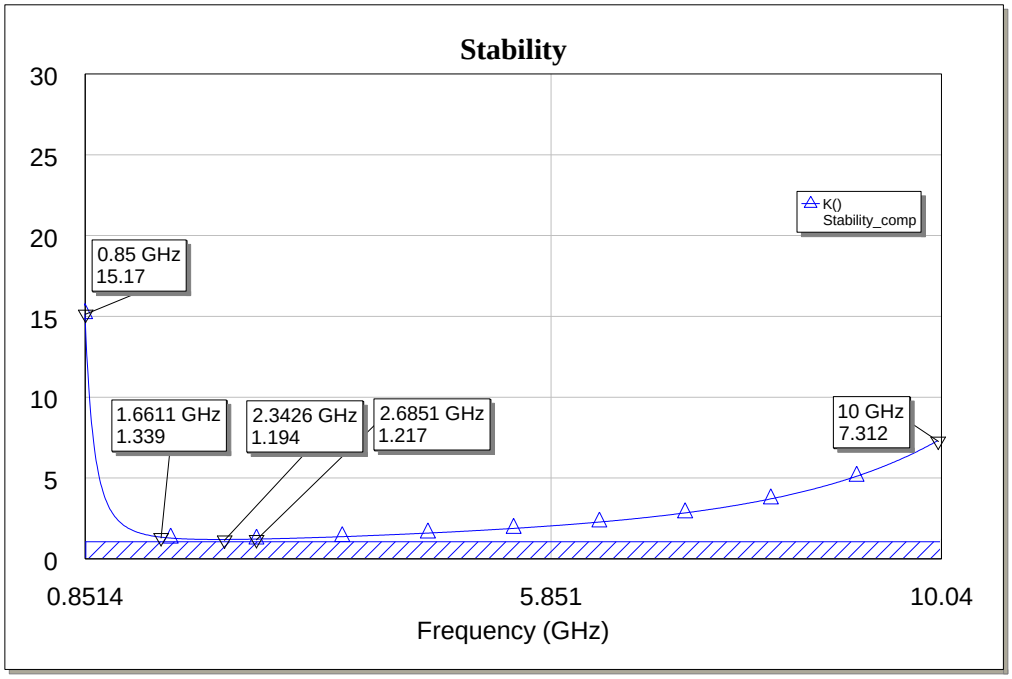

Figure 8-22: K Analysis 2 of 1W pulse modulated amplifier

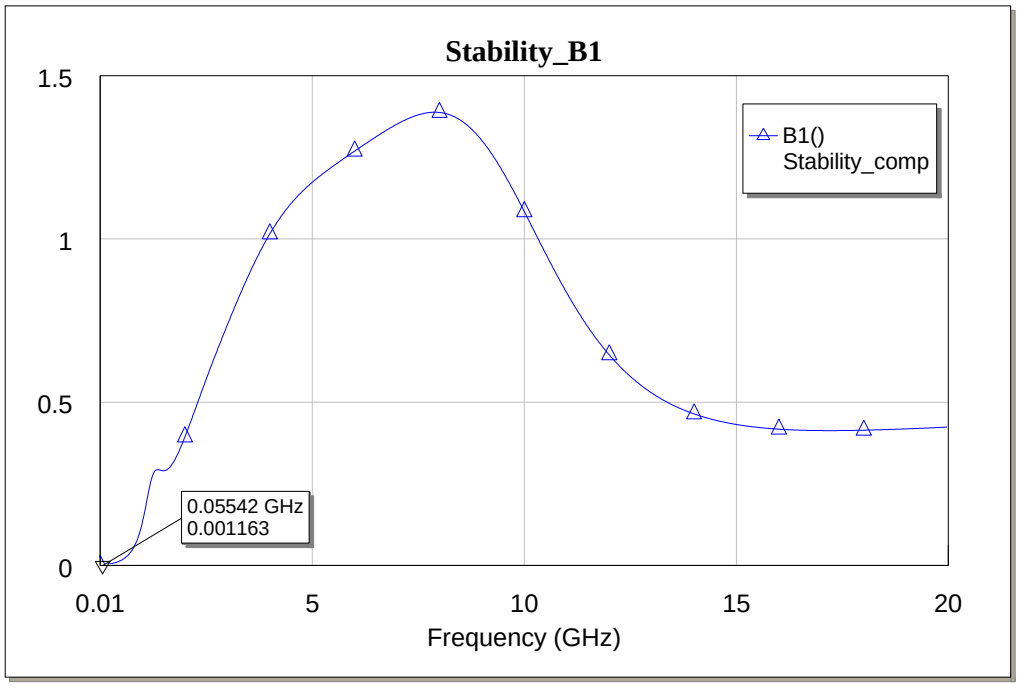

Figure 8-23:B1 Analysis 1 of 1W pulse modulated amplifier

Chapter 9 - **Measurements**

The 1W pulse modulated amplifier was fabricated in a popular 0.25 um Gallium Nitride (GaN) 3MI process and measures 2800 um x 2800 um. It was deposited on a heat spreader into a cavity cut into Rogers TMM10i duroid material and attached to an aluminum plate for heatsinking. The board traces were gold plated and wirebonded to 100um bond pads on the die as shown in Figure 9-1.

The PC board has three SMA connectors used as input RF drive, output RF and input pulse modulation. Two other SMA connectors are possible so that a thru calibration standard required of a TRL (Transmit Reflect Line) calibration can be made. The black molex connector is used for the drain and gate bias and the external surface mount components are used for filtering and bypass.

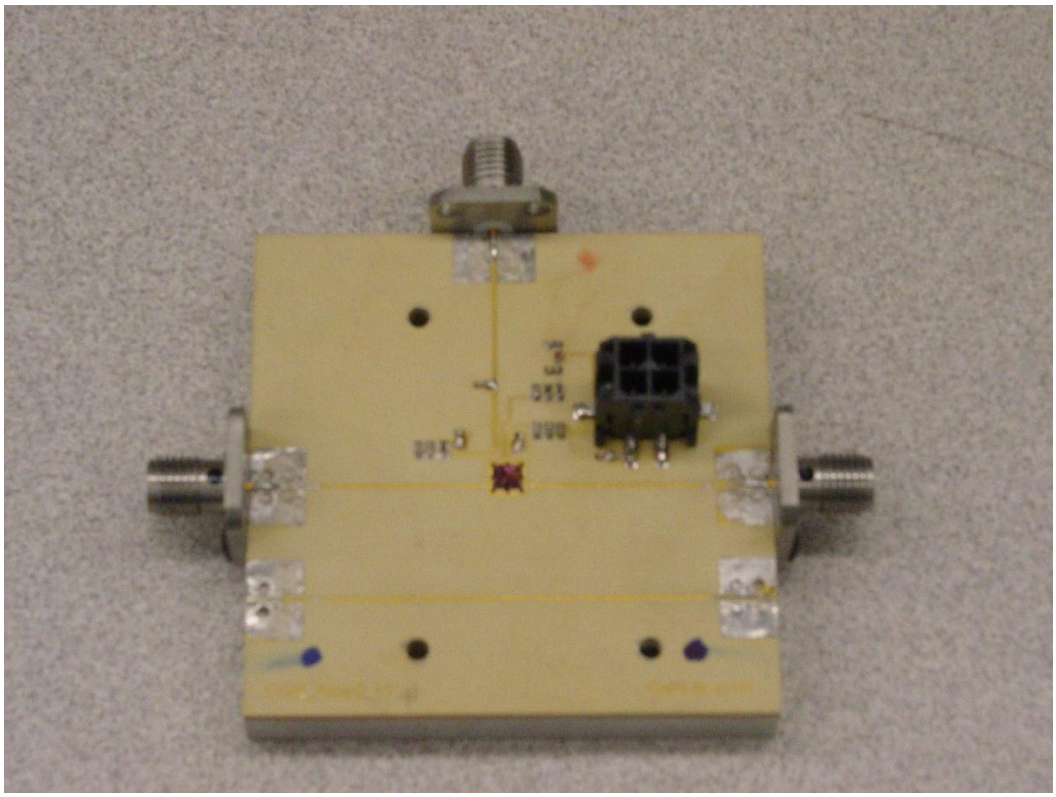

Figure 9-1: 1W S-band amplifier PCB

9.1 Test Bench Setup

The setup for the test bench consists of a microwave generator used to supply S-band continuous wave drive at a nominal level of +24 dBm. The signal is fed through directional coupler, labeled “Dir Coup1” to the RF switch. Directional coupler “Dir Coup1” is used monitor the input CW level so that the generator output does not exceed the maximum power level of the switch.

The switch is used to mimic the operation of a preceding stage and supply pulsed RF at a nominal level of +18dBm to the directional couplers labeled “Dir Coup2” and “Dir Coup3” to the 1W pulse modulated S-band power amplifier. The directional coupler labeled “Dir Comp2” is connected so that the forward power can be measured and fine adjustments made to the amplifier to ensure that the level remains at a nominal +18dBm across the band. The second directional coupler, labeled “Dir Coup3” is used to monitor the reflected power across the band.

The gating pulse labeled “Transmit Enable” is used as a pulse modulation drive for the amplifier and switch and the delay is adjusted so that the pulse arrival occurs simultaneously at both the switch and the 1W power amplifier. The output from the 1W power amplifier is fed to directional coupler “Dir Coup4” and then on to the load.

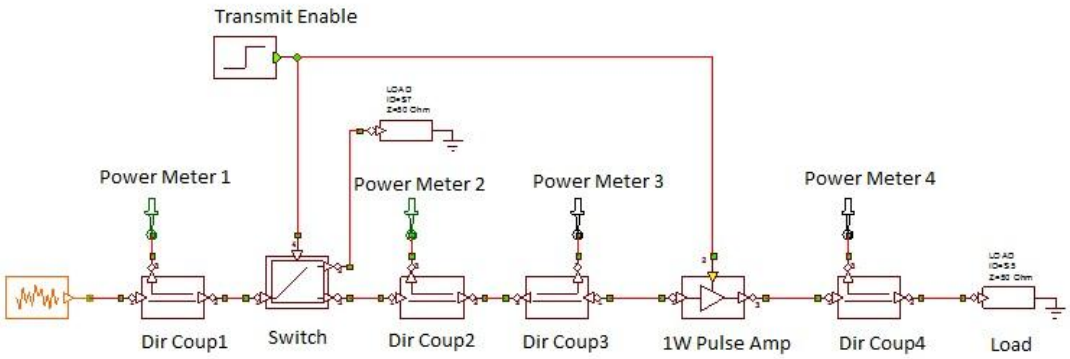

Figure 9-2: Schematic of test bench setup

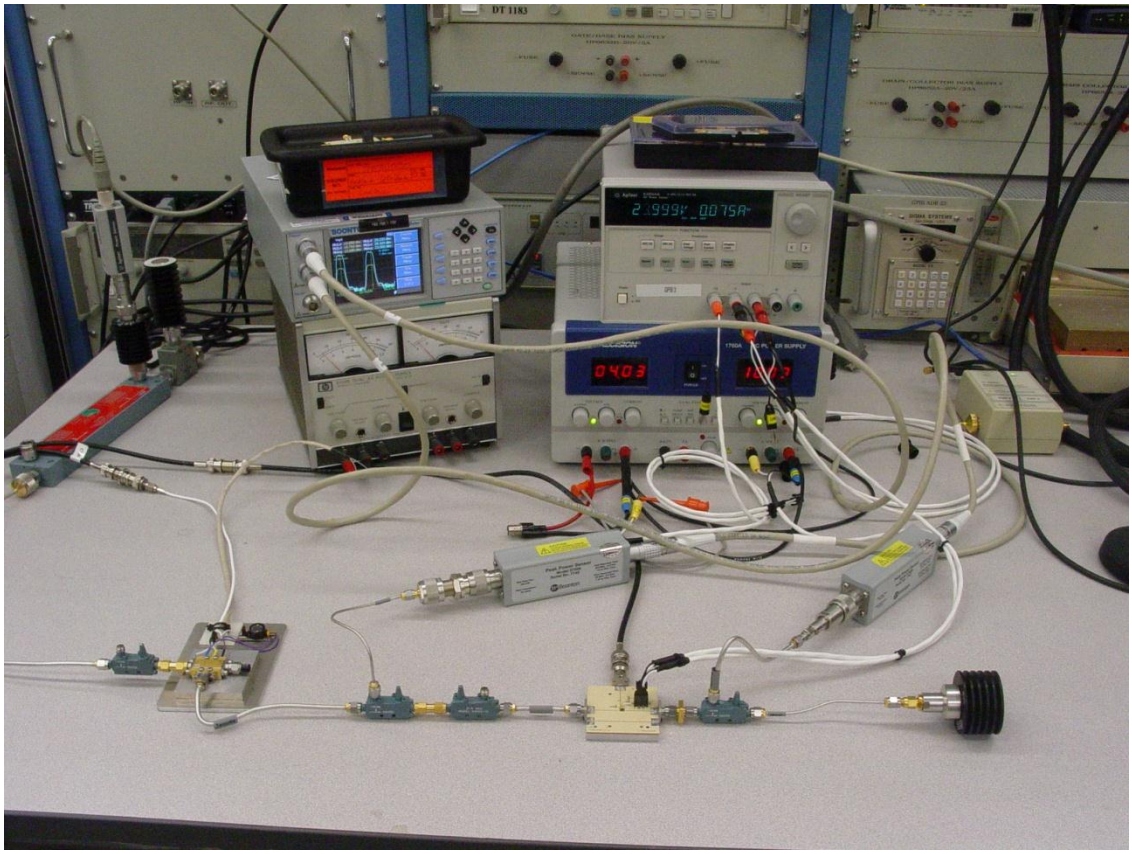

Figure 9-3: Lab setup of test bench

9.2 Test conditions

The amplifier is evaluated under the stimulus conditions listed in Table 9-1.

Supply Bias	$24V$
Gate Bias to Board	$-4.25V$
RF Input	18 dbm
Temp	$25C$
Pulse Width	$20ns$
Pulse Repetition Rate	10 MHz
Duty Cycle	20%

Table 9-1: Test board stimulus

9.3 Pulse power

The peak pulse power was measured at the coupled port of "Dir Coup4" and recorded at 100 MHz intervals from 2.0 GHz to 3.0 GHz. Power output across the band was flat to within 1dB over the interval. The pulse shape and on/off characteristics are shown in Figures 9-4 thru 9-6 respectively, for data taken at 3.0 GHz. This data is representative of the performance across the band.

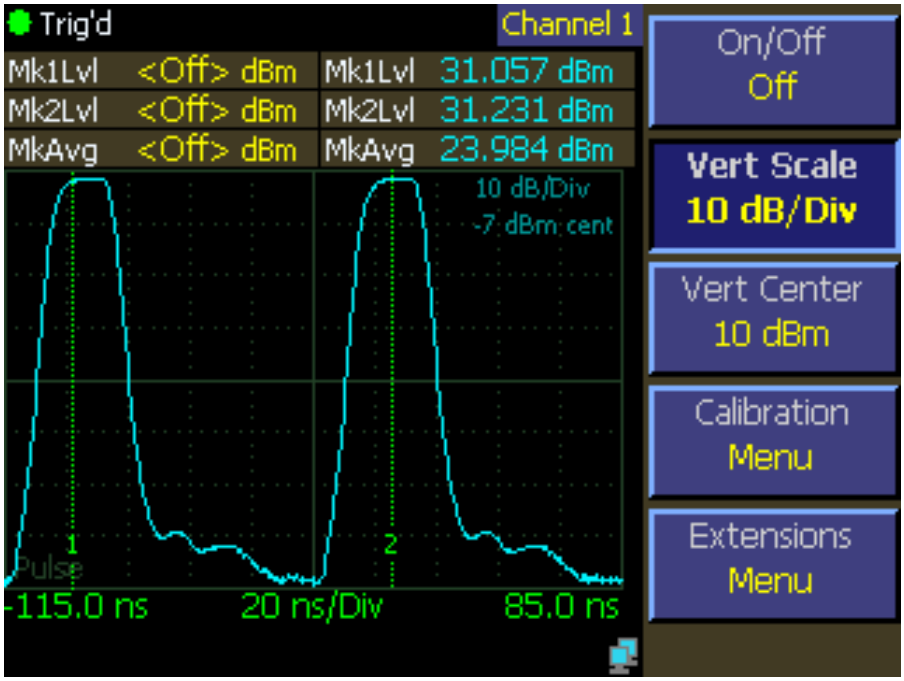

Figure 9-4: Peak power output at 2.9 GHz

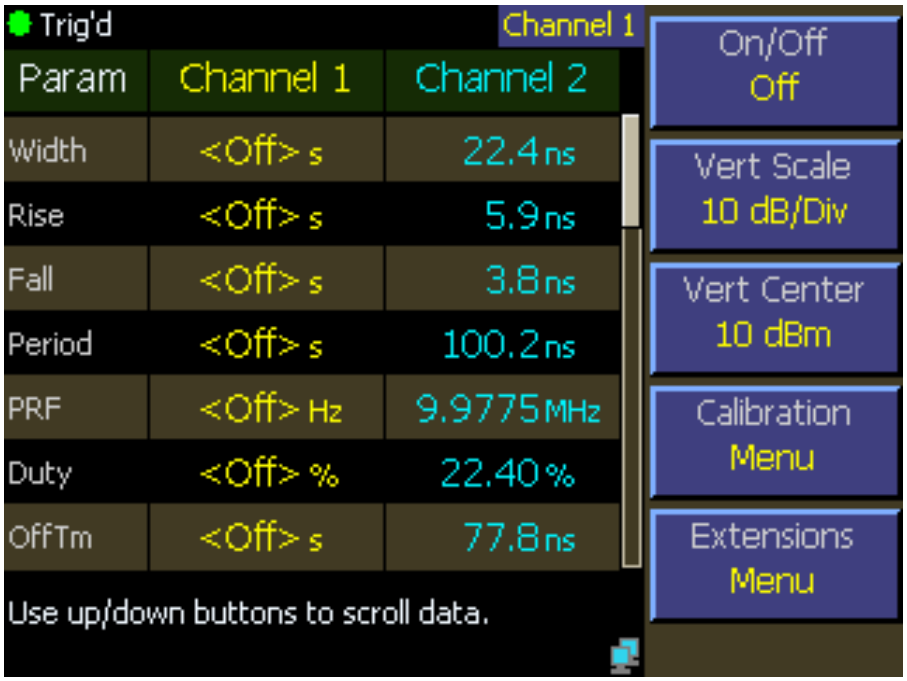

Figure 9-5: Pulse parameters

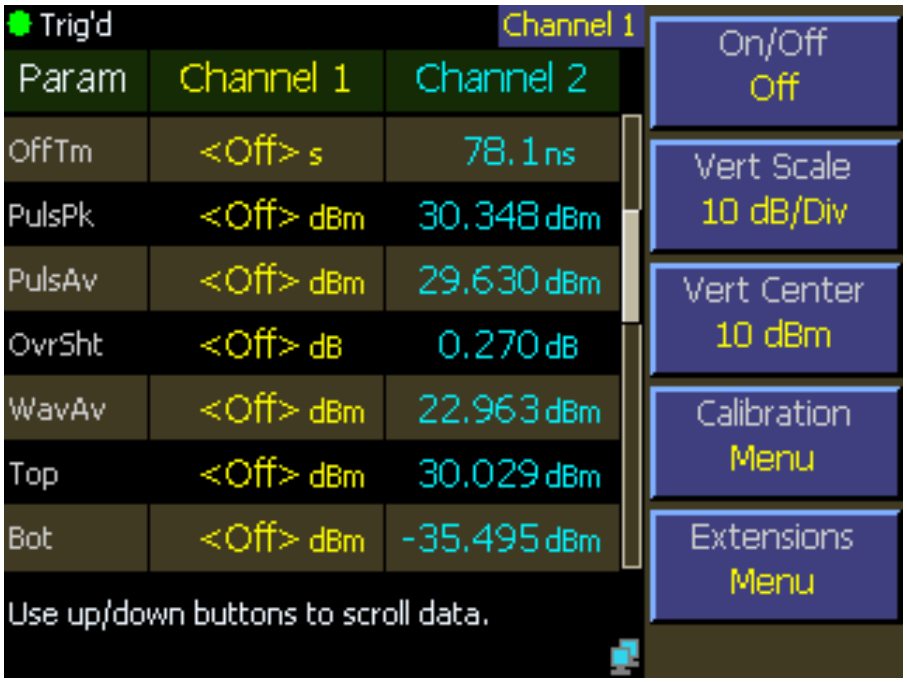

Figure 9-6: pulse parameters continued

9.4 Return Loss

The return loss is the difference between the incident pulsed power that is measured at "Dir Coup2" and the reflected pulse power measured at "Dir Coup3". This measurement is the true pulsed return loss measured under large signal conditions and under the conditions that the amplifier will see. This is recorded in 100 MHz increments from 2.0 to 3.0 GHz as shown in Figure 9-7.

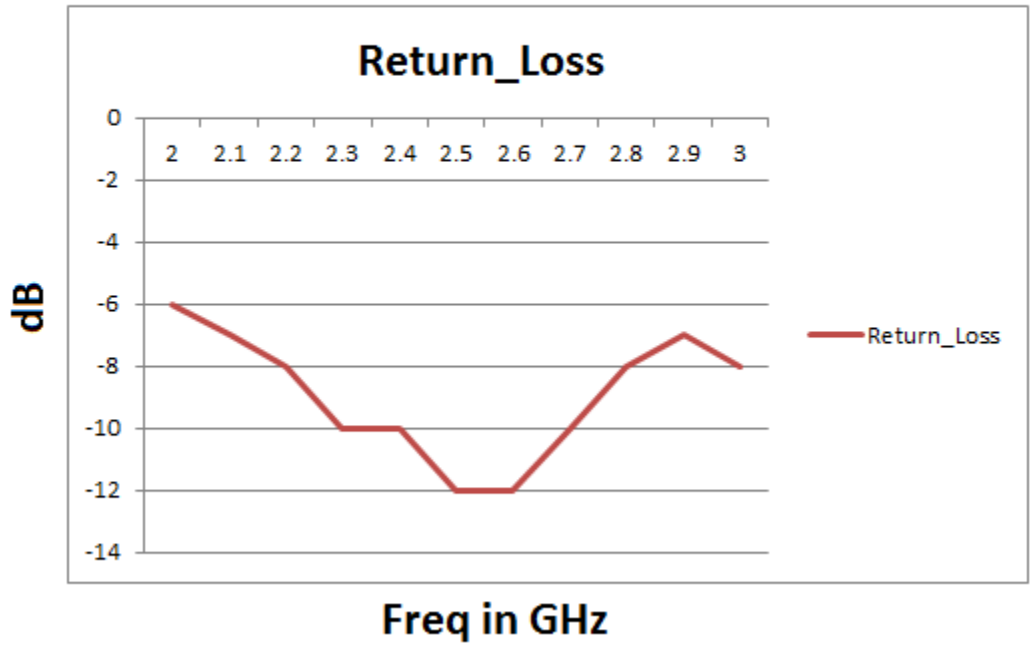

Figure 9-7: Return loss measured

9.5 Power across band

The power across the band is measured at "Dir Coup4". This is recorded in 100 MHz increments from 2.0 to 3.0 GHz as shown in Figure 9-8 and the power ripple across the band is approximately 0.85 dB.

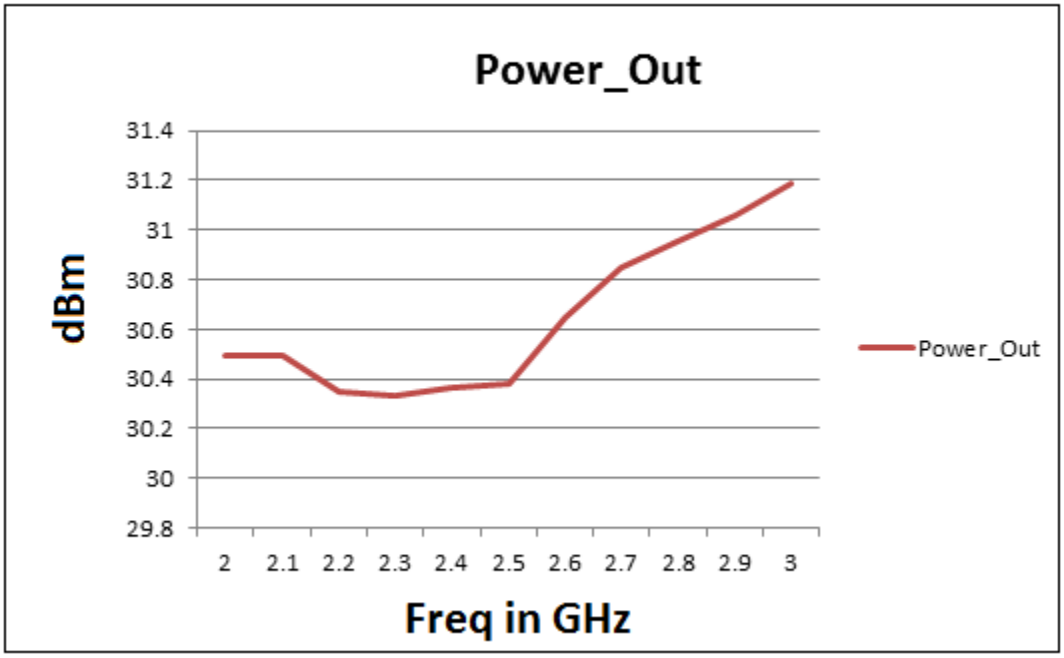

Figure 9-8: Power across band measured

9.6 Spectrum Analysis

The frequency spectrum was checked at 100 MHz intervals from 2.0 to 3.0 GHz for signs of oscillatory behavior, spurious or chaotic effects. At all frequencies the spectrum appeared good and representative of the following measurement plots. Figure 9-9 shows the spectrum at 3.0 GHz with a span of 2.0 GHz.

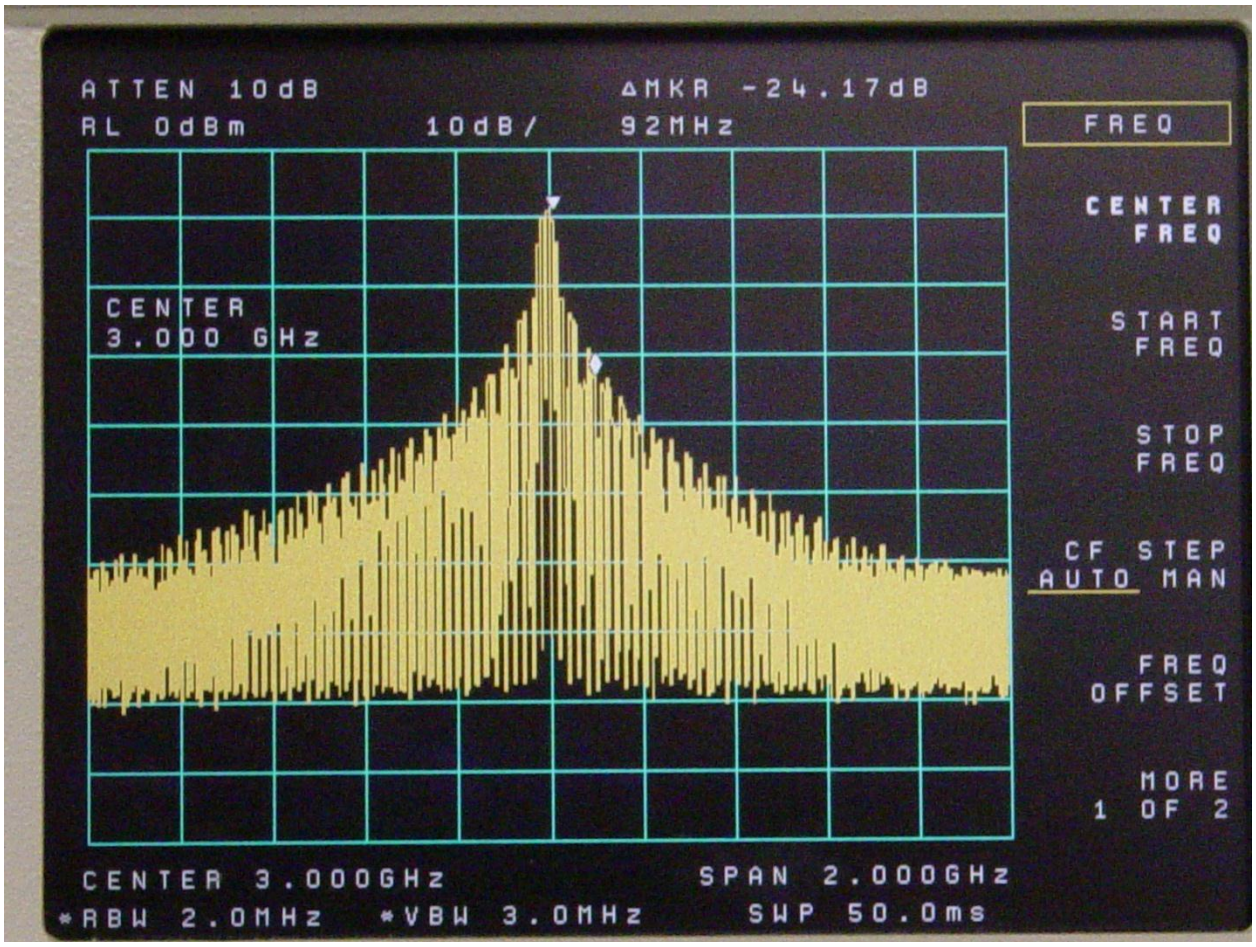

Figure 9-9: Spectrum measurement at 3.0 GHz, 2 GHz span

Figure 9-10 shows the wideband spectrum measurement from 10 MHz to 20 GHz. In this plot the third harmonic is shown with a marker on it and the value indicating the level is 32.50 dB below the main marker power at 3.0 GHz. The specification calls for all harmonics to be below 23 dbc. This specification is exceeded by 9.50 dB.

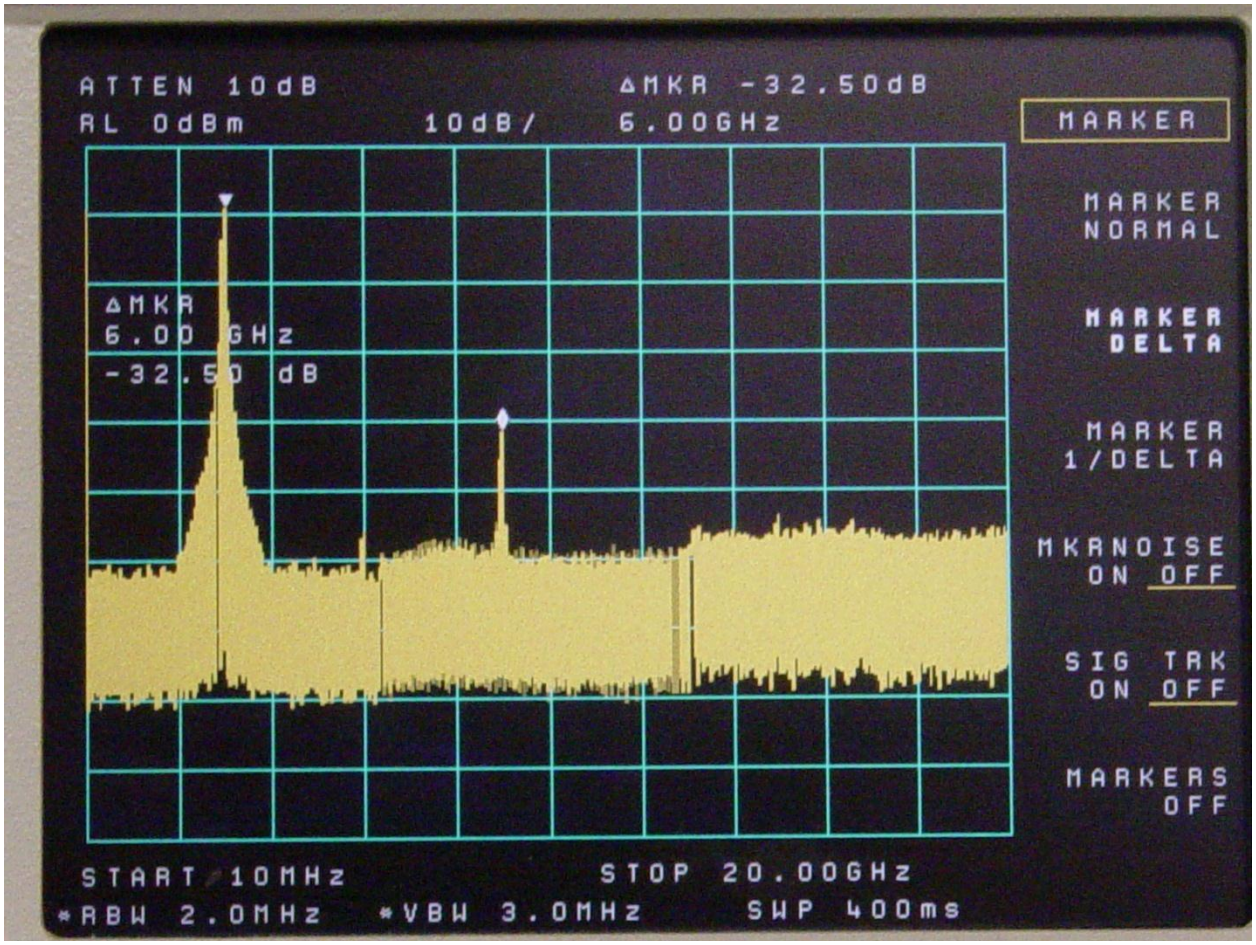

Figure 9-10: Spectrum measurement, third harmonic content

Figure 9-11 again shows the wideband spectrum measurement from 10 MHz to 20 GHz. In this plot the second harmonic is shown with a marker on it and the value indicating the level is 47.50 dB below the main marker power at 3.0 GHz. The specification calls for all harmonics to be below 23 dbc. This specification is exceeded by 24.50 dB.

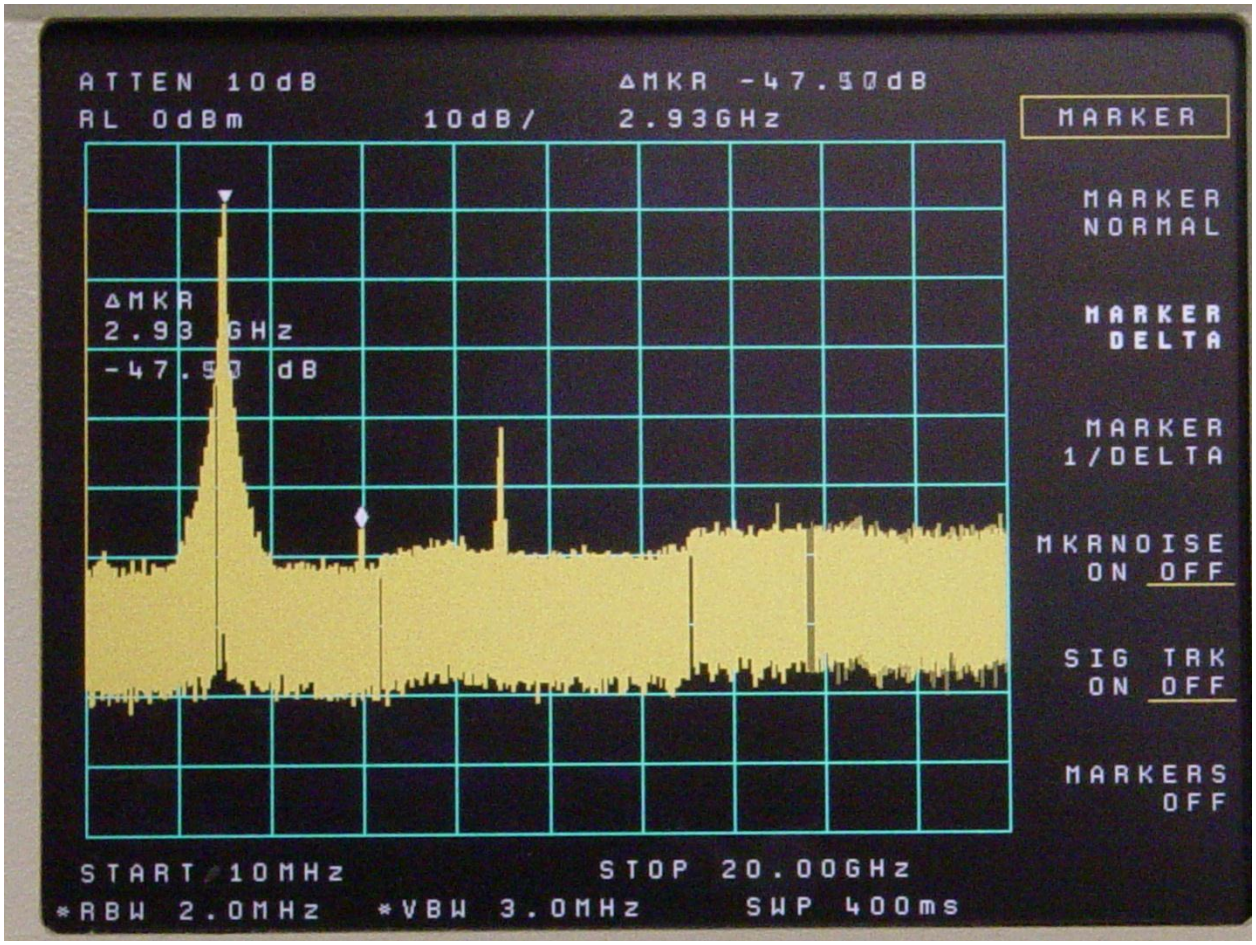

Figure 9-11: Spectrum measurement, second harmonic content

The final spectrum measurement is made with the RF power off but all the supplies on. This includes the 24V drain supply, the -2.2V gate bias and the input switch enable. No unstable operation was noticed.

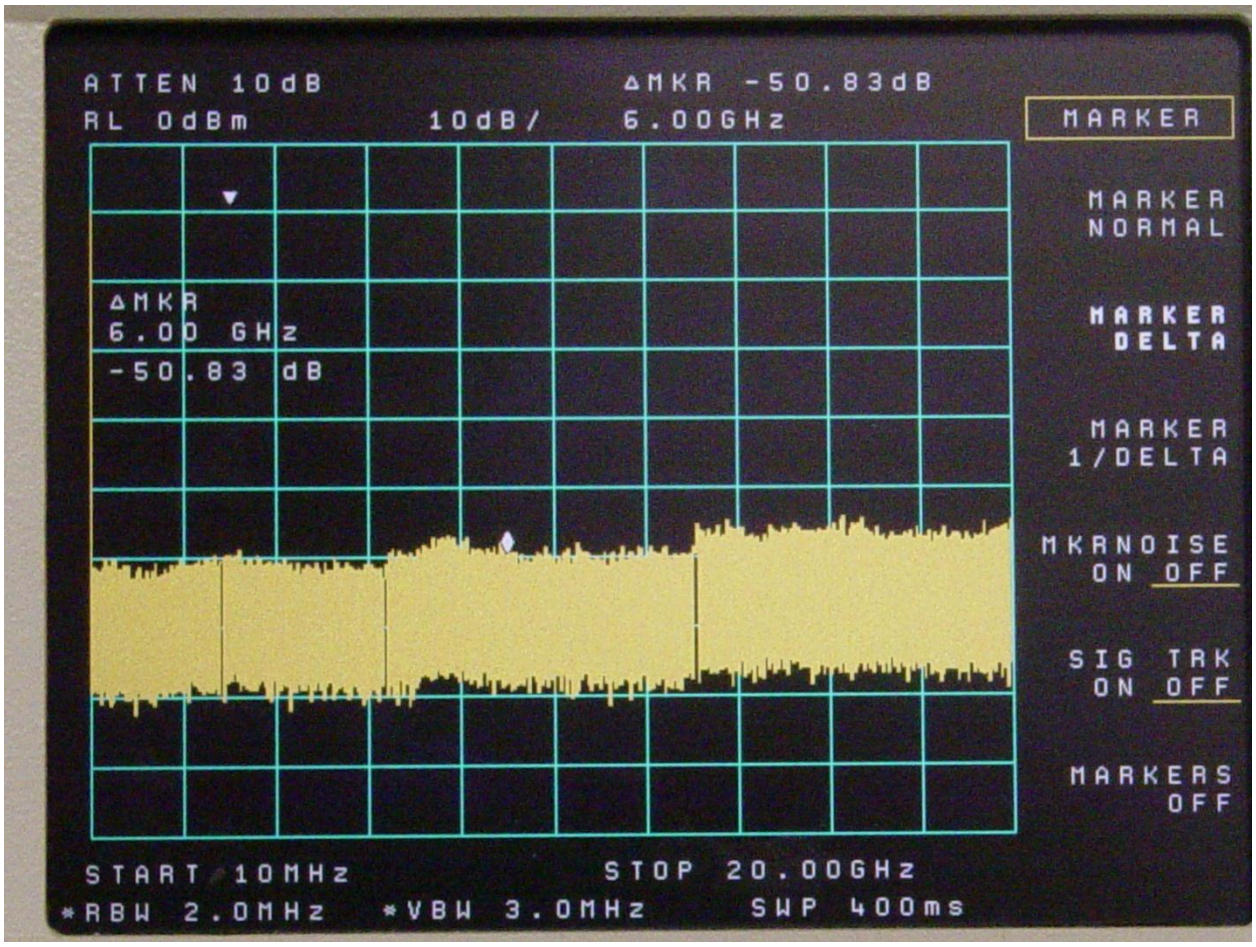

Figure 9-12: Spectrum measurement, no RF applied

Chapter 10 - **Conclusion**

The proper design of microwave amplifier circuits first requires a detailed knowledge of the amplifier type that is dictated by the system specifications followed by a rigorous approach to stability analysis that includes both linear and nonlinear methods. This thesis first examined the common types of current mode amplifiers that a designer has to choose from, namely the class A, AB, B and C. From a stability standpoint it is important to understand the nonlinear effects that are present in these architectures so that these areas of operation are avoided and that methods to stabilize these circuits are effective. It was also noted that there is no free lunch here and circuits added to stabilize an amplifier often do so by creating negative feedback that has the effect of lowering the gain, power output or detuning the matching networks.

High efficiency amplifiers were subsequently addressed. These types of amplifiers operate with the active device functioning as a switch delivering energy to tuned tank circuits in the drain output networks. These type of amplifiers do not purposely operate with feedback networks and methods to control any instability issues must not introduce them or efficiency will degrade. These types of amplifiers usually have minimal stabilizing networks often limited to small resistance values, usually less than 10 ohms, added at the gate.

Unstable behavior can take many different forms from continuous spectrum bands known as chaos, jumps and hysteresis effects, subharmonic oscillation and steady state oscillation. Oscillation start up conditions were defined in admittance terms as the point where the $Re(Y_T) < 0 \; and \; Im(Y_T) = 0$ and the auxiliary generator method was introduced as a way of monitoring the admittance at a particular node under varying drive amplitudes to test for stable operation.

Following the work of Aryeh Platzker and Wayne Struble [5], a rigorous evaluation of a ring oscillator circuit for stability has been demonstrated. It has been shown that the traditional linear stability analysis based on S-parameter analysis of a two port network and evaluating $K > 1 \; and \; B1 > 0$ is not sufficient by itself and can fail even for simple circuits. The results clearly indicate that the stability of the network must be verified first, either by NDF, transient, pole zero or analytical methods. Since our original goal was to determine stability by applying

the stability factor $and\ B1$, this restriction seriously questions the validity of its use in determining stability in the first place.

Performing a linear stability analysis on an amplifier does not accurately indicate stability as amplifiers are not linear devices and are subject to nonlinear operating conditions such as second and third order distortion and compression. In order to include these effects and to do a complete analysis of stability, nonlinear tools are required. The auxiliary generator method is the primary method for nonlinear stability analysis. It looks for the oscillation condition $Re(Y_T) < 0\ and\ Im(Y_T) = 0$ by perturbing the circuit at sensitive node locations such as at the gate of an RF amplifier FET or at feedback locations. The auxiliary generator method allows for an infinite number of drive levels in order to check stability and unlike the other methods it doesn't have to be a reduced two port network. It is one of the few nonlinear stability methods being used and highlights the need for commercial microwave software companies to develop time domain and harmonic balance based non-linear stability tools. NDF based nonlinear tools that rely on an extension of the specific functions for linear stability have been developed by Campovecchio and others but have not found widespread use and implementation into commercially available software packages as of yet [14].

These methods were next applied to the design and analysis of a 1W pulse modulated amplifier. GaN has excellent thermal features due to its construction on a Silicon Carbide (SiC) substrate. This process enables high power density, greater than four times the power density of GaAs and ten times the thermal conductivity. Even though the GaN process has excellent thermal properties a complete evaluation of the heat flow out of the die into the heatsink is required to avoid heat related failure mechanisms and degradations to reliability.

The methodology of the design and the recommended battery of stability measurements undertaken for the 1W pulse modulated amplifier were demonstrated with simulation data and laboratory test results. Stability was verified through multiple tools to include conventional K and B1, $Mu1$ and $Mu2$ analysis, Nyquist and most importantly the NDF tool. Under conditions where the NDF tool indicate stability the results of the K and B1 analysis guarantee that stability will be maintained through all source and load values.

Finally, test measurements confirm the success of the design and the approach and that the amplifier was stable. It also exceeded the design specifications of 1W pulsed output power, at a pulse width of 20 ns, from 2.0 GHz to 3.0 GHz with less than 1 dB ripple.

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[19] Cree Semiconductor. Available: www.cree.com

Appendix A - Maple code for case 1

```
> with(LinearAlgebra) :
>
>
```

$$> A := \begin{bmatrix} G_2 + Y_s & 0 & -G_2 & 0 \\ 0 & G_2 + Y_1 & 0 & -G_2 \\ -G_2 & 0 & T_1 & T_2 \\ 0 & -G_2 & T_3 & T_4 \end{bmatrix}$$

$$A := \left[\left[\frac{1}{25}, 0, -\frac{1}{50}, 0\right], \left[0, \frac{1}{25}, 0, -\frac{1}{50}\right], \left[-\frac{1}{50}, 0, \frac{1}{50} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s, -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}\right], \left[0, -\frac{1}{50}, -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}, \frac{1}{50} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s\right]\right]$$

$$> \Delta := Determinant(A)$$

$$\Delta := \left(4.687420281\,10^{25}\,s^2 + 1.165880104\,10^{15}\,s^3 + 8.187500002\,10^{5}\,s^4 + 6.118463008\,10^{35}\,s + 0.00002322285714\,s^5 + 7.040000000\,10^{-17}\,s^6 + 1.245615434\,10^{45}\right) \Big/ \left(s^2\,(6250000000 + s)^2\,(6.250000000\,10^{9} + s)\right)$$

$$> R_1 := 10$$

$$R_1 := 10$$

> $C_1 := 16 \cdot 10^{-12}$

$$C_1 := \frac{1}{62500000000}$$

> $C_f := 0.1 \cdot 10^{-12}$

$$C_f := 1.000000000\,10^{-13}$$

> $g_{m1} := 0.5$

$$g_{m1} := 0.5$$

> $g_{m2} := 0.4$

$$g_{m2} := 0.4$$

> $G_2 := \frac{1}{50}$

$$G_2 := \frac{1}{50}$$

> $L_1 := 560 \cdot 10^{-12}$

$$L_1 := \frac{7}{12500000000}$$

>

>

> $T_1 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_1 := \frac{1}{50} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $T_2 := -2 \cdot s \cdot C_f + \frac{g_{m2}}{1 + s \cdot C_1 \cdot R_1}$

$$T_2 := -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}$$

> $T_3 := -2 \cdot s \cdot C_f + \frac{g_{m1}}{1 + s \cdot C_1 \cdot R_1}$

$$T_3 := -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}$$

> $T_4 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_4 := \frac{1}{50} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $Y_1 := 20 \cdot 10^{-3}$

$$Y_1 := \frac{1}{50}$$

> $Y_s := 20 \cdot 10^{-3}$

$$Y_s := \frac{1}{50}$$

>

>

>

> $\Delta num := numer(\mathbf{(2)})$

$$\Delta num := 4.687420281\,10^{25}\,s^2 + 1.165880104\,10^{15}\,s^3 + 8.187500002\,10^{5}\,s^4 + 6.118463008\,10^{35}\,s + 0.00002322285714\,s^5 + 7.040000000\,10^{-17}\,s^6 + 1.245615434\,10^{45}$$

> $solve(\ \mathbf{(16)} = 0, s\ )$

$$4.250831105\,10^{9} + 8.843684454\,10^{9}\,\mathrm{I},\ -2.558709415\,10^{9},\ -6.249999996\,10^{9},\ -3.963538769\,10^{10},\ -2.899276949\,10^{11},\ 4.250831105\,10^{9} - 8.843684454\,10^{9}\,\mathrm{I}$$

Appendix B - Maple code for case 2

```
> with(LinearAlgebra) :
>
>
```

$$> A := \begin{bmatrix} G_2 + Y_s & 0 & -G_2 & 0 \\ 0 & G_2 + Y_1 & 0 & -G_2 \\ -G_2 & 0 & T_1 & T_2 \\ 0 & -G_2 & T_3 & T_4 \end{bmatrix}$$

$$A := \left[\left[\frac{11}{50}, 0, -\frac{1}{5}, 0\right], \left[0, \frac{11}{50}, 0, -\frac{1}{5}\right], \left[-\frac{1}{5}, 0, \frac{1}{5} + \frac{12500000000}{7s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s, -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}\right], \left[0, -\frac{1}{5}, -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}, \frac{1}{5} + \frac{12500000000}{7s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s\right]\right]$$

$$> \Delta := Determinant(A)$$

$$\Delta := \left(1.586405851\,10^{27}\,s^2 + 6.622596450\,10^{16}\,s^3 + 2.739928574\,10^{7}\,s^4 + 1.885363520\,10^{37}\,s + 0.0007958214290\,s^5 + 2.288000000\,10^{-15}\,s^6 + 3.767986686\,10^{46}\right) \Big/ \left(s^2\,(6250000000 + s)^2\,(6.250000000\,10^{9} + s)\right)$$

$$> R_1 := 10$$

$$R_1 := 10$$

> $C_1 := 16 \cdot 10^{-12}$

$$C_1 := \frac{1}{62500000000}$$

> $C_f := 0.1 \cdot 10^{-12}$

$$C_f := 1.000000000\,10^{-13}$$

> $g_{m1} := 0.5$

$$g_{m1} := 0.5$$

> $g_{m2} := 0.4$

$$g_{m2} := 0.4$$

> $G_2 := \frac{1}{5}$

$$G_2 := \frac{1}{5}$$

> $L_1 := 560 \cdot 10^{-12}$

$$L_1 := \frac{7}{12500000000}$$

>

>

> $T_1 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_1 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $T_2 := -2 \cdot s \cdot C_f + \frac{g_{m2}}{1 + s \cdot C_1 \cdot R_1}$

$$T_2 := -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}$$

> $T_3 := -2 \cdot s \cdot C_f + \frac{g_{m1}}{1 + s \cdot C_1 \cdot R_1}$

$$T_3 := -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}$$

> $T_4 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_4 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $Y_1 := 20 \cdot 10^{-3}$

$$Y_1 := \frac{1}{50}$$

> $Y_s := 20 \cdot 10^{-3}$

$$Y_s := \frac{1}{50}$$

>

>

>

> $\Delta num := numer(\mathbf{(2)})$

$$\Delta num := 1.586405851\,10^{27}\,s^2 + 6.622596450\,10^{16}\,s^3 + 2.739928574\,10^{7}\,s^4 + 1.885363520\,10^{37}\,s + 0.0007958214290\,s^5 + 2.288000000\,10^{-15}\,s^6 + 3.767986686\,10^{46}$$

> $solve(\ \mathbf{(16)} = 0, s\ )$

$$3.766540938\,10^{9} + 8.719424663\,10^{9}\,\mathrm{I},\ -2.539824094\,10^{9},\ -6.249999996\,10^{9},\ -3.716814100\,10^{10},\ -3.093991679\,10^{11},\ 3.766540938\,10^{9} - 8.719424663\,10^{9}\,\mathrm{I}$$

Appendix C - Maple code for case 3

```
> with(LinearAlgebra) :
>
>
```

$$> A := \begin{bmatrix} G_2 + Y_s & 0 & -G_2 & 0 \\ 0 & G_2 + Y_1 & 0 & -G_2 \\ -G_2 & 0 & T_1 & T_2 \\ 0 & -G_2 & T_3 & T_4 \end{bmatrix}$$

$$A := \left[\left[0.3500000000 + \frac{2000000000}{s}, 0, -\frac{1}{5}, 0\right],\right.$$
$$\left[0, 0.3000000000 + \frac{800000000}{s}, 0, -\frac{1}{5}\right],$$
$$\left[-\frac{1}{5}, 0, \frac{1}{5} + \frac{12500000000}{7\,s}\right.$$
$$\left. + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s,\right.$$
$$\left.\left. -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}\right],\right.$$
$$\left[0, -\frac{1}{5}, -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}, \frac{1}{5}\right.$$
$$+ \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s}$$
$$\left.\left. + 2.000000000\,10^{-13}\,s\right]\right]$$

```
> Δ := Determinant(A)
```

$$\Delta := \left(2.046147540\,10^{28}\,s^4 + 2.185130999\,10^{18}\,s^5 + 1.56056375\,10^{8}\,s^6\right.$$
$$+ 1.530457988\,10^{38}\,s^3 + 0.003638824998\,s^7$$
$$+ 7.400000000\,10^{-15}\,s^8 + 7.049099669\,10^{47}\,s^2$$
$$\left. + 1.562001754\,10^{57}\,s + 1.245615434\,10^{66}\right) /$$
$$\left(s^4\,(6250000000 + s)^2\,\left(6.250000000\,10^{9} + s\right)\right)$$

```
> R_1 := 10
```

$$R_1 := 10$$

> $C_1 := 16 \cdot 10^{-12}$

$$C_1 := \frac{1}{62500000000}$$

> $C_f := 0.1 \cdot 10^{-12}$

$$C_f := 1.000000000\,10^{-13}$$

> $g_{m1} := 0.5$

$$g_{m1} := 0.5$$

> $g_{m2} := 0.4$

$$g_{m2} := 0.4$$

> $G_2 := \frac{1}{5}$

$$G_2 := \frac{1}{5}$$

> $L_1 := 560 \cdot 10^{-12}$

$$L_1 := \frac{7}{12500000000}$$

>

>

> $T_1 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_1 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $T_2 := -2 \cdot s \cdot C_f + \frac{g_{m2}}{1 + s \cdot C_1 \cdot R_1}$

$$T_2 := -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}$$

> $T_3 := -2 \cdot s \cdot C_f + \frac{g_{m1}}{1 + s \cdot C_1 \cdot R_1}$

$$T_3 := -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}$$

> $T_4 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_4 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $Y_1 := 0.100 + \frac{1}{s \cdot 1250 \cdot 10^{-12}}$

$$Y_1 := 0.100 + \frac{800000000}{s}$$

> $Y_s := 0.150 + \frac{1}{s \cdot 500 \cdot 10^{-12}}$

$$Y_s := 0.150 + \frac{2000000000}{s}$$

>

>

>

> $\Delta num := numer(\mathbf{(2)})$

$$\Delta num := 2.046147540\,10^{28}\,s^4 + 2.185130999\,10^{18}\,s^5 + 1.56056375\,10^{8}\,s^6 + 1.530457988\,10^{38}\,s^3 + 0.003638824998\,s^7 + 7.400000000\,10^{-15}\,s^8 + 7.049099669\,10^{47}\,s^2 + 1.562001754\,10^{57}\,s + 1.245615434\,10^{66}$$

> $solve(\mathbf{(16)} = 0, s)$

$$7.404047350\,10^{7} + 8.167585465\,10^{9}\,\mathrm{I},\ -1.831058256\,10^{9},\ -2.944209825\,10^{9},\ -5.748229152\,10^{9},\ -6.250000251\,10^{9},\ -2.921557062\,10^{10},\ -4.458921207\,10^{11},\ 7.404047350\,10^{7} - 8.167585465\,10^{9}\,\mathrm{I}$$

Appendix D - Maple code for case 4

```
> with(LinearAlgebra) :
>
>
```

$$> A := \begin{bmatrix} G_2 + Y_s & 0 & -G_2 & 0 \\ 0 & G_2 + Y_1 & 0 & -G_2 \\ -G_2 & 0 & T_1 & T_2 \\ 0 & -G_2 & T_3 & T_4 \end{bmatrix}$$

$$A := \left[\left[0.2500000000 + \frac{2000000000}{s}, 0, -\frac{1}{5}, 0\right], \left[0, 0.3000000000 + \frac{800000000}{s}, 0, -\frac{1}{5}\right], \left[-\frac{1}{5}, 0, \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s, -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}\right], \left[0, -\frac{1}{5}, -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}, \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s\right]\right]$$

```
> Δ := Determinant(A)
```

$$\Delta := (1.636666313\,10^{28}\,s^4 + 1.645926159\,10^{18}\,s^5 + 1.031161965\,10^{8}\,s^6 + 1.288629225\,10^{38}\,s^3 + 0.002029046428\,s^7 + 4.600000000\,10^{-15}\,s^8 + 6.377090143\,10^{47}\,s^2 + 1.499720982\,10^{57}\,s + 1.245615434\,10^{66}) / (s^4\,(6250000000 + s)^2\,(6.250000000\,10^{9} + s))$$

> $R_1 := 10$

$$R_1 := 10$$

> $C_1 := 16 \cdot 10^{-12}$

$$C_1 := \frac{1}{62500000000}$$

> $C_f := 0.1 \cdot 10^{-12}$

$$C_f := 1.000000000\,10^{-13}$$

> $g_{m1} := 0.5$

$$g_{m1} := 0.5$$

> $g_{m2} := 0.4$

$$g_{m2} := 0.4$$

> $G_2 := \frac{1}{5}$

$$G_2 := \frac{1}{5}$$

> $L_1 := 560 \cdot 10^{-12}$

$$L_1 := \frac{7}{12500000000}$$

>

>

> $T_1 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_1 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $T_2 := -2 \cdot s \cdot C_f + \frac{g_{m2}}{1 + s \cdot C_1 \cdot R_1}$

$$T_2 := -2.000000000\,10^{-13}\,s + \frac{0.4}{1 + \frac{1}{6250000000}\,s}$$

> $T_3 := -2 \cdot s \cdot C_f + \frac{g_{m1}}{1 + s \cdot C_1 \cdot R_1}$

$$T_3 := -2.000000000\,10^{-13}\,s + \frac{0.5}{1 + \frac{1}{6250000000}\,s}$$

> $T_4 := G_2 + \frac{1}{s \cdot L_1} + \frac{s \cdot C_1}{1 + s \cdot C_1 \cdot R_1} + 2 \cdot s \cdot C_f$

$$T_4 := \frac{1}{5} + \frac{12500000000}{7\,s} + \frac{1}{62500000000}\,\frac{s}{1 + \frac{1}{6250000000}\,s} + 2.000000000\,10^{-13}\,s$$

> $Y_1 := 0.100 + \frac{1}{s \cdot 1250 \cdot 10^{-12}}$

$$Y_1 := 0.100 + \frac{800000000}{s}$$

> $Y_s := 0.050 + \frac{1}{s \cdot 500 \cdot 10^{-12}}$

$$Y_s := 0.050 + \frac{2000000000}{s}$$

>

>

>

> $\Delta num := numer(\mathbf{(2)})$

$$\Delta num := 1.636666313\,10^{28}\,s^4 + 1.645926159\,10^{18}\,s^5 + 1.031161965\,10^{8}\,s^6 + 1.288629225\,10^{38}\,s^3 + 0.002029046428\,s^7 + 4.600000000\,10^{-15}\,s^8 + 6.377090143\,10^{47}\,s^2 + 1.499720982\,10^{57}\,s + 1.245615434\,10^{6}$$

> $solve(\mathbf{(16)} = 0, s)$

$$-1.675993767\,10^{8} + 8.467375748\,10^{9}\,I,\ -1.833771651\,10^{9},\ -2.965127087\,10^{9},\ -6.249999961\,10^{9},\ -7.886135470\,10^{9},\ -3.656537277\,10^{10},\ -3.852614439\,10^{11},\ -1.675993767\,10^{8} - 8.467375748\,10^{9}\,I$$

Appendix E - Schematics

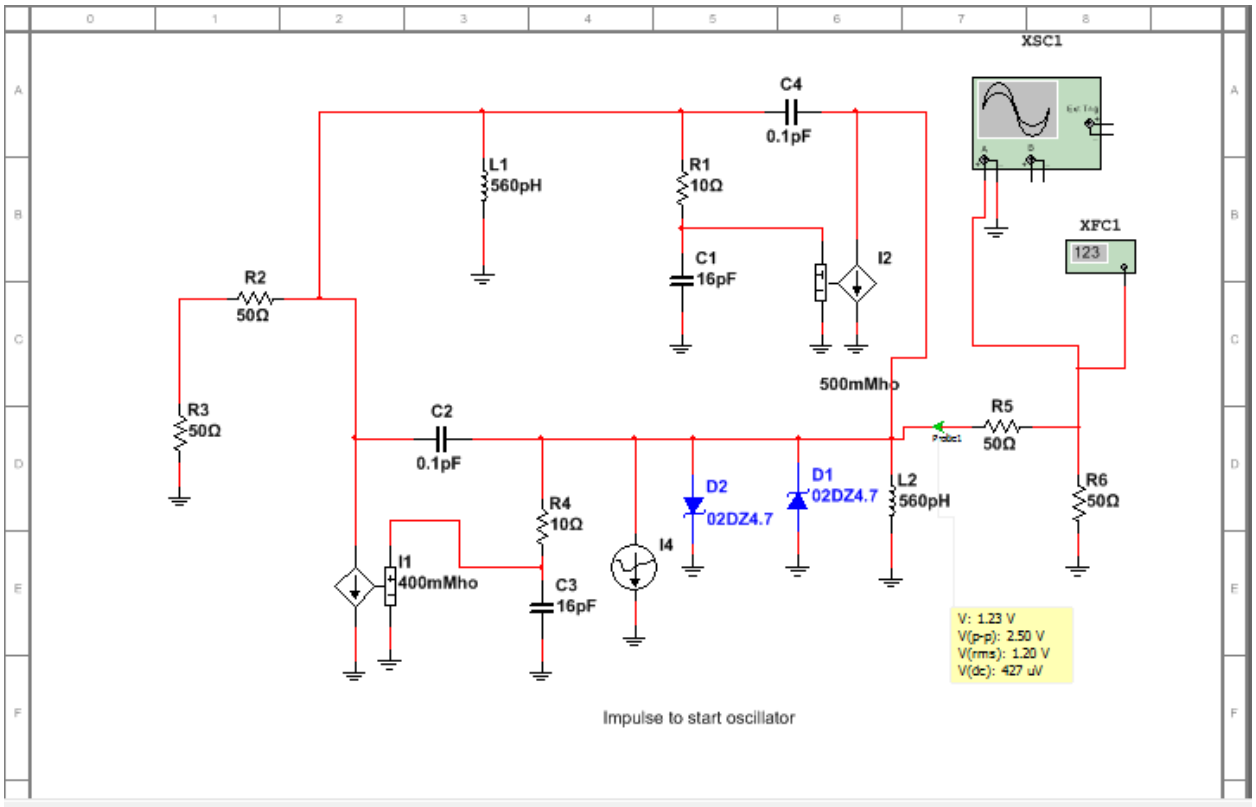

Figure E-1: Case 1 transient analysis schematic

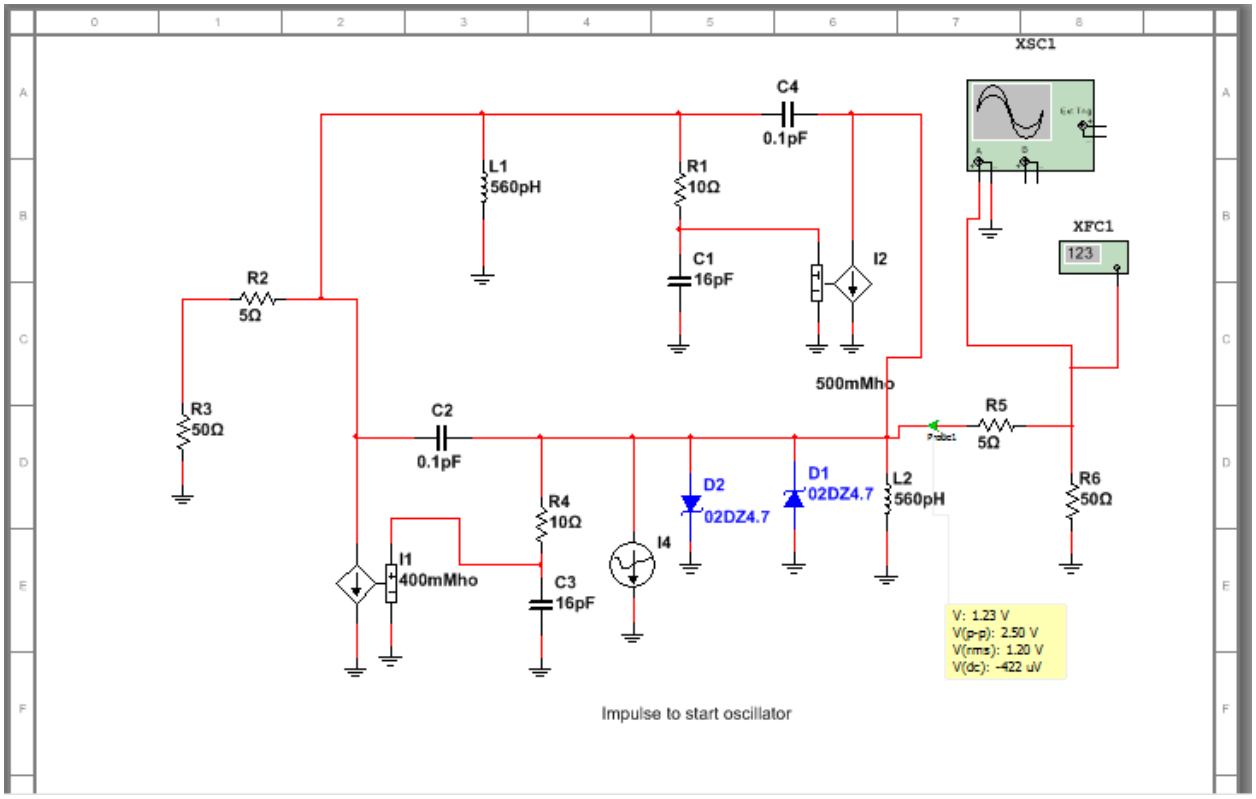

Figure E-2: Case 2 transient analysis schematic

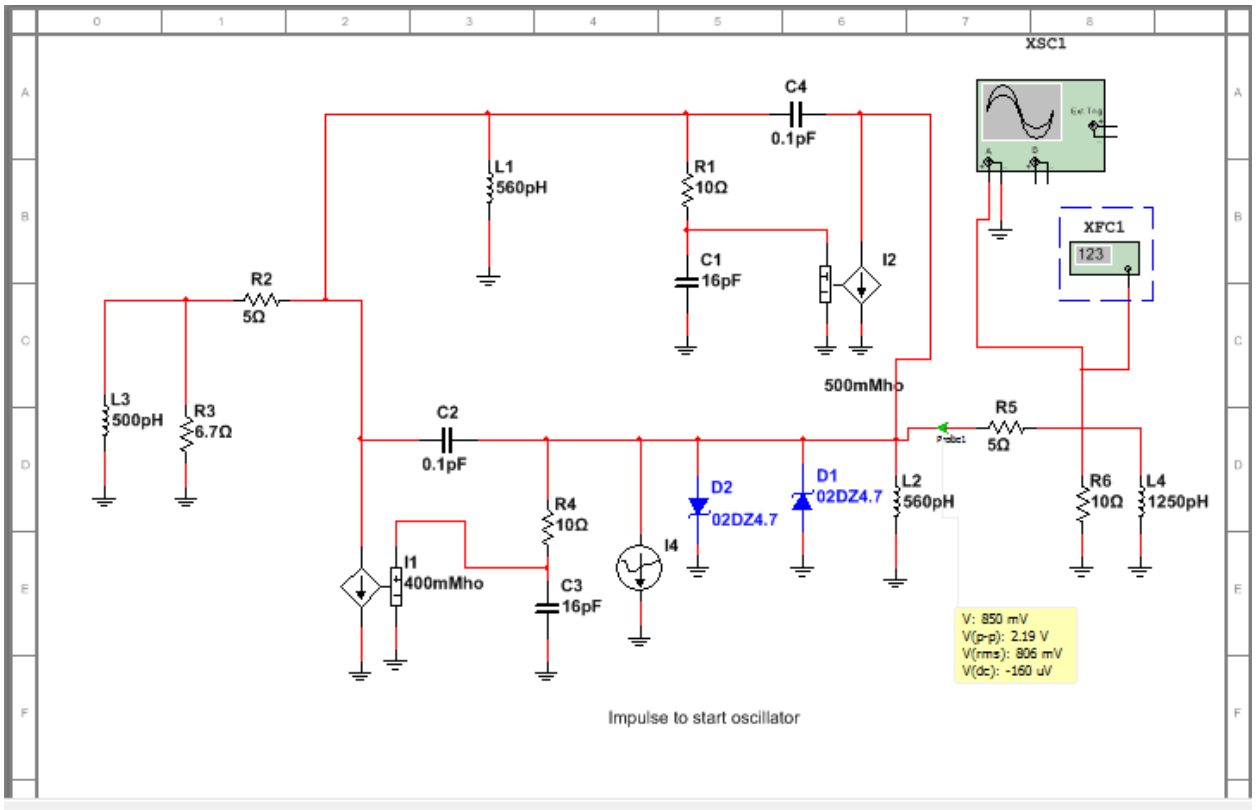

Figure E-3: Case 3 transient schematic

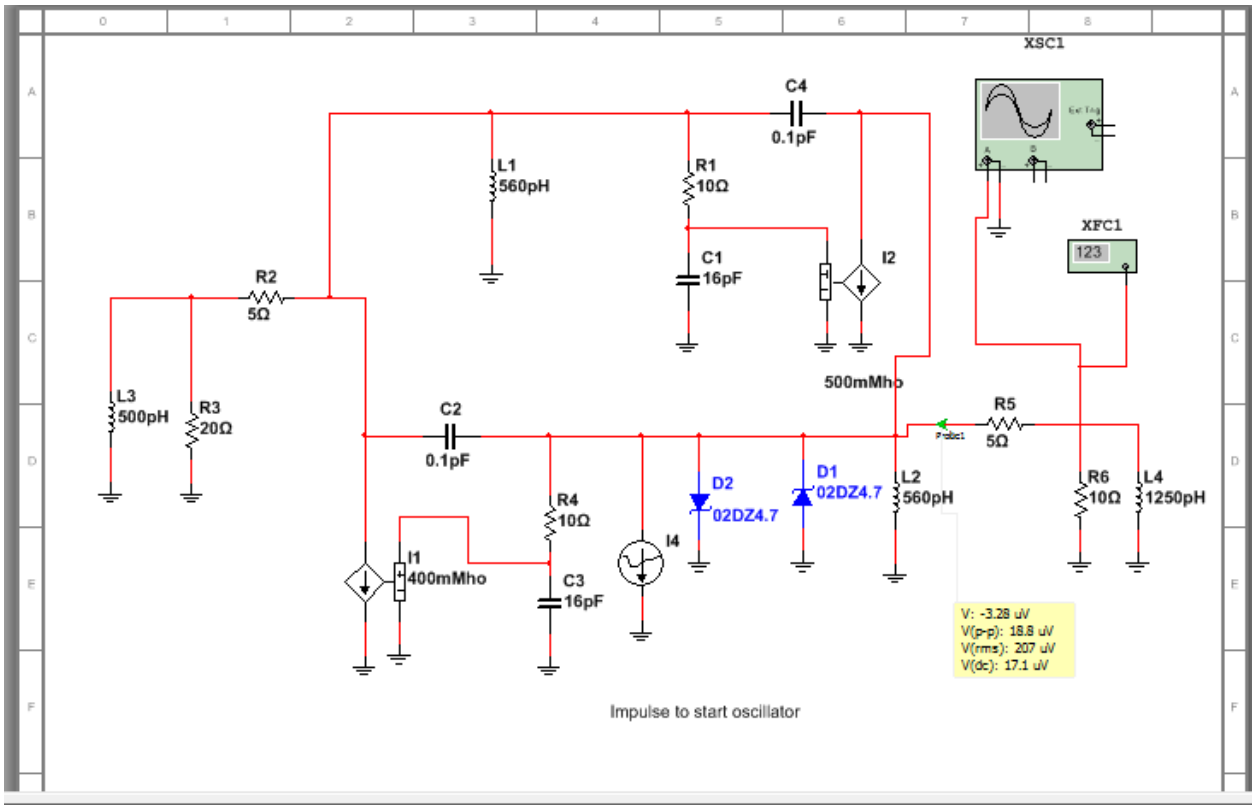

Figure E-4: Case 4 transient schematic

Appendix F - Auxiliary Generator

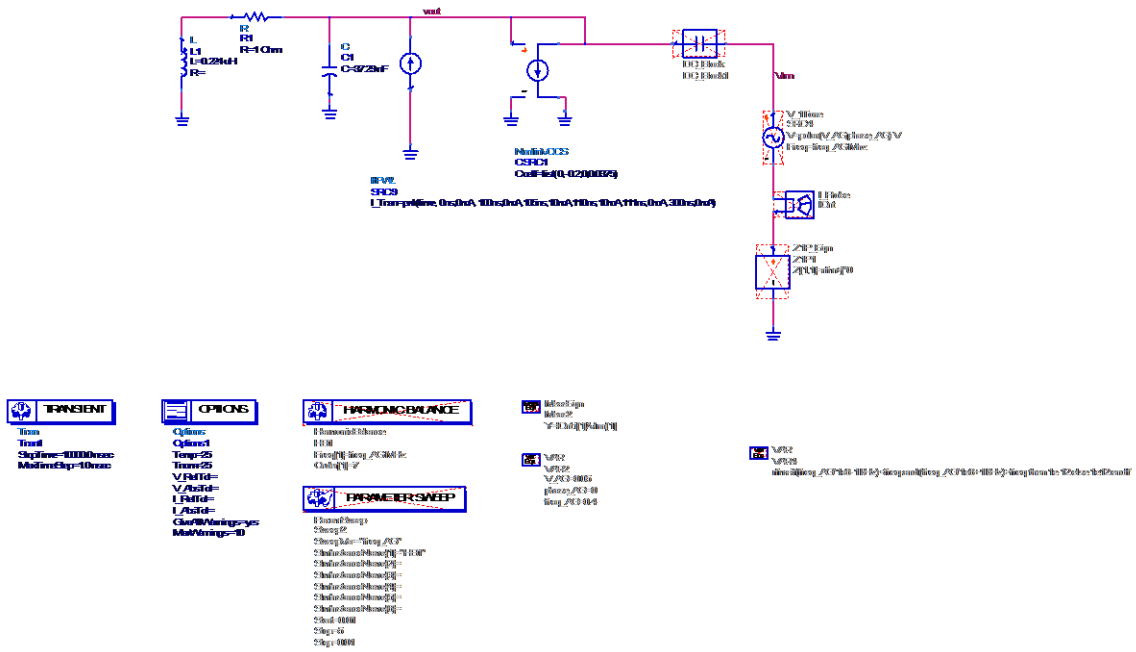

Figure F-1: Transient Analysis schematic for Auxiliary generator

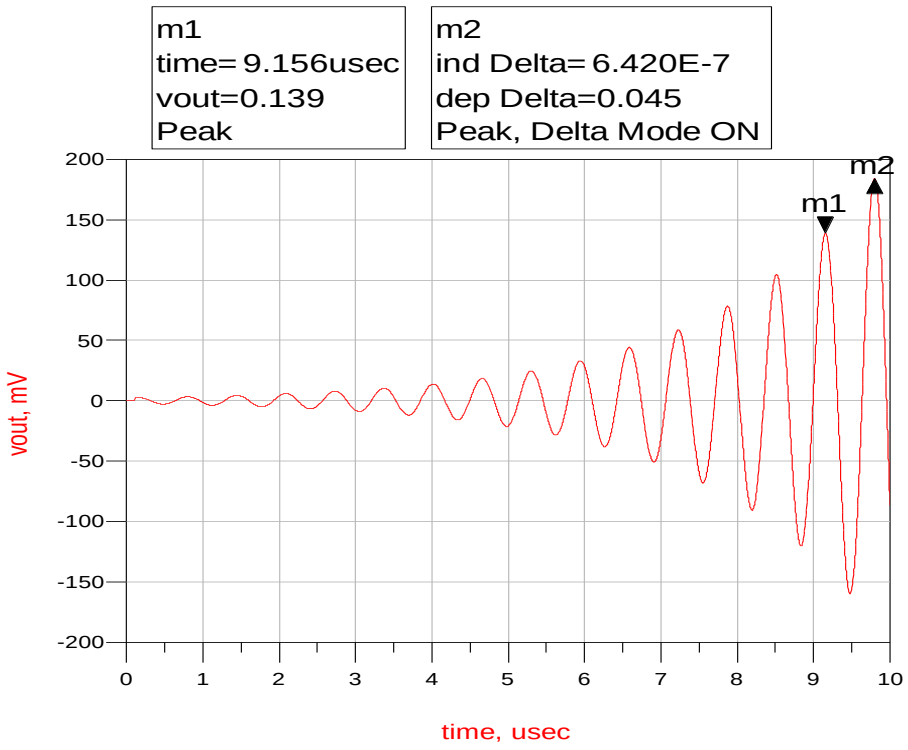

Figure F-2: Results 1, Transient Analysis of Auxiliary Generator circuit

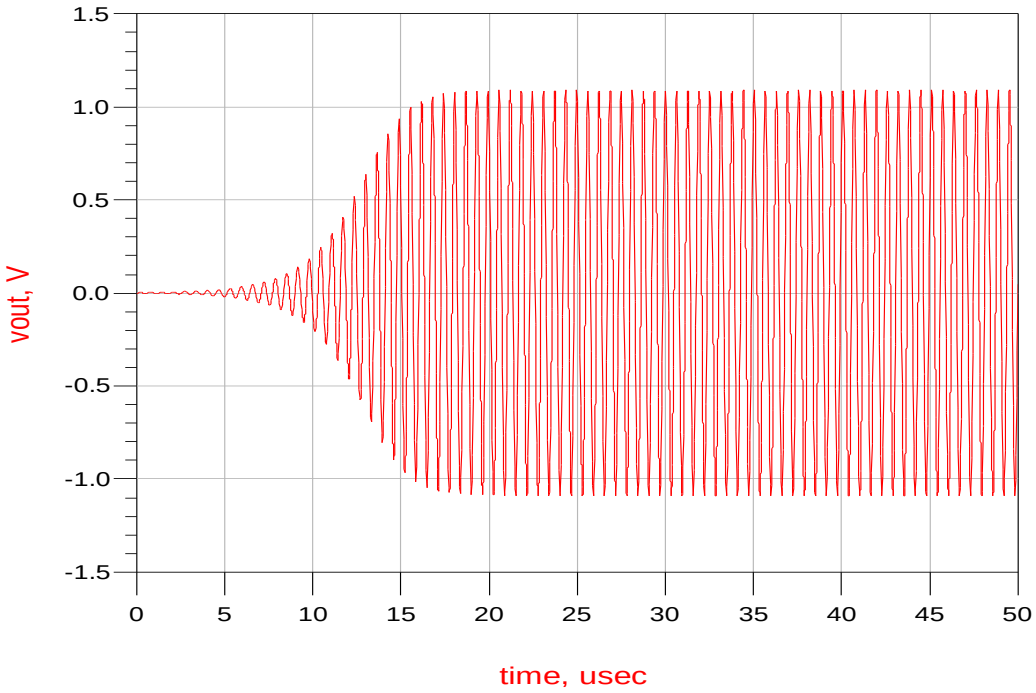

Figure F-3: Results 2, Transient Analysis of Auxiliary Generator circuit