THE DESIGN OF A SERIAL MSK MODEM

by

LARRY N. PHILLIPS

B. S., Kansas State University, 1978

———————————

A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1980

Approved by:

Donald R. Hummele
Major Professor

TABLE OF CONTENTS

THIS BOOK CONTAINS NUMEROUS PAGES WITH DIAGRAMS THAT ARE CROOKED COMPARED TO THE REST OF THE INFORMATION ON THE PAGE.

THIS IS AS RECEIVED FROM CUSTOMER.

LIST OF FIGURES

CHAPTER I

INTRODUCTION

The spectral congestion in the radio frequency (RF) band as a result of increased demand for digital transmission channels has inspired a search for more efficient signaling techniques. The goal is to use as little transmitter power and channel bandwidth as possible without sacrificing error rate performance. The efforts to realize this goal have led to the development of several spectrally efficient digital transmission schemes. These schemes include quadrature phase-shift keying (QPSK), offset QPSK (OQPSK), and minimum shift keying (MSK) [1].

MSK represents a special case of frequency shift keying (FSK) because the frequency separation between the two signaling frequencies is only half that of conventional orthogonal FSK [1], [3]. For this reason, MSK is often referred to as fast FSK. MSK sometimes goes by the name of continuous phase FSK (CPFSK) because of its continuous phase characteristic. This phase continuity and a constant envelope make MSK attractive [1].

This report will consider the MSK signaling scheme, and the primary focus will be on the design of a serial MSK (SMSK) modulator and demodulator (modem). This type of MSK was first described by Amoroso and Kivett [2].

CHAPTER II

DESCRIPTION OF MSK

MSK in General

It has been shown that MSK conceptually resembles OQPSK [1]. Instead of rectangular pulses modulating the in-phase and quadrature channels of a carrier as in OQPSK, sinusoidal pulses modulate the two channels in MSK. First, OQPSK will be reviewed; then, its relationship to MSK will be shown.

As shown in Figure 1, a binary bit stream at a rate of $\frac{1}{T}$ where T is the bit time, has been split into two binary bit streams: one containing only even bits, $b_i(t)$; and one containing only odd bits, $b_q(t)$. When the even bit stream is offset from the odd bit stream by T seconds and these offset bit streams, $b_{io}(t)$ and $b_{qo}(t)$, modulate the in-phase and quadrature channels of a carrier, the sum of the two modulated signals is OQPSK. Figure 2 illustrates this process. Now, if $b_{io}(t)$ and $b_{qo}(t)$ are shaped into sinusoidal pulses, as seen in Figure 3, then the resulting waveform at the output of the summer in Figure 2 will be MSK [1]. The mathematical description of MSK is then

$$s_{MSK}(t) = b_{io}(t)\cos(2\pi f_c t)\cos(\tfrac{\pi t}{2T}) + b_{qo}(t)\sin(2\pi f_c t)\sin(\tfrac{\pi t}{2T}) \qquad (1)$$

Recalling that

$$\cos\alpha\,\cos\beta = \tfrac{1}{2}\cos(\alpha-\beta) + \tfrac{1}{2}\cos(\alpha+\beta)$$

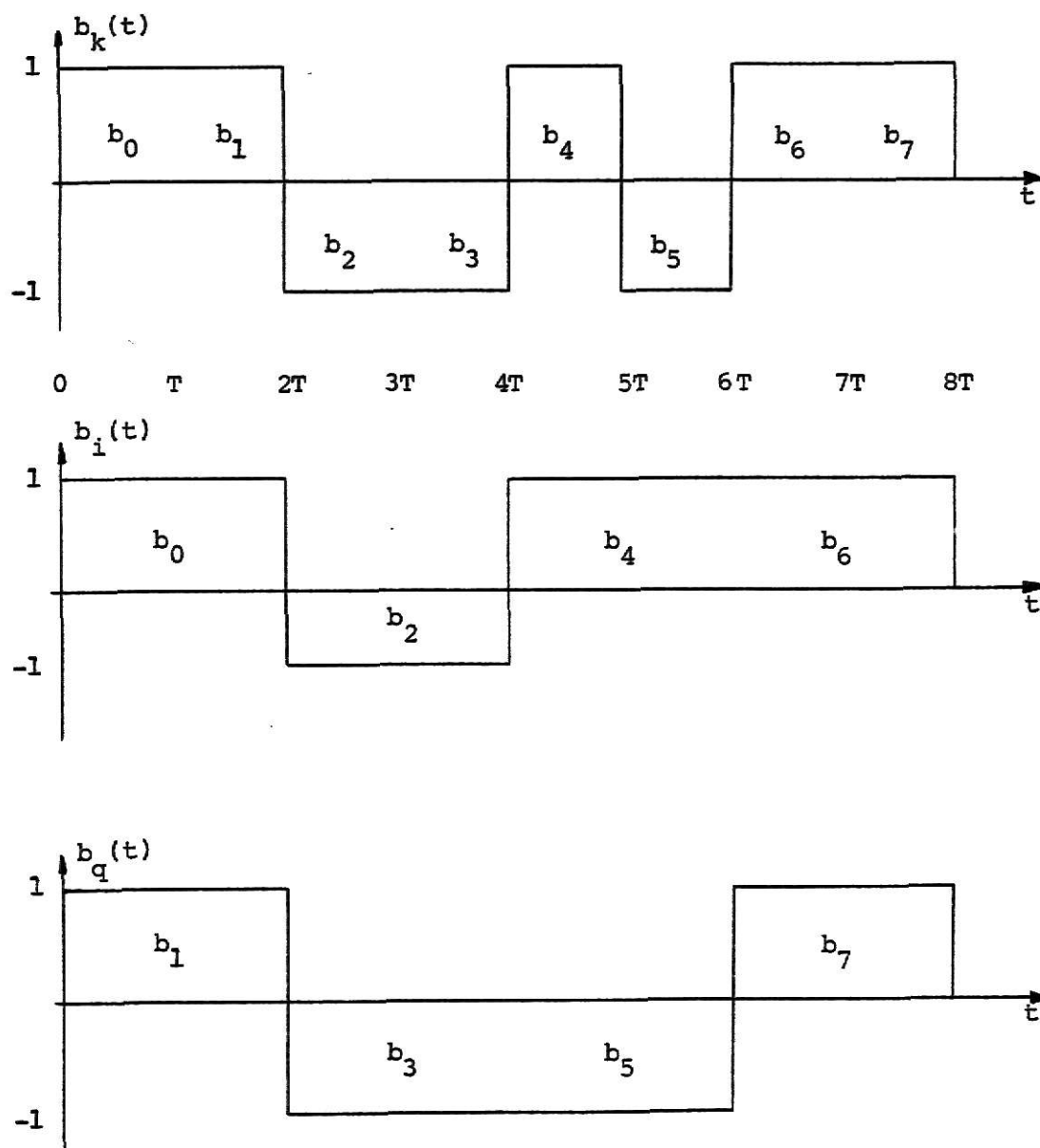$$\sin\alpha\,\sin\alpha = \tfrac{1}{2}\cos(\alpha-\beta) - \tfrac{1}{2}\cos(\alpha+\beta)$$

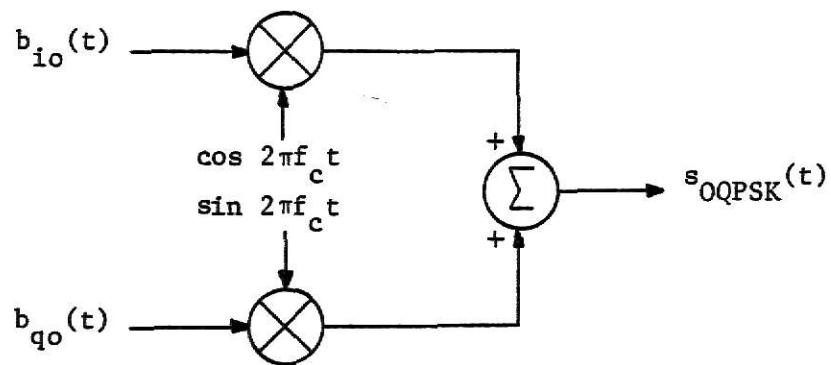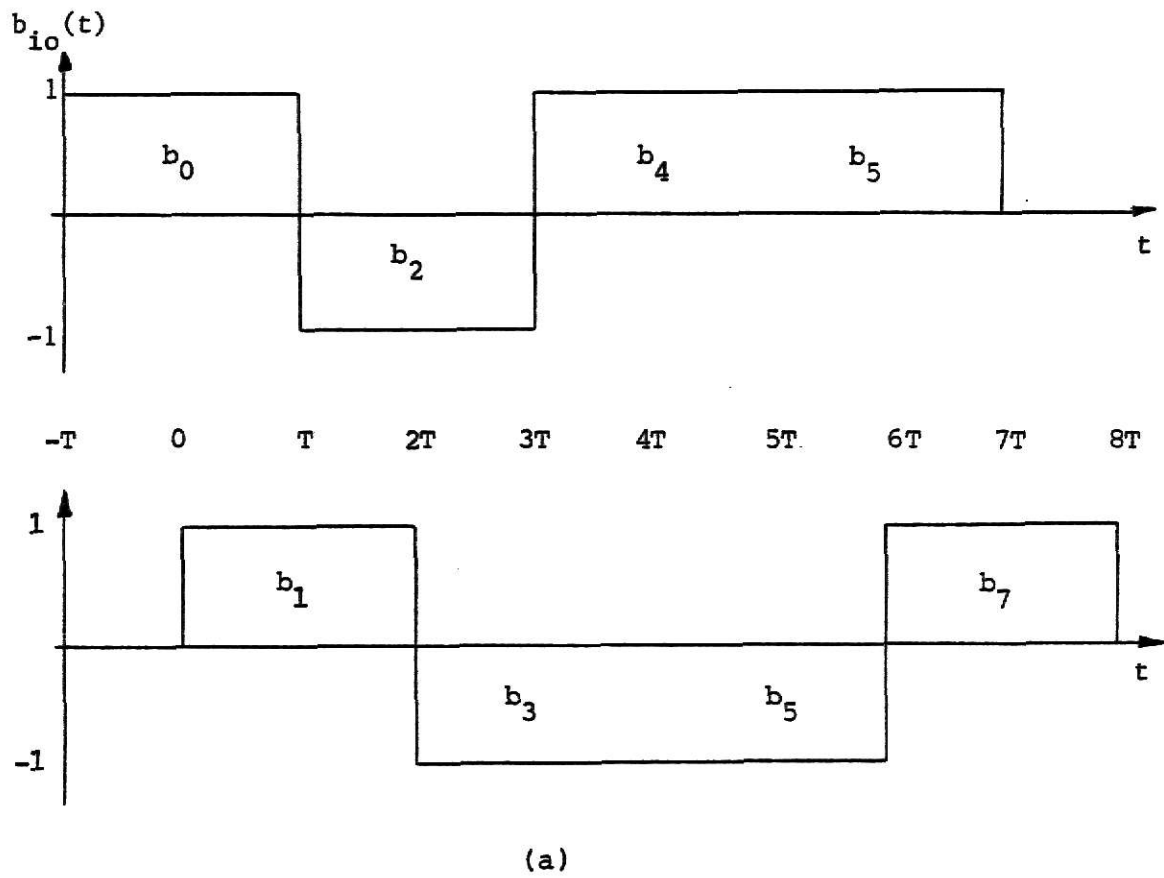Figure 1. Binary Bit Stream Split into Even and Odd Bit Streams.

(a)

Figure 2. (a) Offset Binary Bit Streams; (b) OQPSK Modulator.

then (1) becomes

$$s_{MSK}(t) = \frac{1}{2}b_{io}(t)\cos 2\pi(f_c - \frac{1}{4T})t + \frac{1}{2}b_{io}(t)\cos 2\pi(f_c + \frac{1}{4T})t$$

$$+ \frac{1}{2}b_{qo}(t)\cos 2\pi(f_c - \frac{1}{4T})t - \frac{1}{2}b_{qo}(t)\cos 2\pi(f_c - \frac{1}{4T})t \ .$$

For easier manipulation, define

$$\alpha = 2\pi(f_c - \frac{1}{4T})t, \ \beta = 2\pi(f_c + \frac{1}{4T})t.$$

Since $b_{io}(t)$ and $b_{qo}(t)$ can each take on values of 1 or -1, there are four cases to consider.

case 1: $b_{io}(t) = 1$, $b_{qo}(t) = 1$

$$\frac{1}{2}\cos\alpha + \frac{1}{2}\cos\beta + \frac{1}{2}\cos\alpha - \frac{1}{2}\cos\beta = \cos\alpha$$

case 2: $b_{io}(t) = 1$, $b_{qo}(t) = -1$

$$\frac{1}{2}\cos\alpha + \frac{1}{2}\cos\beta - \frac{1}{2}\cos\alpha + \frac{1}{2}\cos\beta = \cos\beta$$

case 3: $b_{io}(t) = -1$, $b_{qo}(t) = 1$

$$- \frac{1}{2}\cos\alpha - \frac{1}{2}\cos\beta + \frac{1}{2}\cos\alpha - \frac{1}{2}\cos\beta = -\cos\beta$$

case 4: $b_{io}(t) = -1$, $b_{qo}(t) = -1$

$$- \frac{1}{2}\cos\alpha - \frac{1}{2}\cos\beta - \frac{1}{2}\cos\alpha + \frac{1}{2}\cos\beta = -\cos\alpha$$

The results of these four cases generate information that allows simplification of (1). Note that $b_{io}(t)$ determines the sign of the signal, that is, when $b_{io}(t)$ is 1, the signal is positive, and when $b_{io}(t)$ is -1,

the signal is negative. Also observe that the product of $b_{io}(t)$ and $b_{qo}(t)$ determines the argument of the resulting cosine term. Thus (1) becomes

$$s_{MSK}(t) = b_{io}(t) \cos 2\pi (f_c - \frac{b_{io}(t) \, b_{qo}(t)}{4T}) t. \tag{2}$$

Equation (2) shows that when a mark is sent, the resulting frequency is $f_c - \frac{1}{4T}$, and when a space is sent, the resulting frequency is $f_c + \frac{1}{4T}$. In other words, MSK represents a special case of FSK where the frequency deviation is exactly $\frac{1}{2T}$. The necessary constraints for MSK are therefore

$$f_1 = \frac{n}{2T} \quad , \quad \text{mark}$$

$$f_2 = \frac{n+1}{2T} \quad , \quad \text{space} \tag{3}$$

$$f_c = \frac{(2n+1)}{4T}, \quad \text{carrier frequency}$$

where n denotes the number of half-cycles in a keying interval. Figure 3e shows the MSK waveform for n = 2. Note the continuous phase of the MSK signal as well as its constant envelope.

The normalized power spectral density of MSK is given by

$$G_{MSK}(f) = \frac{16}{\pi^2} (\frac{\cos 2\pi fT}{1 - 16f^2T^2})^2 \tag{4}$$

where f is the offset from the carrier [3]. The normalized MSK amplitude spectrum is then

$$\left| S_{MSK}(f) \right| = \left| \frac{4}{\pi} \frac{\cos 2\pi ft}{(1 - 16f^2T^2)} \right| \tag{5}$$

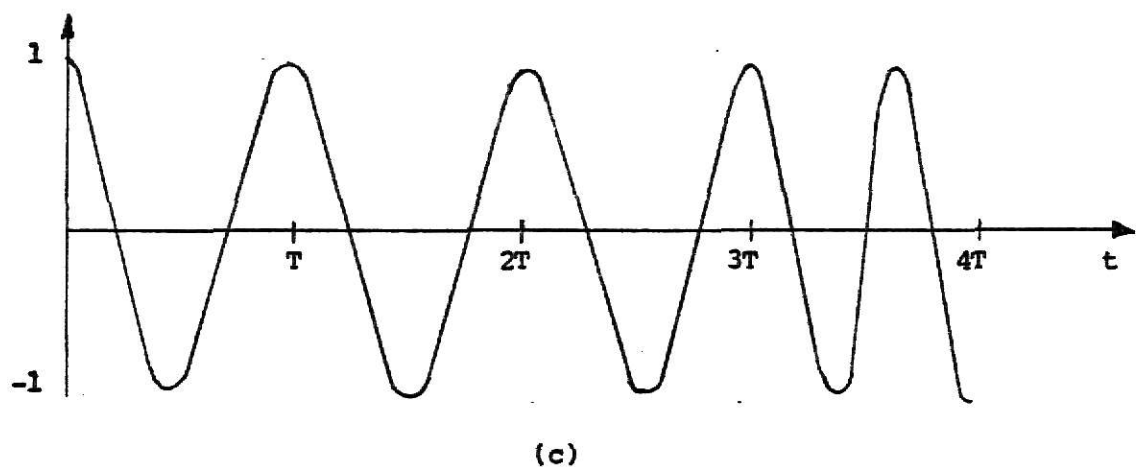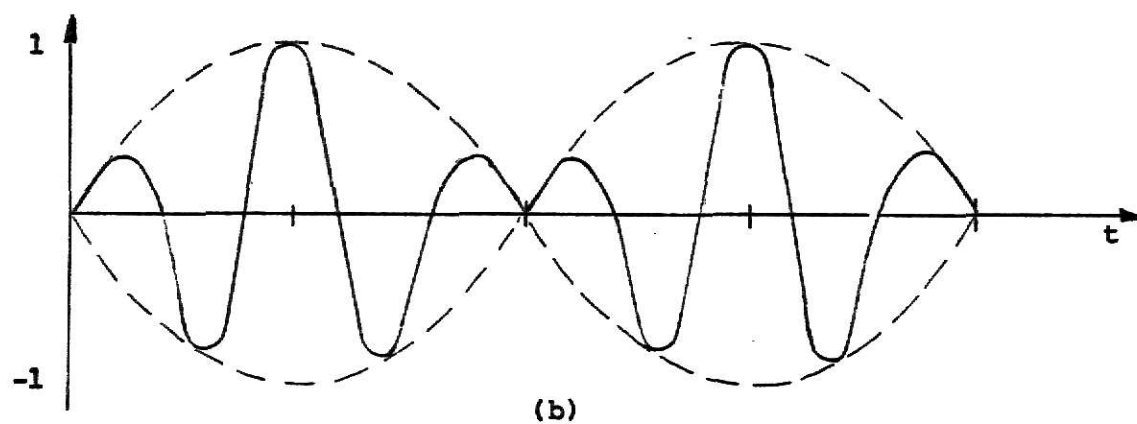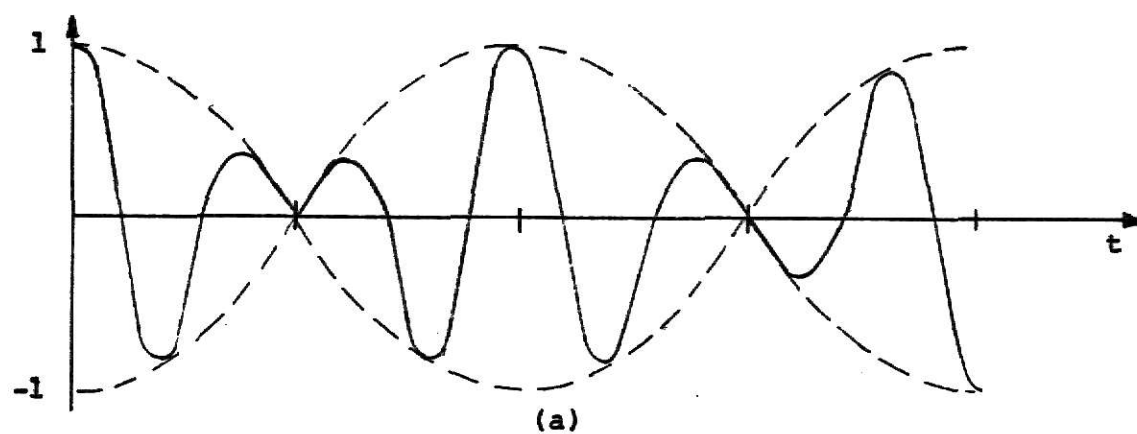A sketch of this spectrum can be found in Figure 4.

Figure 7. (a) In-phase Data Pulses.
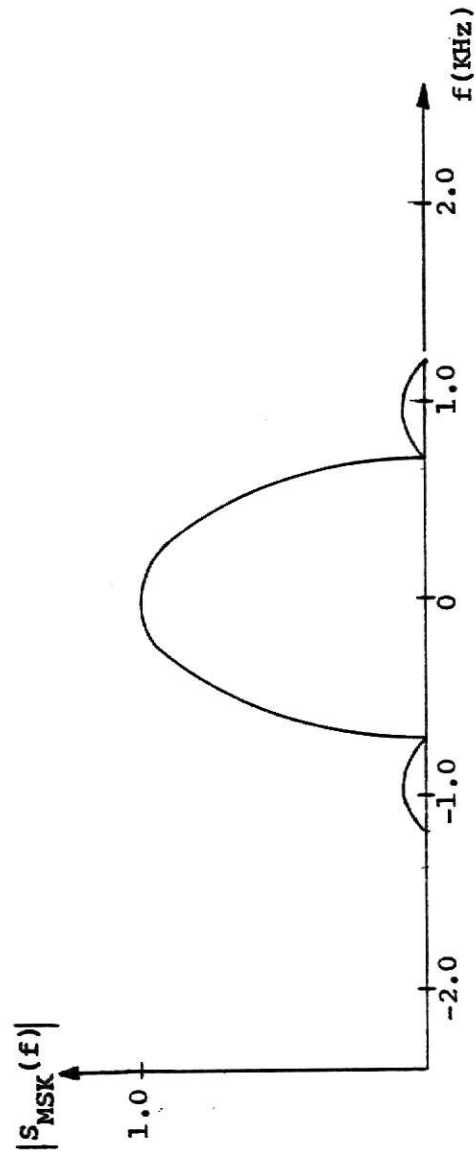(b) Quadrature Data Pulses.
(c) MSK Waveform.

Figure 4. MSK Amplitude Spectrum (normalized frequency).

Serial MSK

As mentioned previously, this report will be concerned with the design of a SMSK modem a description of which will be found in Chapter 3. The following describes the concepts of SMSK signaling.

It has been shown that MSK can be generated by filtering a 2ϕ - PSK signal so that the result is MSK [2]. This method of generating MSK, simpler than the previous method, is called serial MSK. The block diagram in Figure 5 shows the simplicity of a SMSK modulator and demodulator.

The SMSK modulator operates in the following fashion. The binary bit stream modulates the carrier. so that the zero-crossings of the data correspond to the peak voltage of the oscillator. This operation defines 2ϕ - PSK, and the signal contains n half-cycles of f_1, the mark frequency, that occur during each keying interval T. The 2ϕ - PSK signal is then filtered using a filter which has an impulse response h(t) that is a contant envelope of n + 1 half-cycles of f_2 of duration T. Thus, the response of h(t) to the 2ϕ - PSK signal is the SMSK signal. That is,

$$s_{MSK}(t) = s_{PSK}(t)*h(t)$$

where

$$s_{PSK}(t) = \begin{cases} b_k(t)\sin(2\pi f_1 t+\phi) = b_k(t)\sin(\frac{n\pi t}{T} + \phi), & kT \leq t \leq (k+1)T \\ 0 & , \text{ elsewhere.} \end{cases} \qquad (6)$$
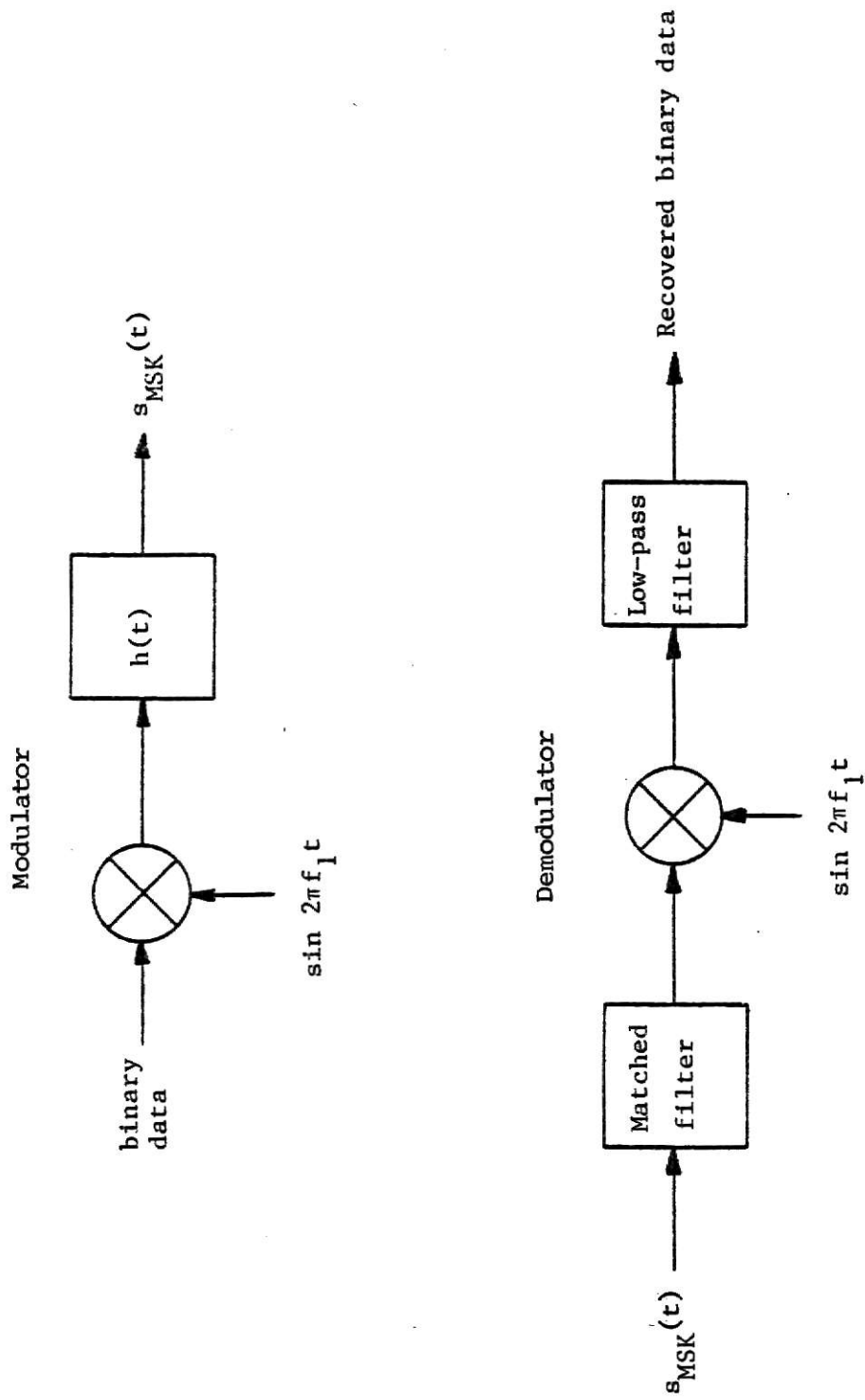
Figure 5. Block Diagram of SMSK Modulator and Demodulator

and

$$h(t) = \begin{cases} \sin 2\pi f_2 t = \sin \dfrac{\pi(n + 1)t}{T} \ , & 0 \le t \le T \\ 0 & , \ \text{elsewhere.} \end{cases} \qquad (7)$$

The $b_k(t)$ represent the data and ϕ denotes the relative phase between f_1 and the data transmissions [2].

In order to see the development of the SMSK amplitude spectrum, it may be more desirable to view the frequency domain representations of $s_{PSK}(t)$ and $h(t)$. For $s_{PSK}(t)$, $\pm \sin 2\pi f_1 t$ is sent. For the interval $[0,T]$, the output of the 2ϕ – PSK modulator is a pulse with transform

$$P(f) = \frac{T \sin \pi fT}{\pi fT} \, e^{-j\pi fT/2} \qquad \text{where } p(t) = \begin{cases} 1, & 0 \le t \le T \\ 0, & \text{elsewhere.} \end{cases}$$

Use of the modulation theorem yields the following amplitude spectrum for $s_{PSK}(t)$

$$\left| s_{PSK}(f) \right| = \left| \frac{1}{2} P(f - f_1) - P(f + f_1) \right|.$$

The transform of $h(t)$ is found in the same way; so,

$$\left| H(f) \right| = \left| \frac{1}{2} P(f - f_2) - P(f + f_2) \right|$$

hence, the MSK amplitude spectrum is given by

$$\left| S_{MSK}(f) \right| = \left| S_{PSK}(f) \right| \left| H(f) \right|$$

or

$$\left| S_{MSK}(f) \right| = \left| \frac{1}{4} P(f - f_1) - P(f + f_1) \quad P(f - f_2) - P(f + f_2) \right|.$$

Figure 6a shows $\left|S_{PSK}(f)\right|$ and $\left|H(f)\right|$. Note that if f_1 and f_2 are separated by $\frac{1}{2T}$, then the resulting spectrum in Figure 6b matches the MSK amplitude spectrum in Figure 4.

The SMSK demodulator is shown in Figure 5. This demodulator utilizes an input filter matched to the SMSK signal, followed by a product detector and an integrate and dump [2]. It has been found that this configuration is one form of the optimum demodulator for SMSK [4].
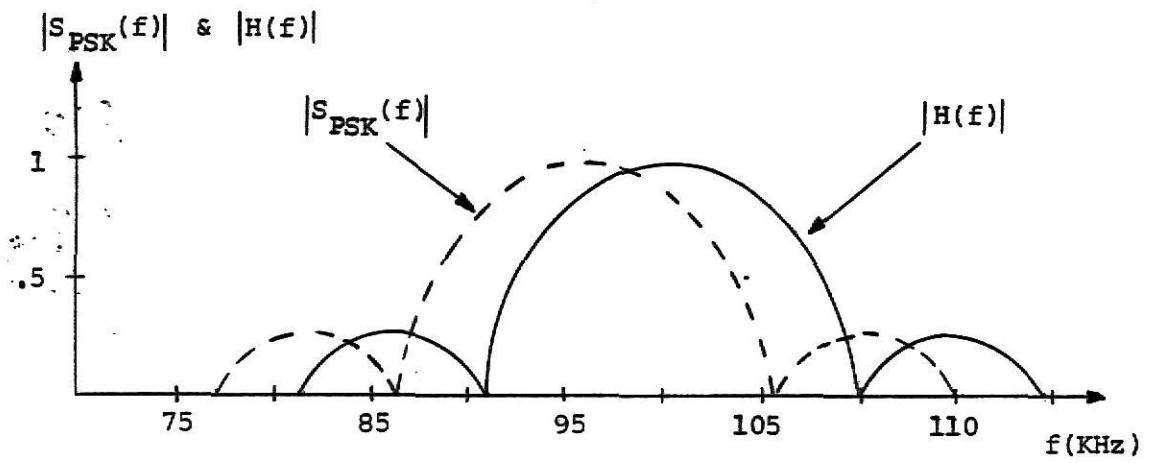
(a)
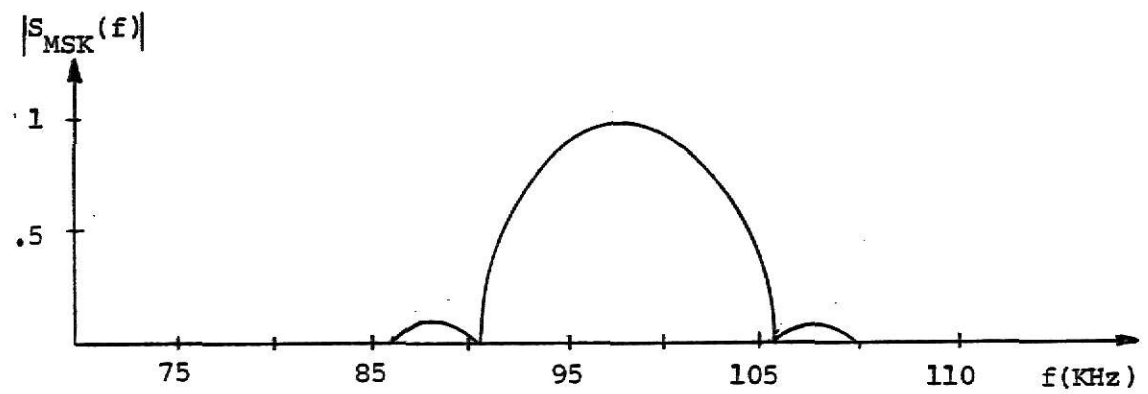
(b)

Figure 6. (a) Amplitude Spectrum of Biphase PSK and H(f);
(b) SMSK Amplitude Spectrum.

CHAPTER III

DESCRIPTION OF THE MODEM

The following description details the design of a SMSK modem in
order to experimentally validate theoretical aspects of SMSK. The block
diagram of the modem can be seen in Figure 7. This modem is suboptimal
because a filter with the required impulse response could not be realized
exactly. Instead, it was approximated with a single pole bandpass filter.

All of the circuits were configured for a data rate of 9.6 Kbps,
n=20, and a carrier frequency of 98.4 KHz. Because of the available
equipment and the desire for simple construction, all of the circuits
were built on EL breadboards.

Modulator

The SMSK modulator can be realized by generating a 2ϕ - PSK signal
and then filtering the signal in the way described in Chapter 2. The
circuit diagram of the modulator can be seen in Figure 8.

2ϕ - PSK

The 2ϕ - PSK signal can be generated by any device that will switch
the phase of f_1 by $\pm 180^{\circ}$ with respect to the incoming binary data. The
Motorola MC1496 Balanced Modulator integrated circuit easily serves this
purpose [5]. The IC is configured as a double side-band (DSB) modulator
since 2ϕ - PSK represents the digital equivalent of DSB. Aside from the
typical biasing scheme of the IC, nothing out of the ordinary has been
done with the exception of nulling the carrier at frequency f_1 by adjusting
the voltage at pin 4. With this arrangement, the carrier (f_1) has been
nulled better than 40 dB below the first sidebands, an acceptable level.
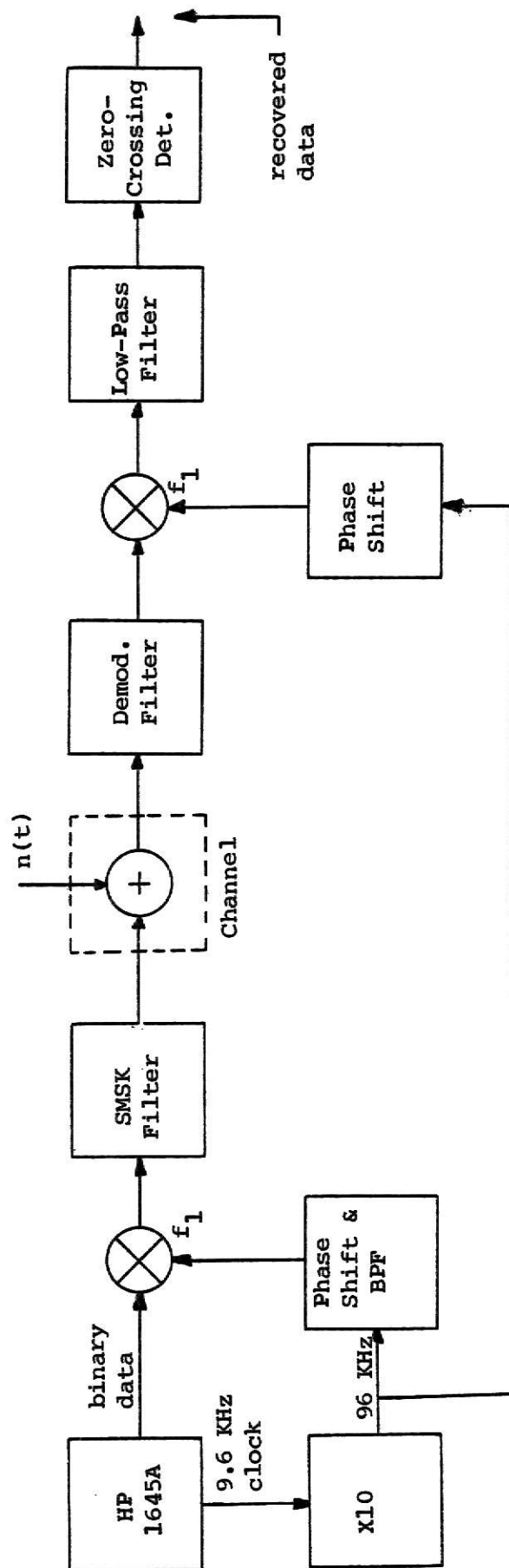
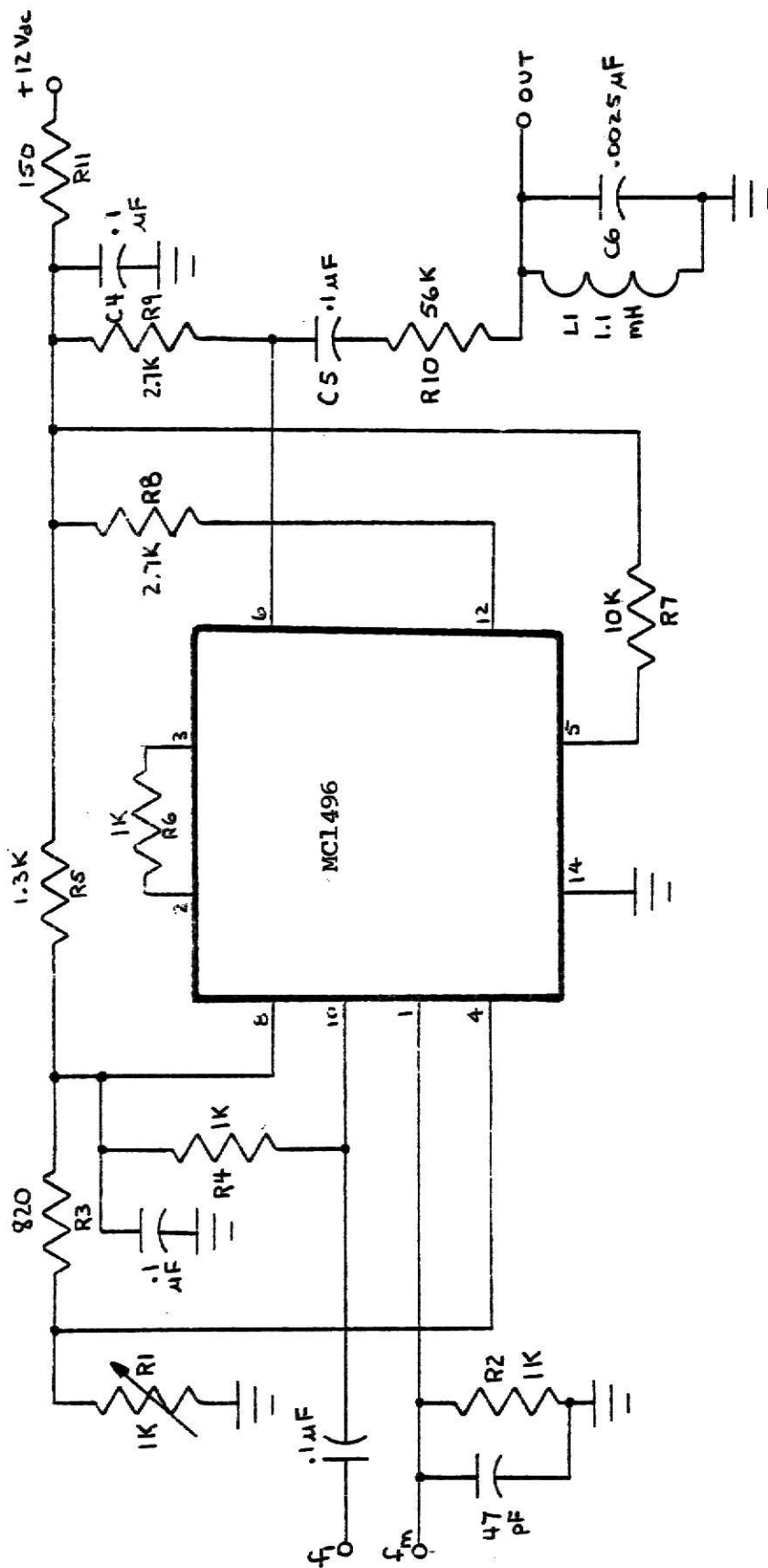Figure 7. Block Diagram of Experimental SMSK Modem.

16

Figure 8. SMSK Modulator Circuit.

The f_1 input is at 50 mVrms, and the modulating binary bit stream is at TTL levels.

MSK Filter

Synthesis of the filter with impulse response h(t) given in (7) cannot be easily achieved at any frequency because of its shape as shown in Figure 6b. At frequencies in the UHF region and higher, surface acoustic wave techniques can be used to closely approximate the impulse response of the filter. At frequencies in the vicinity of 100 KHz, however, resistors, inductors, and capacitors are best used. Active filters were also tried, but because they did not possess the necessary Q, they were abandoned

Inspection of Figure 6b, which shows the amplitude spectrum of MSK, indicates that the lower notch of the MSK spectrum coincides with the lower notch of the ideal SMSK filter, and its upper notch results from the upper notch of the PSK spectrum. Three approaches to synthesizing the filter were tried. These approaches included a notch filter tuned to the lower notch of the MSK spectrum followed by a low-pass filter; two cascaded notch filters with one tuned to the lower notch and the other tuned to the upper notch; and a bandpass filter. The first two approaches were not acceptable because the notch depths were only on the order of -6 dB. The shallow notch depths resulted from low inductor Q. However, acquisition of a Ferroxcube 2616 PA 600 pot core allowed the construction of a 1.1 mH inductor with a Q of 300 [6]. With the new inductor, the bandpass filter (BPF) approach was then tried. The bandwidth of the BPF was chosen to be the 3 dB bandwidth of the $\frac{\sin x}{x}$ function which corresponds to a bandwidth of 2.7 KHz at a center frequency of $f_2 = 100.8$ KHz,

Referring to Figure 8, the filter which consists of R10, L1, and C6, can be seen at the output of the MC1496 at pin 6.

As previously stated, difficulty in achieving the impulse response h(t) prevents the construction of an optimum SMSK modem. With that in mind, this system is a form of suboptimum SMSK.

Demodulator

Refer again to the demodulator block diagram for SMSK shown in Figure 5. It is assumed that the modem is coherent, and three items make up the demodulator: a matched filter, a product detector, and an integrate and dump. The circuit diagram of the SMSK demodulator can be found in Figure 9.

Matched Filter

In order to construct an optimum SMSK demodulator, the receiver filter must be matched to the SMSK signal. The same problems encountered in synthesizing the modulator filter exist with the matched filter as well. In light of that, the same filter used as the modulator filter will serve as the matched filter. Because the filter has an input resistance of 56 KΩ and it is connected to the 10 KΩ input of the product detector, an impedance transformation must be made. The transformation is effected with C2 and C3 which also serve to tune the filter to 100.8 KHz. Small value capacitors placed in parallel with C2 adjust the filter to the desired center frequency. The amplitude response of this filter is shown in Figure 10.

Product Detector

Again, the MC1496 is used, but this time it functions as a product detector [5]. As a product detector the MC1496 does not need a sinusoidal reference at frequency f_1; in fact a square wave will suffice. This means that the output of the X10 multiplier does not need to be filtered. The magnitude
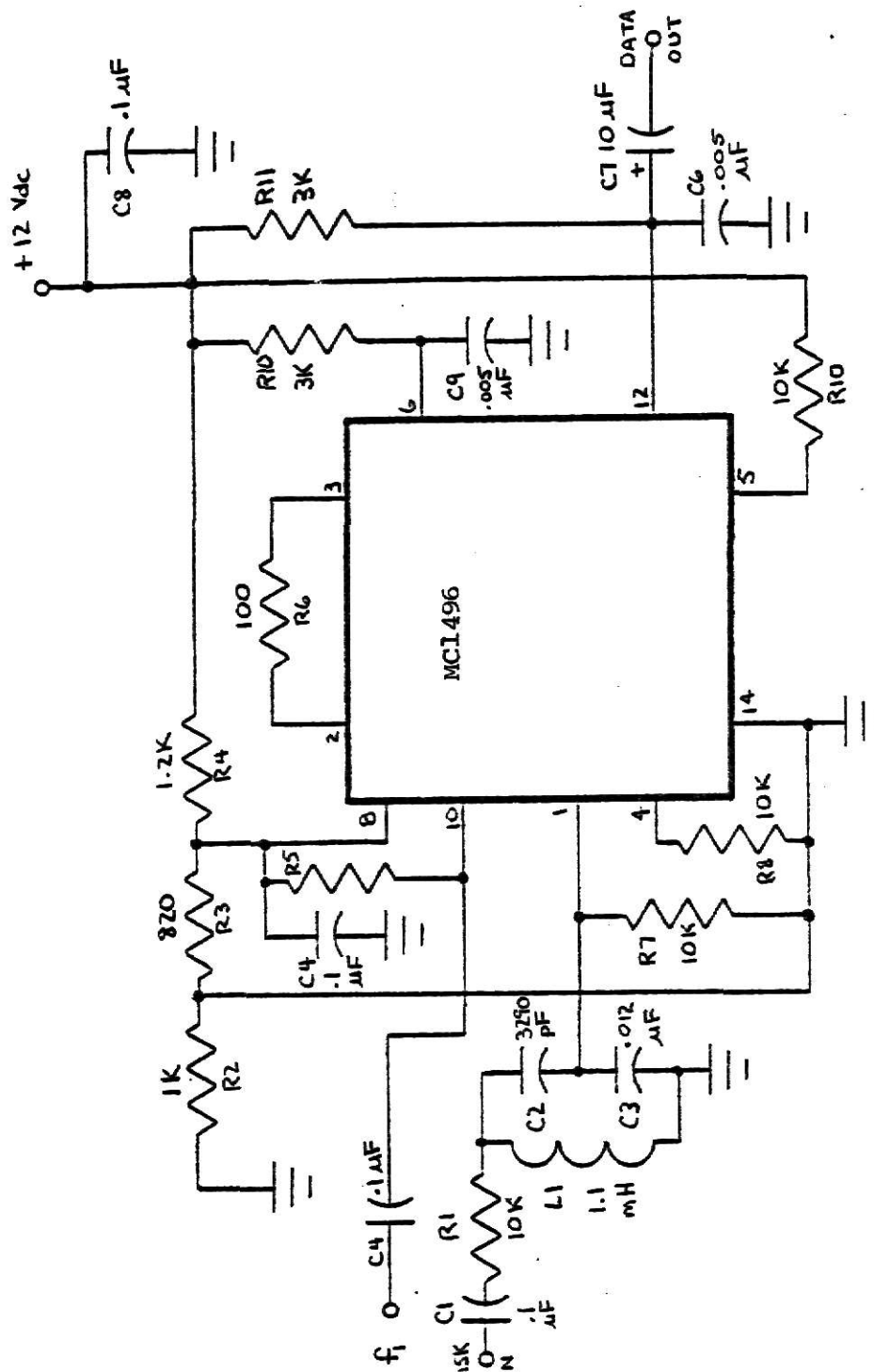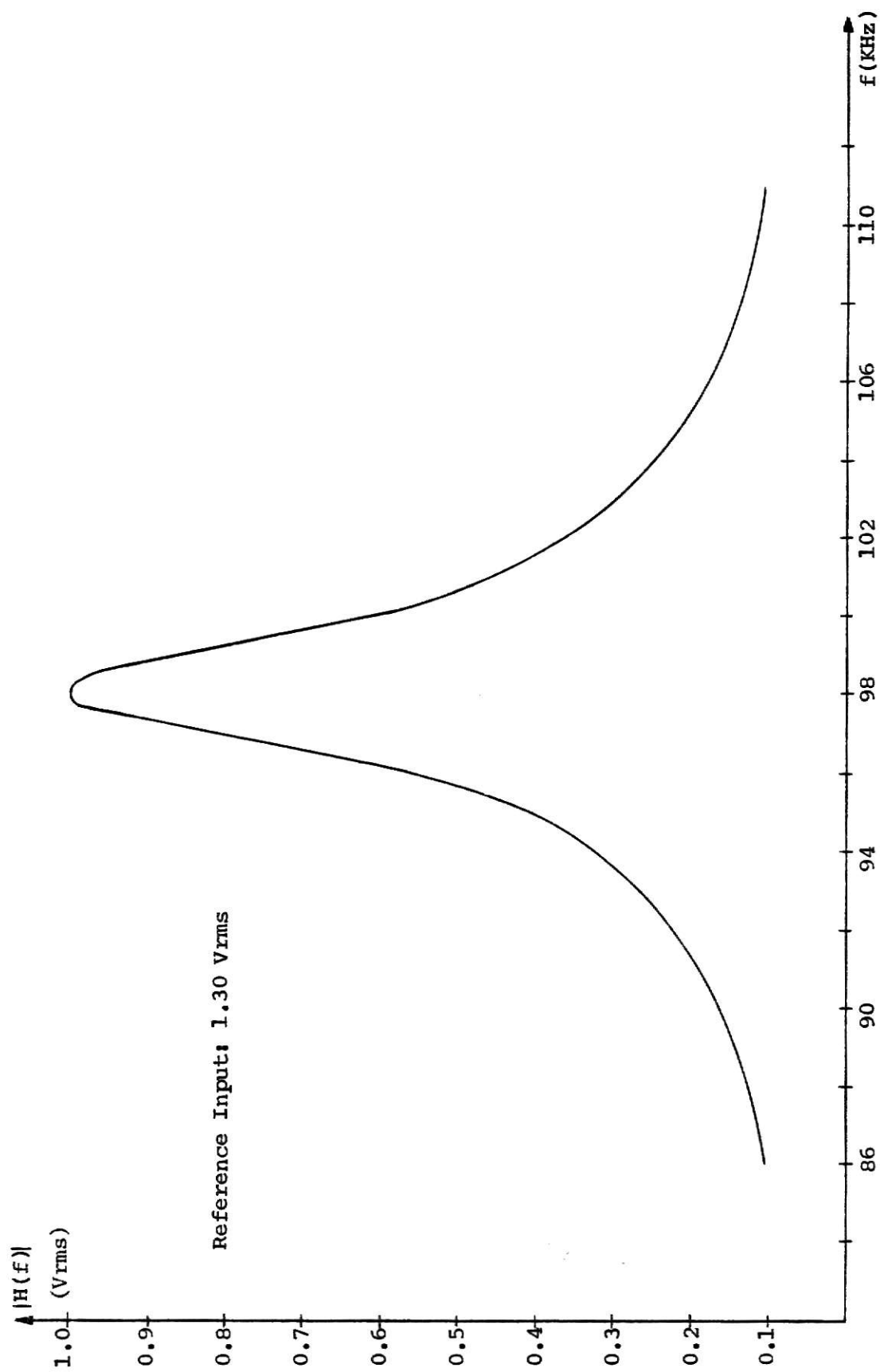
Figure 9. SMSK Demodulator Circuit.

Figure 10. Amplitude Response of Suboptimum SMSK Filter.

of the f_1 input is about 60 mVrms.

Integrate and Dump

Instead of using an integrate and dump, it is simpler to use a simple low-pass filter with a cut-off frequency set at the data rate of 9.6 kbps. This filter, consisting of R11 and C6, can be seen at pin 12 of the MC1496. Some sacrifice in performance is expected to occur with this compromise.

The Channel

In order to simulate the effects of the channel on SMSK, a summing amplifier was constructed, and it can be found in Figure 11. Because of the loss in the demodulator filter, it is necessary to amplify the signal plus noise in order for the demodulator to work properly. The noise is generated from a Gaussian noise generator with a bandwidth of 500 KHz.

Support Circuitry

The Hewlett-Packard HP-1645A Data Error Analyzer serves as the heart of the support circuitry. Not only does it provide the pseudo-random binary data to test the modem, but it also provides an external clock signal that is synchronous with the binary data. The clock signal is then frequency multiplied in order to get a synchronous frequency f_1 that is exactly 10 times the data rate.

X10 Multiplier

Phase-locked loop (PLL) frequency synthesis provides a simple technique for frequency multiplication. For details of the PLL multiplier refer to Figure 12. In order to achieve an f_1 that is 10 times the data rate, N equals 10. The PLL can be easily constructed using Motorola's MC4044 phase detector IC and the MC4024 voltage controlled oscillator (VCO) IC, and a 7490 divide by 10 counter IC. All of these devices are TTL compatible which makes interfacing to the HP-1645A TTL outputs simple.
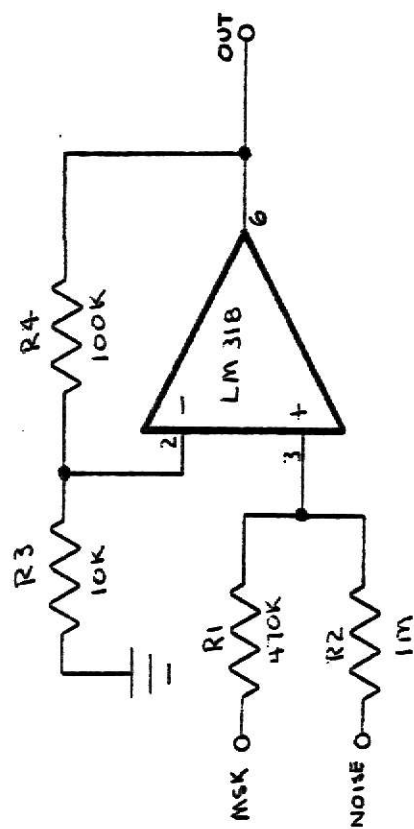
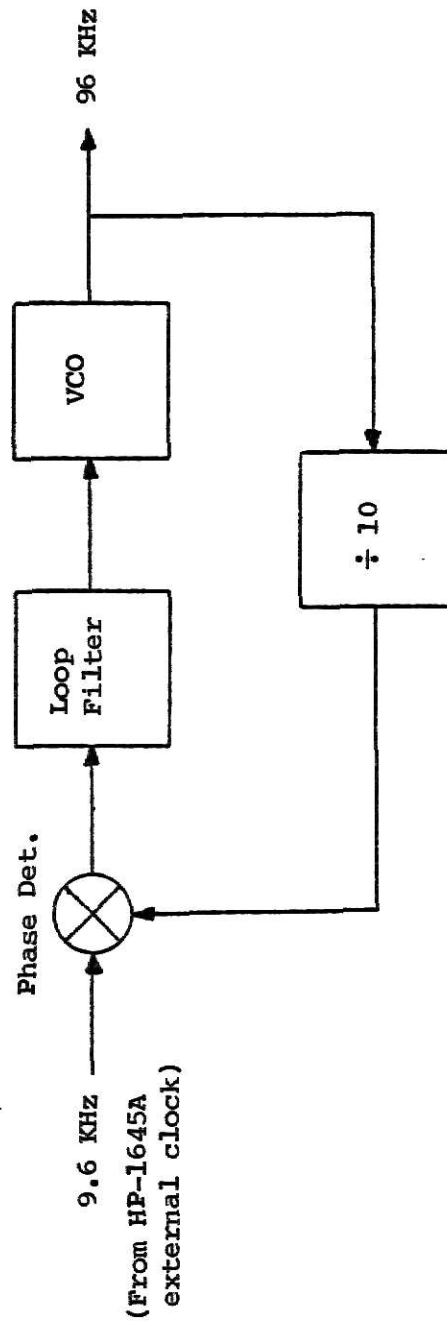Figure 11. Summing Amplifier Used as the Channel

Figure 12. Block Diagram of Phase-Locked Loop Frequency Multiplier.

The circuit diagram for the X10 multiplier, as seen in Figure 13, shows the PLL as described in the Motorola PLL Handbook [7]. The loop filter, consisting of R1, R2, and C2, can be seen at pins, 8, 9, and 10 of the MC4044. The loop filter is designed for an ω_n = 1 KHz and ζ = 0.707. To ensure the loop has sufficient gain, the optional amplifier internal to the MC4044 was used.

The VCO operated at a frequency close to 96.0 KHz in order to make the output of the PLL 96.0 KHz. The MC4024 only needs one capacitor to determine its operating frequency, and this is done so that the VCO operates in the center of its control range [7].

To complete the X10 multiplier, a 7490 is used as the divide by ten counter. As a result, the 9.6 KHz input becomes a 96.0 KHz square wave at the PLL output.

Phase Shifter

To make the modem coherent with the data, phase shifting circuits must be built in order to compensate for phase shifts that occur in the modem or the channel. The phase shifter shown in Figure 14, is used at the f_1 input of the SMSK modulator and product detector. The LM339 quad comparator, with a variable resistor and a fixed capacitor functions as the phase shifter. Each stage can provide $0^o - 90^o$ phase shift; since it is desirable to have a $0^o - 180^o$ phase shift, two stages are used. The stages are isolated from one another by using one of the comparators in the LM339 as a voltage follower. The circuit in Figure 14 represents the circuit used at the f_1 input of the modulator; whereas, the one used at the product detector includes a voltage follower preceeding the first stage so that the phase shifter will not load the output of the channel summing amplifier.
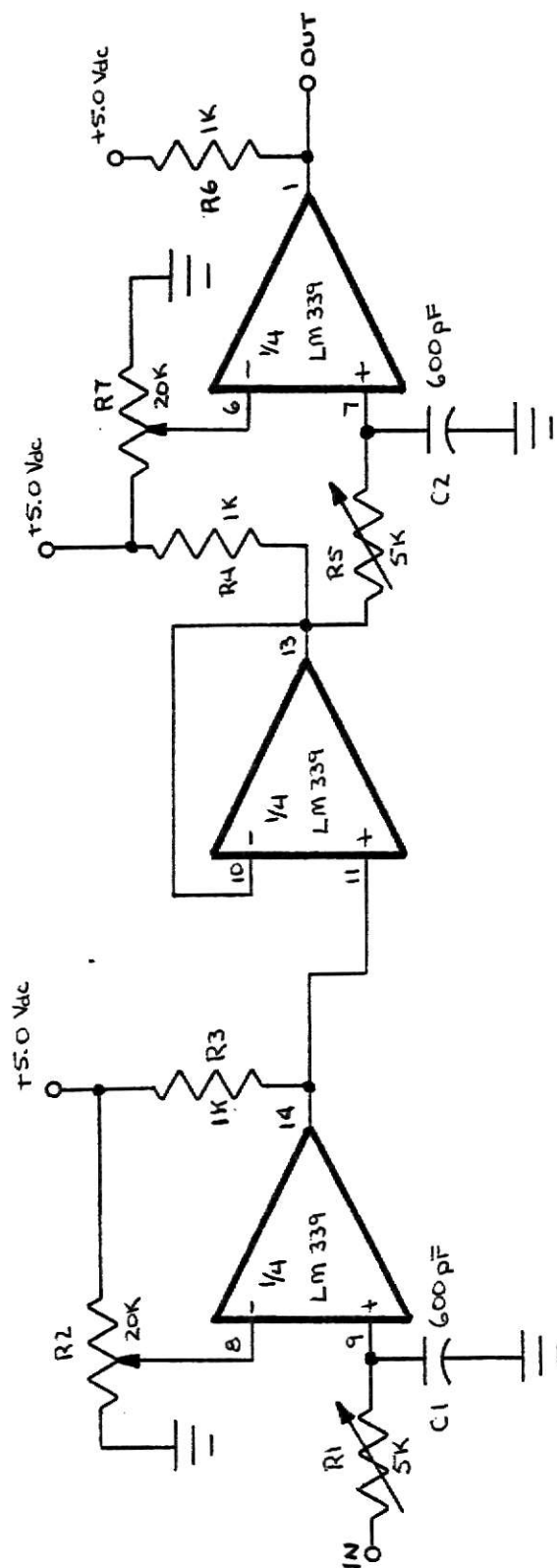
Figure 13. Frequency Multiplier Circuit.

Figure 14. Phase Shifter Circuit.

Bandpass Filter

The SMSK modulator needs a sinusoidal carrier input at frequency f_1 so that the 2ϕ - PSK signal can be generated. For that reason, a bandpass filter, including an 8 to 1 impedance transformation is used at the output of the phase-shifter so that a 96.0 KHz sinusoidal reference signal is available for the MC1496 modulator circuit. The circuit for this filter can be seen in Figure 15.

Zero-Crossing Detector

The output of the demodulator low-pass filter is not TTL compatible so it can not be directly connected to the input of the HP-1645A Error Analysis. Since the signal at the low-pass filter is symmetrical about ground potential, a zero-crossing detector (ZCD) can serve to make the output of the demodulator TTL compatible. The circuit for the ZCD is shown in Figure 16. The LM318 operational amplifier, functioning as a ZCD, amplifies the demodulator output so that it can be input to the LM339 ZCD. The output of the LM339 represents the recovered binary data at TTL levels.
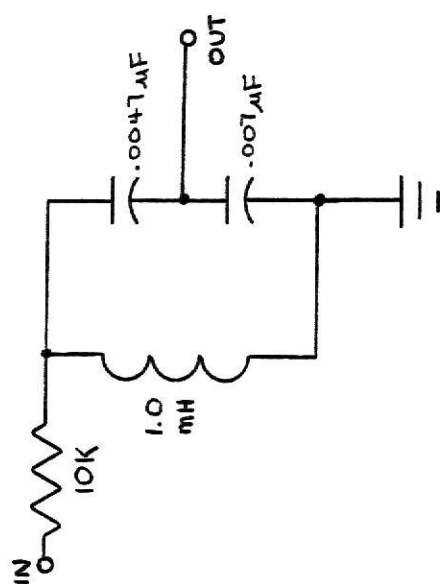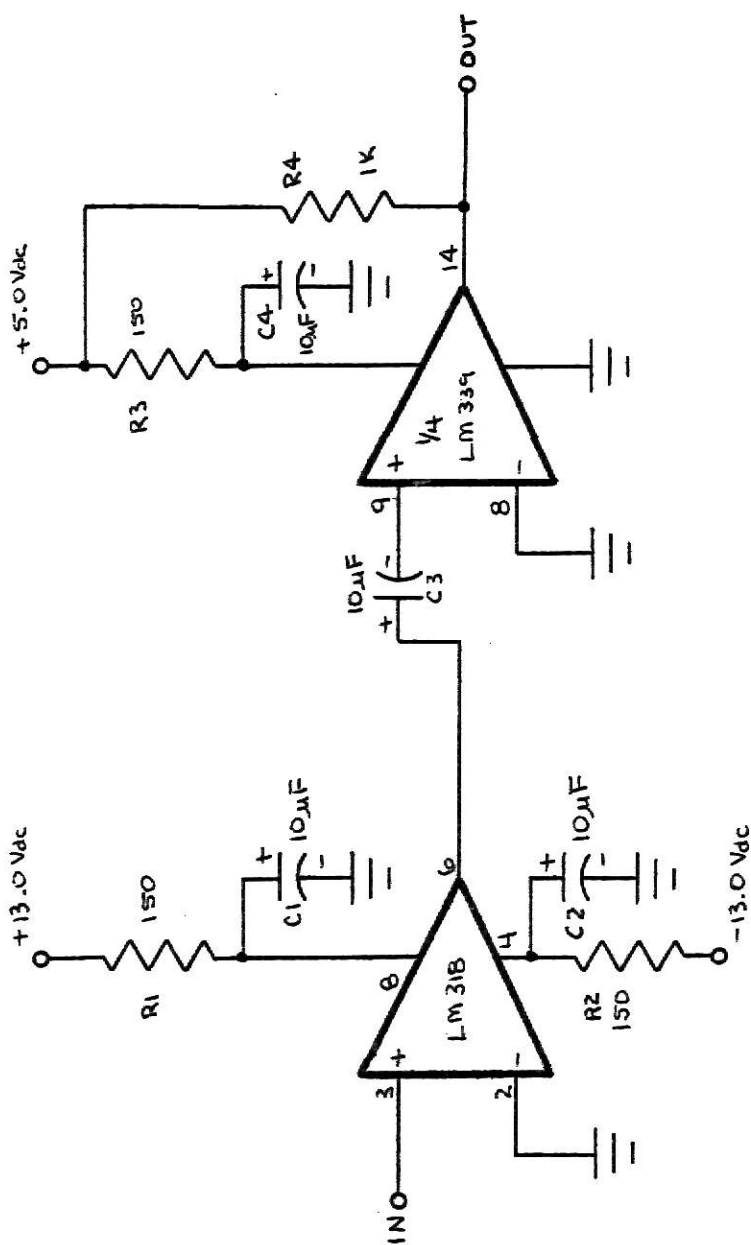
Figure 15. Bandpass Filter Circuit

Figure 16. Zero-Crossing Detector Circuit.

CHAPTER IV

PERFORMANCE OF THE MODEM

Envelope

The picture in Figure 17a shows the envelope of the suboptimum SMSK modulator output when modulated with a 101010... bit pattern. Observe that there is approximately a 6 dB variation in the envelope as a result of the suboptimum filter used in the modulator. A computer analysis of the SMSK envelope **verifies** the experimental observation of the approximate 6 dB variation; this is shown in Figure 18.
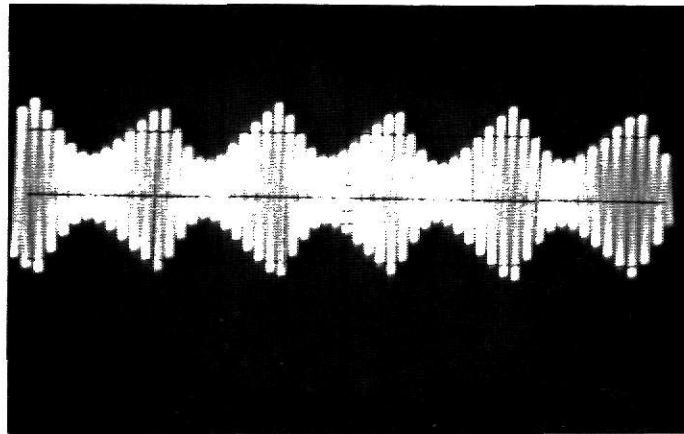
Power Spectrum

A photograph of the actual suboptimum SMSK power spectrum can be seen in Figure 17b, and Figure 19 shows the calculated power spectrum for suboptimum SMSK. Comparison of these two figures reveals several strong similarities. Both figures show that the first nulls occur approximately 20 KHz apart and the remainder of the nulls are approximately 10 KHz apart. Also note that the assymmetrical shape of the actual spectrum strongly resembles the shape of the calculated spectrum.

It is also interesting to make a comparison between the ideal and suboptimum SMSK power spectra in Figure 19. Notice that the out-of-band power of the suboptimum spectrum is slightly greater than that of the ideal spectrum. Also observe that the side-lobes of the suboptimum spectrum are twice as wide as those of the ideal spectrum.

Bit Error Performance

Because of time constraints, no experimental bit error rate (BER) data were obtained. However, Figure 20 shows an analytical comparison

30

(a)
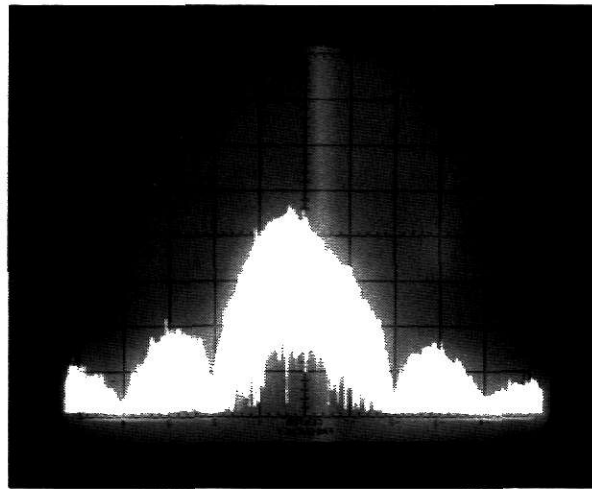
(b)

Figure 17. (a) Suboptimum SMSK Envelope
            (b) Power Spectrum of Suboptimum SMSK Spectrum.
                Horizontal Scale: 5KHz/div.; Vertical
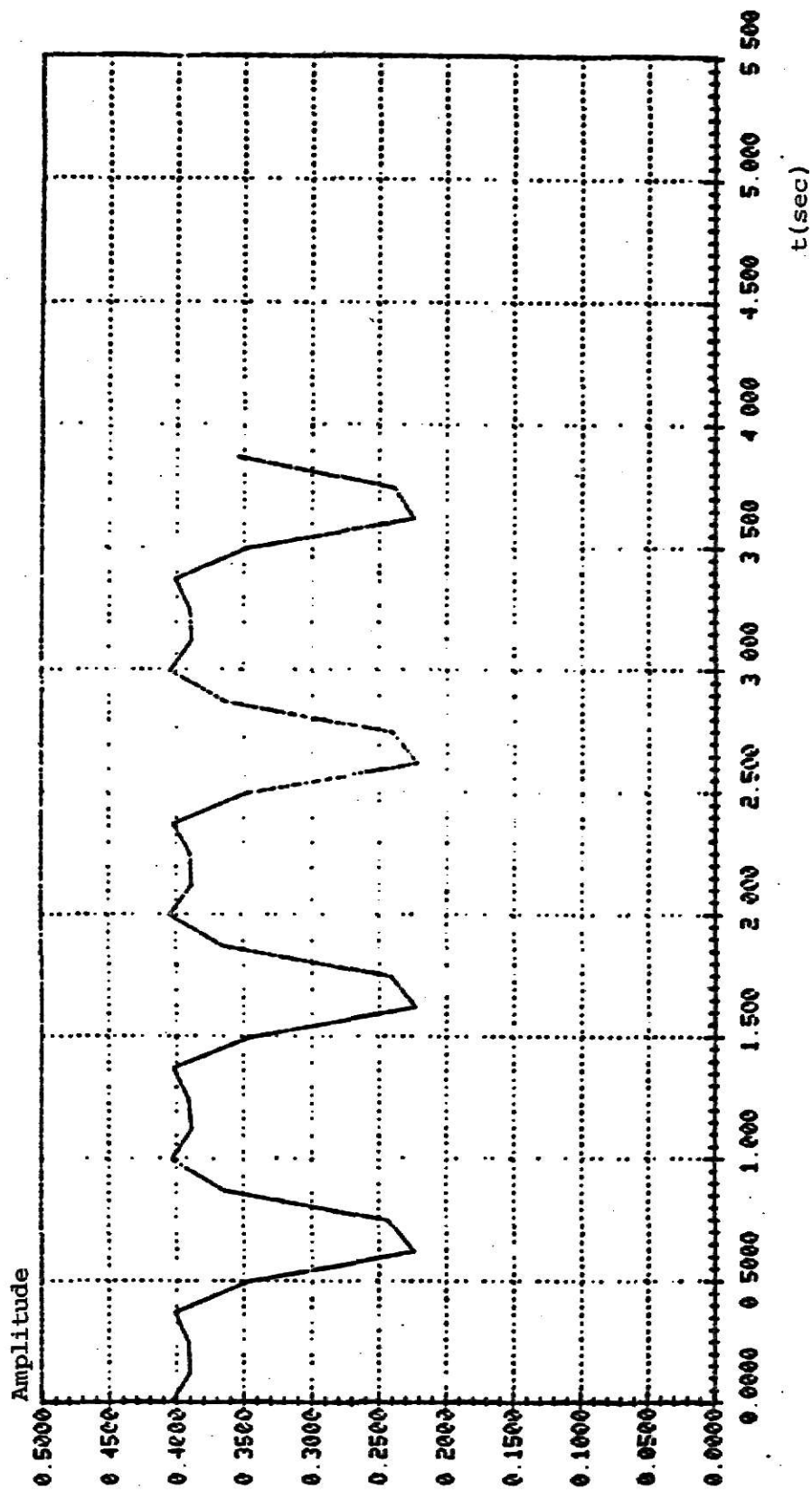   Scale: 10 dB/div.
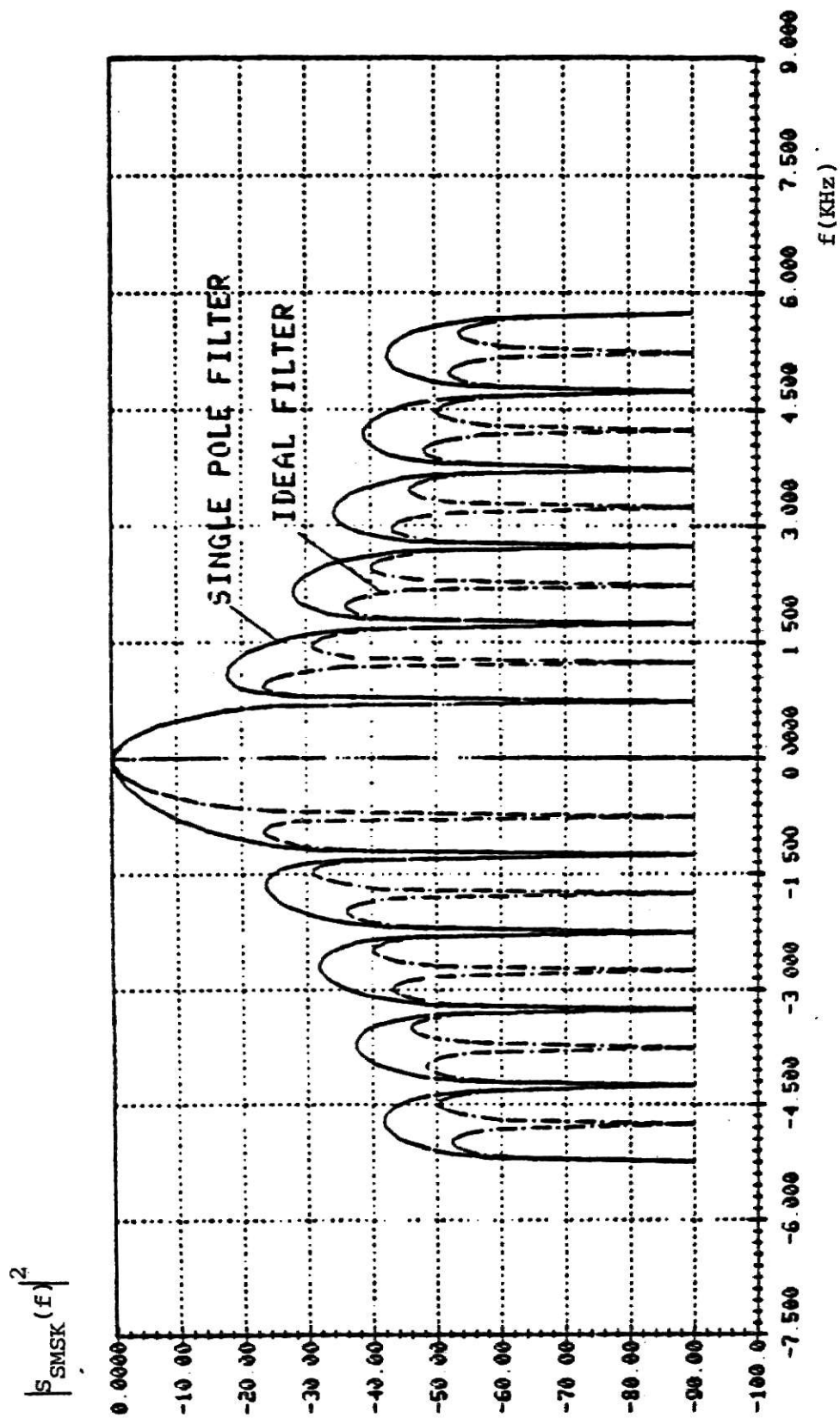
Figure 18. Calculated Suboptimum SMSK Envelope.

Figure 19. Calculated Suboptimum SMSK Power Spectrum (normalized frequency).

of the BER performance between ideal and suboptimum SMSK. It is not surprising that the two curves are identical because both schemes employ antipodal signaling and matched filter detection.
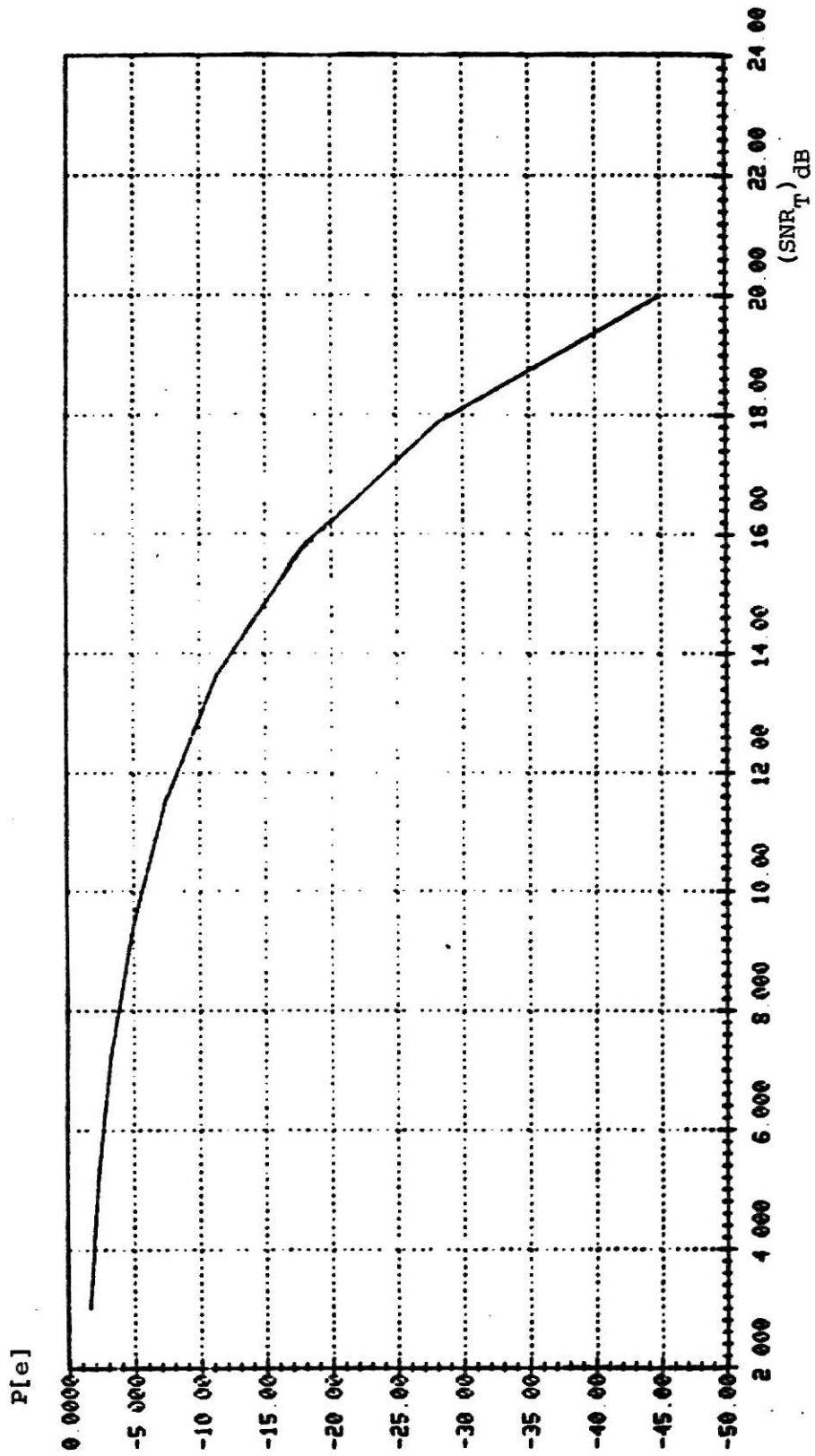
Figure 20. Bit Error Rate Curve for Ideal and Suboptimum SMSK.

CHAPTER V

CONCLUSIONS

SMSK represents a simple way of generating MSK, and the emphasis of this report was to design, construct, and evaluate a SMSK modem. It was found that the construction of an optimum SMSK system was complicated by the difficulty in synthesizing an ideal SMSK filter. The ideal filter was approximated with a single pole bandpass filter. This approach represents a simple form of suboptimum SMSK. Evaluation of the suboptimum SMSK modem included observation of the modulator output in the time domain and its power spectrum, and an analytical comparison between the BER performance between ideal and suboptimum SMSK.

In this report, the simplest possible filter has been considered, and it has been determined that in many respects the design of the SMSK filter is not particularly critical. The most significant shortcoming was the envelope variation which occurred with the imperfect filter. An encouraging result was the close agreement between predicted parameters of the system and those determined experimentally.

Further study of the SMSK modem should be done in several areas. For instance, it would be desirable to compare experimental and analytical BER curves. Other types of filters could be studied in order to determine the best possible SMSK filter. Another area of interest would be to determine the effects of hard-limiting on the output waveform which has envelope variation.

REFERENCES

[1] S. Pasupathy, "Minimum Shift Keying: A Spectrally Efficient Modulation," IEEE Communications Magazine, vol. 17, No. 4, July 1979.

[2] F. Amoroso, J.A. Kivett, "Simplified MSK Signaling Technique," IEEE Transactions on Communications, vol. COM-24, No. 4, April 1976.

[3] S.A. Gronemeyer, A.L. McBride, "MSK and Offset QPSK Modulation," IEEE Transactions on Communications, vol. COM-24, No. 8, August 1976.

[4] D.R. Hummels, "On Modeling Digital Communication Systems with Applications to MSK and QPSK," Final Report, KSU Engineering Experiment Station Project 2732, to be published June 1980.

[5] Linear Integrated Circuits, Motorola Data Book, Motorola Inc., vol. 6, Series B, 1976.

[6] Linear Ferrite Materials and Components, Ferroxcube Data Book, Ferroxcube Corp., first edition, Saugerties, N.Y.

[7] Phase-Locked Loop Systems Data Book, Motorola Inc. second edition, August 1973.

AKNOWLEDGEMENTS

THE DESIGN OF A SERIAL MSK MODEM

by

LARRY N. PHILLIPS

B. S., Kansas State University, 1978

_____

A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1980

ABSTRACT

Serial minimum shift keying (SMSK) represents a simple way of generating MSK, and the emphasis of this report was to design, construct, and evaluate a SMSK modem. It was found that the construction of an optimum SMSK system was complicated by the difficulty in synthesizing an ideal SMSK filter. The ideal filter was approximated with a single pole bandpass filter, and this approach represented a form of suboptimum SMSK. Evaluation of the suboptimum modem included observation of the modulator output in the time domain and its power spectrum, and an analytical comparison between the bit error rate performance between ideal and suboptimum SMSK.