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/THE MC68701 BASED SPECTRUM ANALYZER/

by

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CHAPTER I

INTRODUCTION

A time varying signal can be characterized by its frequency spectrum. By knowing the frequency composition of a signal, important operations like sampling can be performed on the signal without loss of information. Also differences in the frequency composition of signals and noise, can be exploited and used as indications for control purposes.

In Fourier analysis, an amplitude-time waveform is transformed into a frequency spectrum, which is the amplitude of each frequency plotted against frequency. The amplitude spectrum of a waveform is plotted as the amplitude density (in volts per hertz) versus frequency (in hertz). In some cases the power density is plotted against frequency. Such a plot is called a power density spectrum or simply a power spectrum.

This report, describes a spectrum analyzer which is relatively simple in operation, and inexpensive in construction, and uses the MC 68701 microcomputer. A block diagram of the system is shown in Fig. 1. Descriptions of the major sections of the Spectrum Analyzer and various hardware designs used are also given.

The key component in this system is the MC68701 microcomputer, which generates the various frequencies of interest, and the control signals. The MC68701 also acts as an interface between the input section and the North Star computer. This interface provides a conversion of ASCII coded serial data (from the NorthStar) to binary coded parallel data required for the

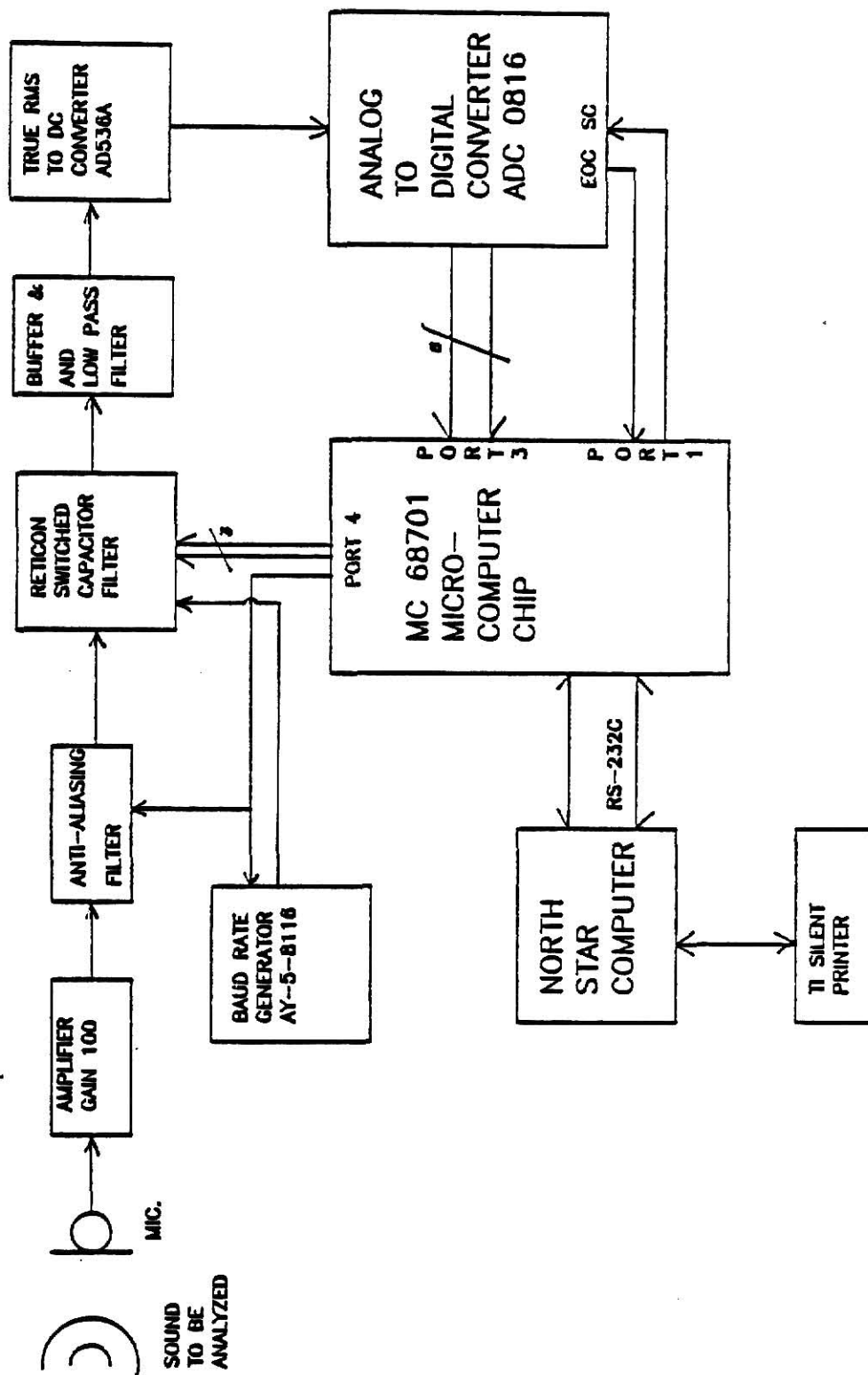


Fig. 1.0 Block diagram of the MC 68701 based Spectrum Analyzer

generation of frequencies. It also receives the binary data from the A/D converter and converts it to ASCII coded serial data (for the North Star). In addition, it also performs logic level translation from RS232C (at the North Star end) to TTL logic (at the interface end). The MC68701 is discussed in detail in chapter III. The analog input section, where the signals are received and modified, is discussed in chapter II. A brief description of the software is also discussed in chapter III. A discussion of results obtained is given in chapter IV. A listing of the software and the program in BASIC for the North Star computer is included in Appendix I.

One of the main advantages of this system is the elimination of tiresome calculations required to obtain the spectrum of noise signals. Such a system will play an important role in the analysis of noise signals. A simple operating procedure is outlined in the chapterVI for the convenience of the user.

CHAPTER II

INPUT ANALOG SECTION

The input analog section essentially consists of the following :

- A. Microphone
- B. Input Amplifier
- C. Anti-Aliasing Filter
- D. Switched Capacitor Filter - The Reticon
- E. Buffer Amplifier
- F. True RMS to DC converter - AD536A
- G. A/D converter - ADC0816
- H. Baud Rate Generator - AY-5-8116
- I. RS-232C standard serial interface

The following sections discuss in detail each of the above.

A. The Microphone

There are several types of microphones commercially available which use a diaphragm arrangement to convert the air pressure oscillations into mechanical motion. This diaphragm is coupled to a condenser, which generates an electrical charge when stressed by the motion of the diaphragm. The microphone used in this present application has good sensitivity and a frequency response of 15 KHz. In addition it offers simplicity and durability.

The microphone is an "omnidirectional" device in that it is sensitive to signals coming at it from virtually any direction. Even so, some care must be exercised when positioning the

microphone in order to obtain reliable data. Also, the positions selected for noise measurement often depend on the purpose of measurement. For example in measuring the noise emitted by a motor, it should be placed as near as possible to the noise source, without actually making contact with any of the moving parts. This way, important information is not lost. To avoid interference it is good to have effective filtering between the microphone and the rest of the analog section. This is achieved by a capacitor and resistor network. The microphone connections are shown in Fig. 2.1.

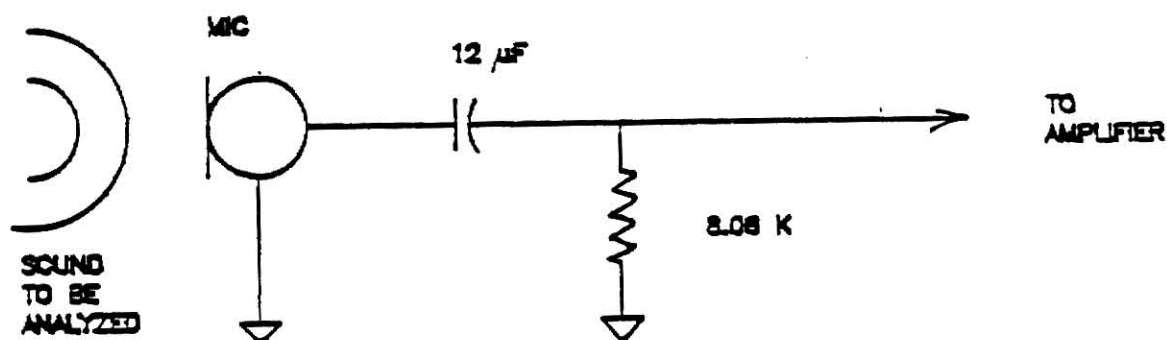


Fig. 2.1 Microphone Connections

B. The Input Amplifier

This amplifier is required at the input so that the signals can be raised to a level where they can be easily analysed. A block diagram of the amplifier is shown in Fig. 2.2. The amplifier is configured as a non-inverting amplifier with an overall gain of approximately 100. An amplifier with such a high gain is required because the noise signals being measured have amplitudes usually in the millivolt range. Also it is required to raise the level of the signal so that it would prove suitable for conversion by the analog to digital converter.

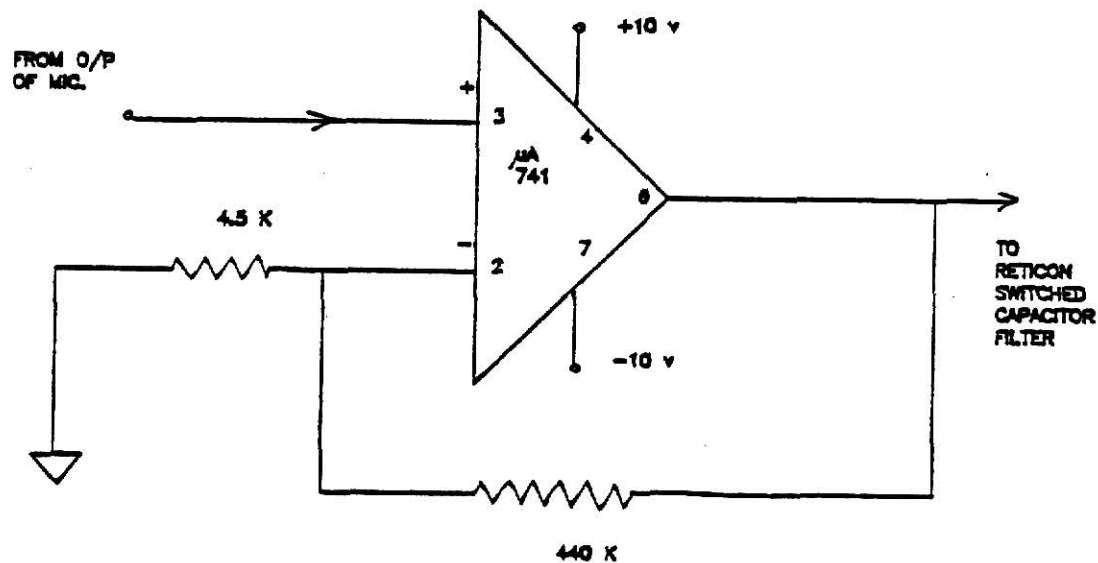


Fig. 2.2 Input amplifier with a gain of 100

C. Anti-Aliasing Filter

At the output of the input a low pass filter is included to avoid aliasing. This low pass filter is actually a filter having two cut-off frequencies. One filter configuration has a cut-off frequency of approximately 5 KHz. When the switch across the resistor is closed, another resistor comes in parallel with the already existing resistor to give a filter cut-off frequency of 15.5 KHz. Care should be taken to see that the 'on' resistance of the switch is taken into account when calculating the cut-off frequency. The switch is controlled by the MSB of port 4 of the MC68701 microprocessor. Two such filters have been provided to accommodate signals having frequencies greater than 5

KHz.

When $R=4\text{ K}$, $C=0.008\text{ mfd}$

$$\begin{aligned} F_c &= 1/2 \times 3.14 \times R \times C \\ &= 1/2 \times 3.14 \times 4 \times 10^3 \times 0.008 \times 10^{-6} \\ &= 4.973\text{ KHz} \end{aligned}$$

When the switch is "ON":

$$\begin{aligned} R_{on} \text{ of switch is } 80\text{ ohm. Then } R_{eff} &= 1.88 \times 4 \times 10^6 / 5.88 \times 10^3 \\ &= 1.2789\text{ K} \end{aligned}$$

$$\begin{aligned} F_c &= 1/2 \times 3.14 \times R_{eff} \times C \\ &= 1/2 \times 3.14 \times 1.2789 \times 0.008 \times 10^{-3} \\ &= 15.5\text{ KHz} \end{aligned}$$

The filter connections are shown in Fig. 2.3.

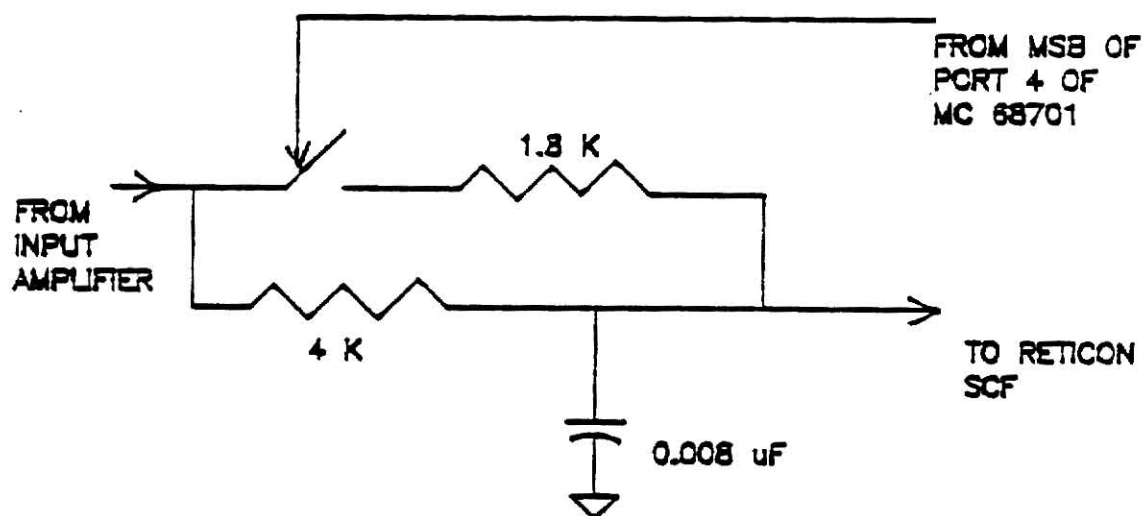


Fig. 2.3 Connections for the Anti-Aliasing filter

D. Switched Capacitor Filter (SCF) - The Reticon

The connections for the SCF is shown in Fig. 2.4.

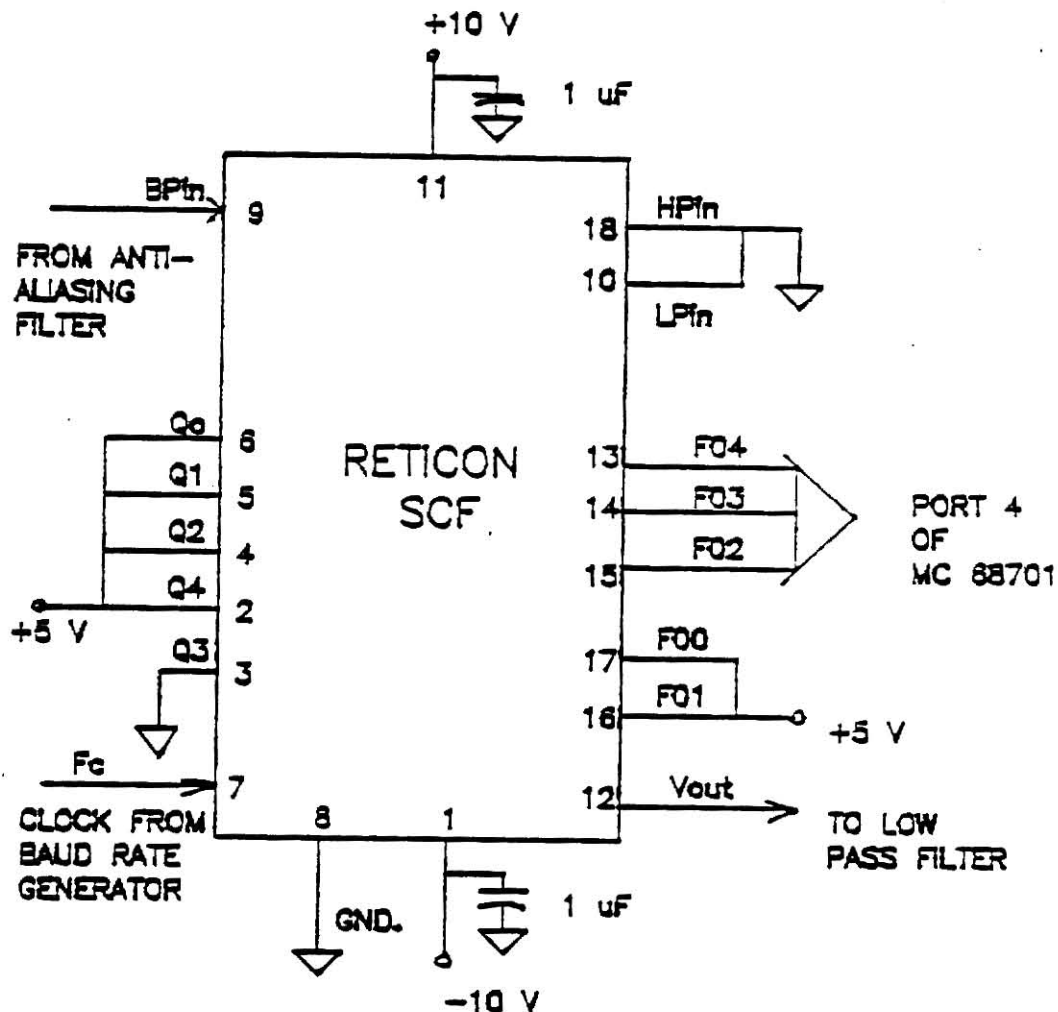


Fig. 2.4 Connections for the Reticon SCF

Switched capacitor filters are similar to standard active filters with switched capacitor resistors in place of the normal non-tunable resistors. The stability and the clock tunability of the SCF eliminates alignment problems. SCF's can be tuned by varying the master clock and have excellent stability. The greatest advantage of this SCF is the ability to integrate several filters of various types onto a single chip, thus realizing a savings in the PC board testing and inventory.

The SCF is used to sweep through the spectrum of interest. The Reticon is a double-poly, NMOS, switched-capacitor, active filter. It can be used to perform as a low pass, high pass, band

pass, all pass or a notch filter. It can also be configured to perform as a sine wave oscillator with no external components except an external clock. The filter responses are determined by ten pins which may be digitally controlled or hardwired.

The Q and center frequency response of the filter are controlled by ten digital inputs. Five of the pins can be used to vary the clock frequency to center frequency ratio over two octaves and the other five pins are used to vary the value of Q , which ranges from 0.57 to 150.

For the present application, the SCF is hardwired for a Q value of 40.0. A high value of Q is chosen so that it would improve the frequency selectivity of the circuit. It may be recalled that the quality factor Q of a circuit is defined as the ratio of resonant frequency to bandwidth. Out of the five pins provided to vary the ratio of F_c/F_o , the pins F_{o1} and F_{o0} are tied high. The other three pins F_{o2} , F_{o3} , F_{o4} are connected to the three LSB's of port 4 of the MC 68701. The baud rate generator which provides the clock for the Reticon is configured so as to generate two frequencies both above 60 KHz. It must be recalled that the microphone used at the input has a cut-off frequency of 15 KHz. Also the anti-aliasing filter used has a maximum cut-off frequency of 15.5 KHz. This means the sampling frequency has to be greater than 30 KHz to avoid aliasing. But, according to the data sheets of the Reticon, it is stated that the master clock has to be greater than twice the clock frequency to avoid aliasing. Hence the baud rate generator is configured to

generate only the frequencies 77504 Hz and 307185 Hz, which are both over 60 KHz. With the SCF being configured as above, the frequency of the input signal ranges from 425.7 Hz to 6143.7 Hz. This is easily determined by using the relation $\text{Ratio} = F_c/F_o$. The amplitude of the the input signal at each of the sixteen frquencies is measured.

The BPin pin of the SCF is used to feed the incoming input signal. The LPin and HPin pins are grounded. The output from the SCF is then fed to a low pass filter which has a cut-off frequency of 20 KHz. The design of this low pass filter is as follows -

$$R = 1000 \text{ ohms, } F = 20 \text{ KHz, } C = ?$$

$$F = 1 / 2\pi \cdot R \cdot C$$

$$20000 = 1 / 2\pi \cdot 10^3 \cdot C$$

$$C = 0.008 \text{ nfd.}$$

A low pass filter is included at the output of the SCF to cut out the clock noise introduced by the baud rate generator. The signal is then passed on to the buffer amplifier stage.

E. Buffer Amplifier

This buffer amplifier is essentially an unity gain voltage follower having a non-inverting configuration. This amplifier has an overall gain of one. The main reason for including a buffer at this stage is to decrease the input loading effect and to provide effective impedance matching. A voltage follower has a high input impedance. Hence, it draws negligible current from a signal source. Also, it provides impedance matching and acts as a "buffer" between two blocks. The signals at the output of this

amplifier follow the input and are not altered. The signals are then passed on to the RMS to DC converter. The circuit diagram for the buffer amplifier is shown in Fig. 2.5.

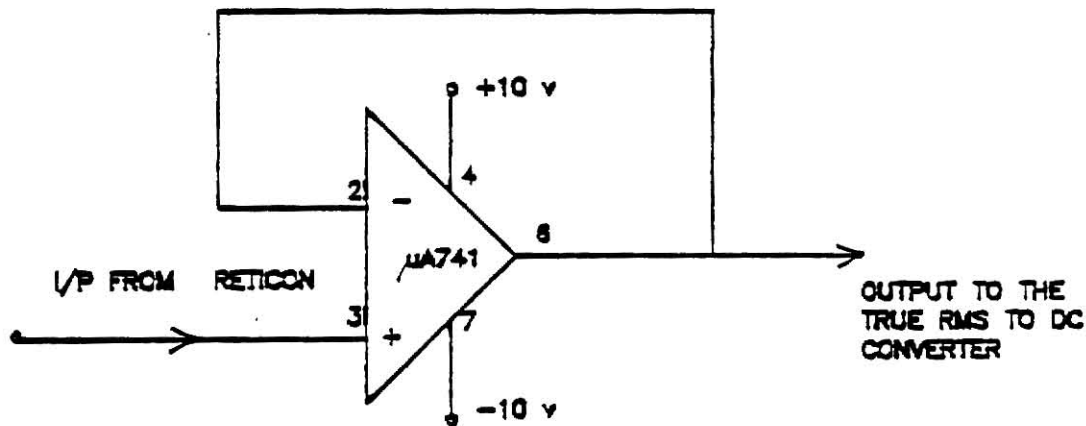


Fig. 2.5 Connections for the Buffer amplifier

F. True RMS to DC converter - AD 536A

The RMS to DC converter computes the true RMS value of any complex input signal containing AC and DC components. The connection diagram for the AD 536A is shown in Fig. 2.6.

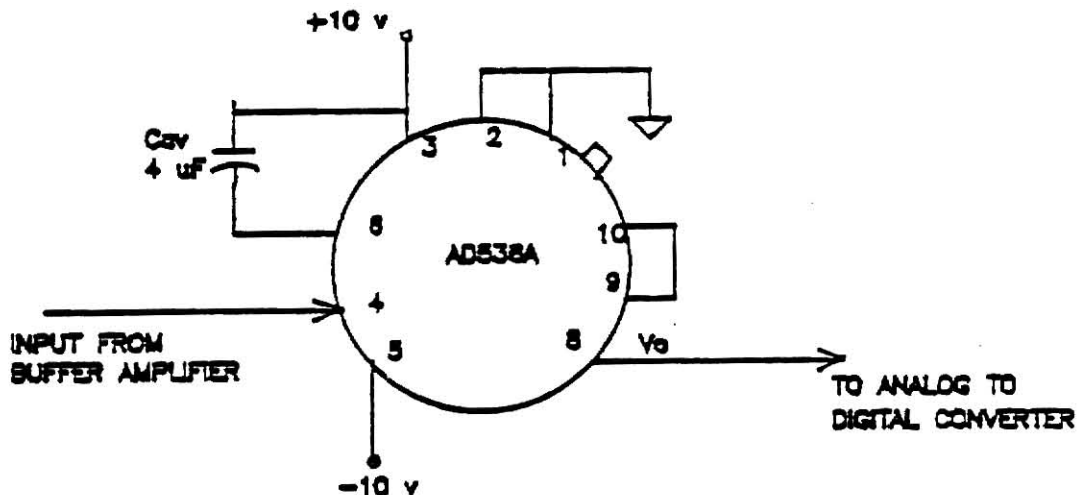


Fig. 2.6 Connections for the true RMS to DC converter

The actual computation performed by this device follows the

equation

$$V_{rms} = \text{Avg.}(V_{in}^2 / V_{rms})$$

This true RMS to DC converter is subdivided into four major sections : absolute value circuit which is an active rectifier, squarer/ divider, current mirror and a buffer amplifier. As shown in the connection diagram the device needs an external capacitor to set the averaging time constant. The AD 536A will compute the RMS value of both AC and DC signals. If the input is a slowly-varying DC, the output of the device will track the input exactly. At higher frequencies, the average output of the device approaches the RMS value of the input signal.

In this present application, the AD 536A is operated with a supply voltage of +10 volts. The input and output signal ranges are a function of the supply voltage. The advantage of this device is that it has a buffer amplifier at the output. A RMS to DC converter is necessary to convert the incoming signal to a RMS value which would be a suitable input to the A/D converter.

G. A/D Converter - ADC 0816

The A/D converter used is the AD 0816. It is a 8 bit converter with a 16-channel multiplexer. The A/D converter uses successive approximation as the conversion technique. The 16-channel multiplexer can directly access any one of the 16 single ended analog signals and provides the logic for additional channel expansion. This A/D offers high speed, high accuracy, minimal temperature dependence, excellent long term accuracy, repeatability and consumes minimal power. There is also another input

available called the comparator input, which is a direct input to the A/D. For the present application, as there is only one input, this input is made use of. The A/D has a conversion time of 100 microsecs. and a total unadjusted error of $\pm 1/2$ LSB. The connection diagram is shown in Fig. 2.7.

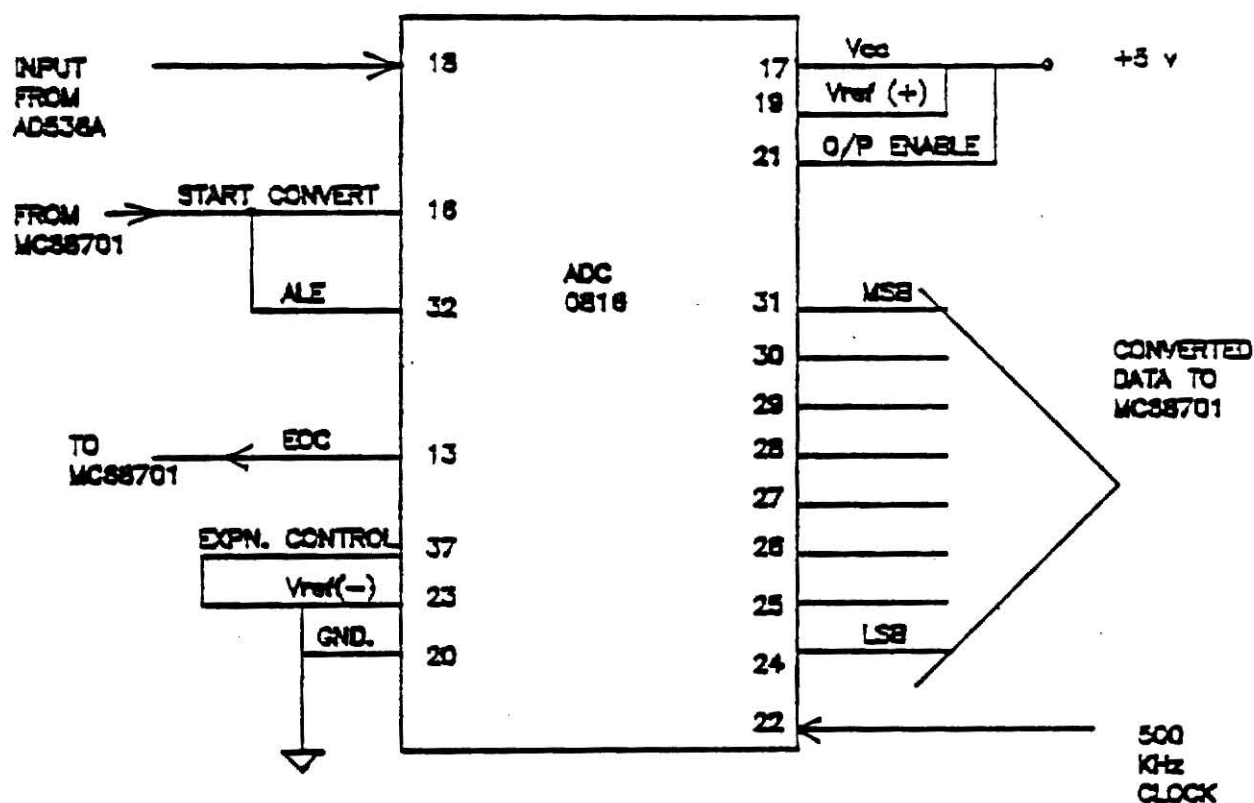


Fig. 2.7 Connections for the ADC 0816

The A/D is under direct control of software. The start convert signal is supplied by software. As it can be observed from the timing diagram of the A/D (Appendix II), the end of conversion (EOC) signal goes low after the start convert signal is supplied. It remains low until the conversion is complete, after which it becomes high, indicating that the conversion is complete. This low-to-high transition of the EOC is sensed again

by software.

The output enable pin of the A/D is tied to +5 volts. When tied permanently high, the output is always enabled. Care should be taken to see that the A/D is read for data only after conversion is complete. The address latch enable (ALE) is tied to start convert pin of the A/D, as it has a similar waveform to the start convert signal only a slightly delayed version. The expansion control pin of the A/D is tied to ground so as to disable the 4 bit address. The 4 bit address is disabled as none of the inputs are being made use of. Vref(-) is tied to ground and Vref(+) is tied to +5 volts.

A 500 KHz square waveform acts as the clock of the A/D. The clock circuit is shown in Fig. 2.8.

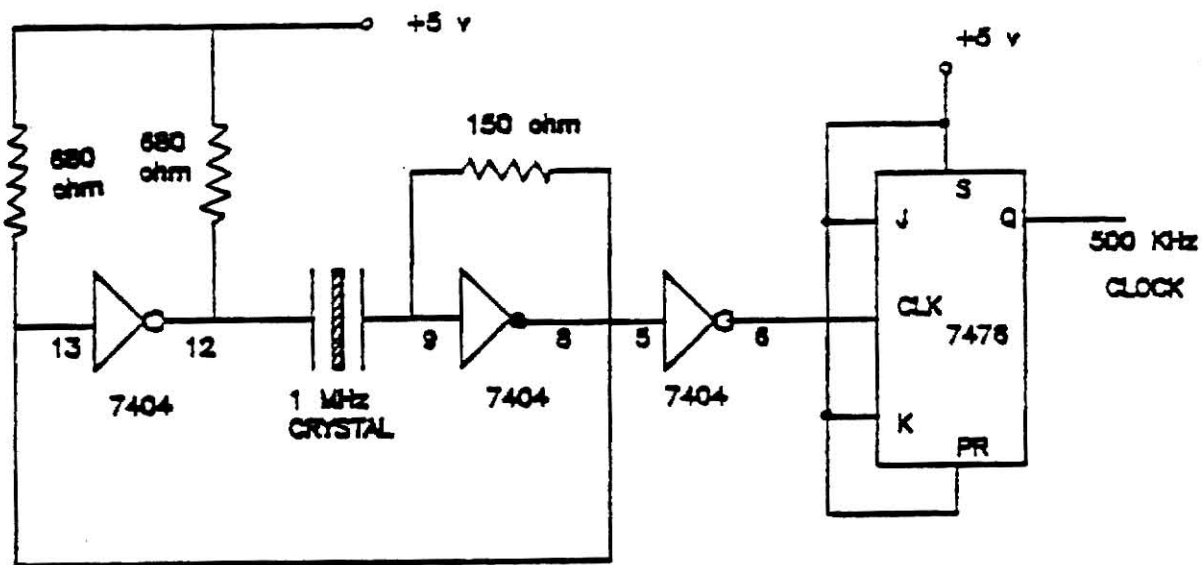


Fig. 2.8 Circuit to obtain 500 KHz clock for the ADC 0816

The crystal used is a 1 MHz crystal and then it is passed through a simple divide by two circuit to obtain the required 500 KHz.

H. Baud Rate Generator - AY-5-8116

The connections for the baud rate generator is shown in Fig. 2.9. The AY-5-8116 is used to generate the clock frequencies for the Reticon Switched capacitor Filter. The frequency generated depends on the word pattern fed to the four inputs Ra, Rb, Rc and Rd of the baud rate generator. An external 4.91520 crystal is connected to the two XTAL pins.

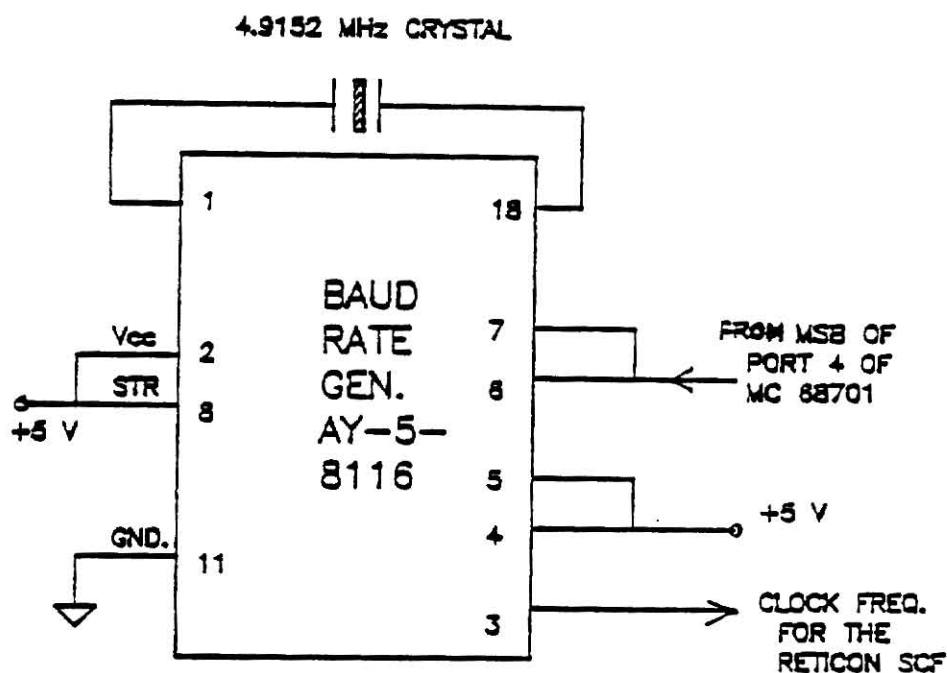


Fig. 2.9 Connections for the Baud rate generator

The AY-5-8116 has dual selectable 16 clock outputs. The range of frequencies extend from 800 Hz to 307.200 KHz. The AY-5-8116 has dividers at the output of the oscillator to generate the different frequencies.

The word pattern to generate the various frequencies is supplied at the computer end by the user. For the present application the baud rate generator is used to generate only two

clock frequencies, both of which have to be above 60 KHz to avoid aliasing. It can be observed from the data data sheet for the AY-5-8116 that the word pattern to generate the frequencies 77504 and 307185 differ by two bits. The two bits which are common for both frequencies are tied high. The other two are bits are shorted and connected to the MSB of port 4 of the MC68701 microprocessor. When the MSB is high the frequency 307185 is generated and when the MSB is low the frequency 77504 is generated. These act as the clock frequency to the Reticon switched-capacitor filter.

I. RS-232C Serial Interface

The signals going in and coming out of the processor are not adequate to communicate with a peripheral controlled by the processor. Thus, the signals are seldom sent directly to the interface. The terminals transfers characters of data in the ASCII form. Special hardware is used to form a standardized communication bus to which memory and peripherals are interfaced. A widely used standard wherein the terminals used serial communication is the Electronic Industry Associates (EIA) specification RS-232C standard.

All RS-232C signals must be within the limits shown below-

1. +3 volts to +15 volts for a zero.
2. -3 volts to -15 volts for a one.

Thus level translators are required between the TTL levels and the MODEMS. The level translators require additional power supplies (+12 volts and -12 volts) to generate the required signal voltages. The two translators used are :

1. MC1488 : Quad TTL to RS-232C. This is for data going to the
MODEM.
2. MC1489 : Quad RS-232C to TTL. This is for the data coming
from the MODEM to the device.

In all, the RS-232C interface consists of 25 data lines. Quite a few of these are undefined. In most computer terminals only 3 to 5 data lines are required for operation.

CHAPTER III

THE MC68701 MICROCOMPUTER

A. HARDWARE DESCRIPTION

The MC68701 is a single chip microcomputer that is compatible with the M6800 family parts. The onboard chip resources of the MC68701 microcomputer include:

1. 128 bytes of internal RAM.
2. 2-K bytes of EPROM.
3. Serial Communications Interface (SCI)- analogous to the Asynchronous Communications Interface Adapter (ACIA).
4. Parallel I/O ports- that could be used as Peripheral Interface Adapter (PIA).
5. Programmable Timer.

The internal RAM is located at hexadecimal addresses 0080 through 00FF and the internal EPROM resides at F800 through FFFF. The memory locations 0000 through 001F are reserved for the internal registers. The microcomputer (MCU) has an access to a 64-K byte address space.

A few hardware features of the MCU are:

1. 8-bit word size.
2. 16-bit address field.
3. An internal oscillator with a divide by four circuit.
4. M6800 bus compatible.

The instruction set for the MC68701 is similar to that of the M6800 except for a few added instructions. Accumulators A and B can be concatenated to form accumulator D, which is 16-bit wide.

The MC68701 has 29 parallel I/O lines shared by four ports 1, 2, 3 and 4. A simple block diagram of the MCU with it's ports is shown in Fig. 3.1.

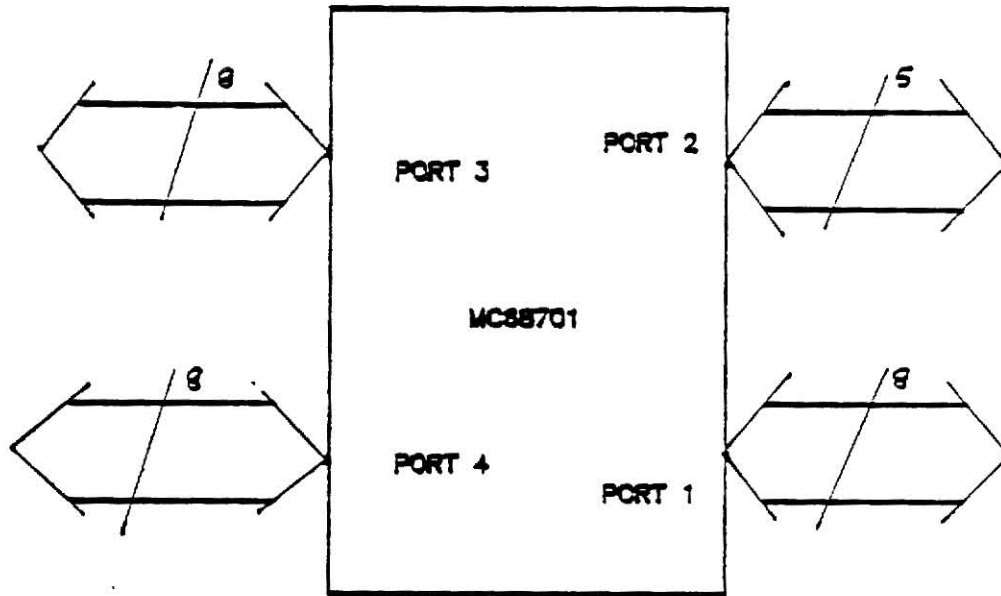


Fig. 3.1 Ports of the MC 68701

An I/O device is interfaced to the microprocessor through an I/O port. Transfer of data and direction of data flow can be accomplished by suitably programming these ports.

Ports 1 and 4 have 8 I/O lines each. Port 3 besides having 8 I/O lines, has two control pins SC1 and SC2. The operation of these pins depend upon the mode of operation of the MC68701.

These ports can be programmed by the user's program. Each port is provided with a data register and a data direction register. The ports act as inputs or outputs depending upon the configuration of the bits in the data direction register. A one in the data direction register indicates that it is an output bit and a zero indicates that it is an input bit.

Port 2 is a 5-bit port unlike the other ports which are 8-

bit. This port is used as an interface for the SCI and the timer. The three least significant bits of the data register of port 2 provide the operating mode for the MC68701. Port 3 in addition to the data register and the data direction register has a control and status register to configure the control lines SC1 and SC2. Depending upon the mode of operation, port 3 can be used either as a bidirectional data bus or a multiplexed address/data bus.

B. MODES OF OPERATION OF THE MC68701

The MC68701 can function in eight modes- Mode 0 through Mode 7. Mode 0 is a reserved mode exclusively for programming the onboard EPROM. The modes are selected by connecting the switches to pins 8,9 and 10 of the MCU as shown in Fig. 3.2 . Upon RESET, the levels on the pins P20, P21 and P22 are latched into PC0, PC1 and PC2 bits of the data register of port 2. The processor then recognizes that it has to operate in the required mode.

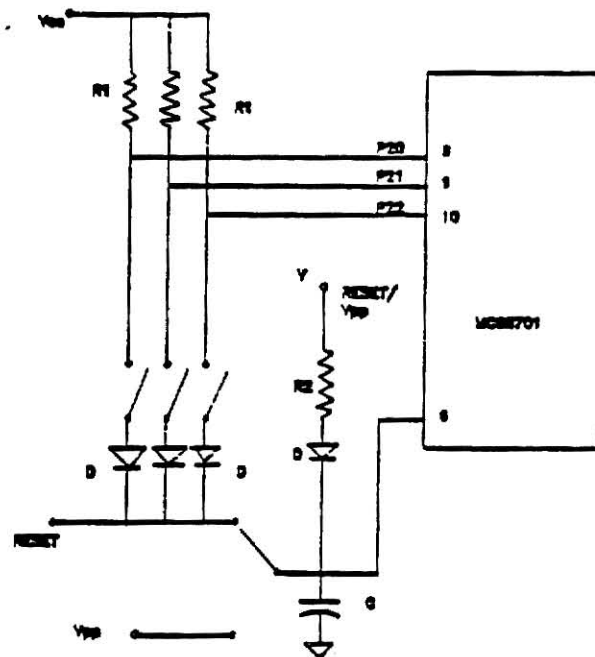


Fig. 3.2 Reset and Mode configuration

The eight operating modes of the MC68701 can be broadly classified under three major modes as:

1. Single chip Mode (Modes 4, 7).
2. Expanded Non-Multiplexed Mode (Mode 5).
3. Expanded Multiplexed Mode (Mode 1, 2, 3, 6).

Each of the above operating modes has an unique memory map, illustrating the allocation of the 64-K byte memory space. Invariably for all the modes, the first 32 locations in memory are reserved for the internal registers. In modes 2, 3 and 4 the internal EPROM is not included in the memory map. Depending upon the user's application, RAM's or ROM's could be fitted into the external memory space in any mode. A decode logic circuit distinguishes the internal memory from the external memory.

In some modes the internal EPROM addresses FFF0 through FFFF are not usable as this area is assigned for the external interrupt vectors. Upon RESET, the processor fetches the RESET vector from an external RAM or ROM where the interrupt vectors reside.

For the present application, the operational mode selected is the Single Chip Mode (Mode 7). Ports 3 and 4 are used for the data transfer between the MCU and the input analog section. In mode 7, ports 3 and 4 being parallel I/O ports, can be used for the above purpose. In this mode of operation there is no need for an external address bus as external memories are not required. Also, the onboard EPROM is included in the memory map.

C. QUAD BUS TRANSCEIVER

The quad three state transceiver is used for the purpose of

data transfer between the MC68701 and the input section. A simple block diagram of a quad three state bus transceiver, the MC8T26A is shown in Fig. 3.3.

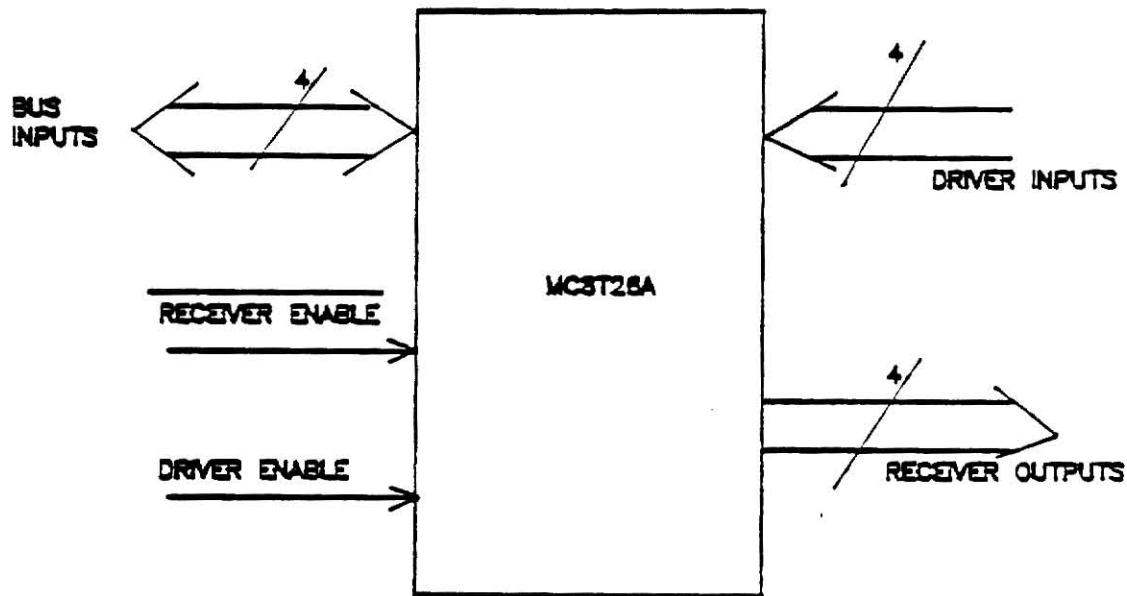


Fig. 3.3 Block diagram of the Tri-state Transceiver

It consists of 4 bus inputs, 4 receiver outputs, 4 driver inputs and 2 control lines (Receiver Enable Input and Driver Enable Input). A low signal on the Receiver Enable Input enables the receiver outputs and a high signal on the Driver Enable Input enables the driver inputs.

A bank of two quad bus transceivers is connected between the processor and the A/D converter in the analog input section. The I/O lines of Port 3 form the bus inputs to the tristate buffers. Another quad bus receiver is connected between the processor and the switched-capacitor filter. The MSB of Port 4 is connected via this quad bus receiver to two of the inputs of the

baud rate generator, to generate the different clock frequencies for the switched capacitor filter. The Receiver Enable Inputs and the Driver Enable Inputs are shorted together.

The software determines if the control pin is to be high or low. When there is a high signal on the Driver Enable Input the data at the output of the A/D converter is sent to the processor.

D. CONFIGURATION OF PORT 1

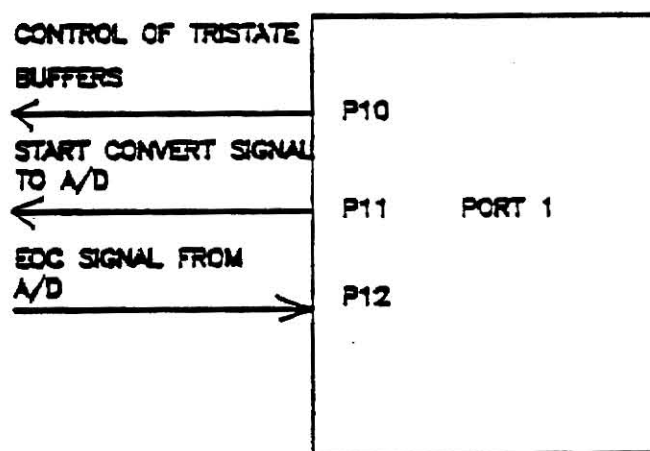


Fig. 3.4 Configuration of Port 1

Port 1 is configured as shown in Fig. 3.4. Bit 0 is connected to the control of the tristate buffers. Bit 1 is connected to the start convert pin of the A/D converter through a buffer stage. Bit 2 is connected to the end of conversion (EOC) pin of the A/D converter.

E. DESCRIPTION OF THE HARDWARE OPERATION

The schematic diagram of the MC68701 based Spectrum Analyzer is shown in Fig. 3.5. The resistor-diode circuit connected to pins 8, 9 and 10 of the processor is for selecting the required mode of operation. In this application the switches S1,

S2 and S3 are open so that the processor operates in Mode 7. A crystal of 3.958 MHz is connected to pins 3 and 4 of the processor. This frequency is chosen so that upon proper configuration of the bits in the Rate and Mode Control Register, standard baud rates are available. Pins 4 and 5 (being Non-Maskable Interrupt and Interrupt Request) are tied high to disable the interrupts.

Pins 11 and 12 of the processor are connected to the level translators, MCl488 and MCl489 allowing for the Serial Communications Interface (SCI) to accept the serial data characters from the terminal or to transmit the bits serially to an asynchronous serial data device. The SCI has two control registers : Rate and Mode Control Register (RMCR) and Transmit/Receive Control and Status Register (TRCSR). The SCI is initialised by initialising these two registers. The least two bits in the RMCR provide the standard baud rates of 300, 1200, 9600 and 76,800. Depending upon the requirement, the bit configuration is done in the software.

Ports 3 and 4 are configured either as input ports or output ports depending on the data transfer between the processor and the A/D converter or the baud rate generator. One of the I/O lines of port 1 is used to indicate to the processor the direction of data flow. If the bit is low, the data flow is from the processor to the baud rate generator and the SCF. If the bit is high the data flow is from the A/D converter to the processor. The software determines if this bit is to high or low. This bit of port 1 is connected to the control line (ie., the Receiver Enable Input or the Driver Enable Input shorted) of the the quad

bus transceivers.

The two main functions of the interface are:

1. To provide the required word pattern to the baud rate generator and the SCF.
2. To read the data from the A/D converter.

The steps involved in providing a word pattern to the baud rate generator are :

1. The SCI accepts the ASCII characters from the terminal via the RS-232C level translators.
2. The software makes the ASCII to BCD to binary conversion.
3. Port 4 is configured as an output port.

The steps involved in reading data from the output of the A/D converter are:

1. Port 3 is configured as an input port.
2. Bit 0 of port 1 is made high. (This drives the Driver Enable Input of the transceiver high, thus enabling the processor to read the data from the output of the A/D converter.)
3. The software makes the binary to BCD to ASCII conversion.
4. The SCI sends the bits serially to the computer.

F. SOFTWARE DESCRIPTION

The software controls the direction of the data transfer and is also responsible for the ASCII to BCD to binary conversion and vice-versa. If the interface receives an "&", the data transfer is from the computer to the baud rate generator, to generate the various clock frequencies. If it receives a "?", the data transfer is from the output of the A/D converter to the computer.

To begin with, all the data registers, data direction registers, control registers and stack pointer are initialized.

The following steps are involved if an "&" is recognized :

1. Port 1 (excepting bit 2) is configured as an output port.
Bit 2 is configured as an input.
2. Port 4 is configured as an output port.
3. ASCII to BCD to binary conversion is performed.
4. The binary data is stored in the four most significant bits of port 4.
5. A software delay is created so that the data on the interface lines becomes stabilised.
6. Bit 1 of port 1 is made high and then low, thus initiating the conversion for the A/D .
7. A software loop is set up to see if the end of conversion pin becomes high, indicating that the conversion is complete. This pin is connected to bit 2 of port 1, which is an input. When conversion is complete, data is available at the output lines of the A/D converter.

The following steps are involved if a "?" is recognized:

1. Port 1 (excepting bit 2) is configured as an input port. Bit 2 is configured as an input.
2. Port 3 is configured as an input port.
3. A high signal is sent to the control of the tristate buffers, enabling the driver inputs of the transceivers.
4. Binary to BCD to ASCII conversion is performed.
5. The ASCII data is sent serially to the computer.

G. ONBOARD EPROM OF THE MC68701

One of the excellent features of the MC68701 microcomputer is its ability to program itself. The processor has an onboard 2-K byte Erasable Programmable Read Only Memory (EPROM). Mode 0 is exclusively used to program the onboard EPROM. This mode is an expanded multiplexed mode wherein the MCU has an ability to access a 64-K byte memory space. There is a special circuit available which is used to program the onboard EPROM. First the codes that are to be loaded into the onboard EPROM are entered into a fully erased EPROM called the data EPROM. Then by applying the appropriate voltages to the programming circuit, the codes are downloaded from the data EPROM to the onboard EPROM of the MC68701. Care should be taken to see that the onboard EPROM is fully erased before programming. The programming of the onboard EPROM of the MC68701 was done on the "MC68701 Programmer" available in the Engineering Technology department of Kansas State University.

CHAPTER IV

TESTING, RESULTS AND ANALYSIS

At the terminal end, a program is written in North-Star BASIC to generate the word pattern for the Baud Rate Generator and the switched-capacitor filter and then to accept the converted value from the A/D converter via the MC68701 interface. This value is then used to express the level of the signal in decibels.

There is a total of sixteen frequencies generated, and for each frequency generated the amplitude of the signal at that frequency is obtained and passed on to the computer to be used to calculate the dB level. These values are then used to plot a graph of noise level in dB as a function of frequency. This gives the audio spectrum of the noise source.

Communication between the North-Star computer and the analog input section is established by the "&" command. The "?" command results in the analog section sending the last reading back to the NorthStar, as an ASCII character string. The BASIC program then calculates the db value of the signal at that frequency and prints out the value.

Now, to test the system under discussion, a step by step process has been evolved. Not only was the performance of the system as a whole evaluated, but also the performance of certain important components like the switched-capacitor filter is studied.

Initially, the audio spectrum of the damped noise

existing in the environment where the experiment is carried out is measured. No area is completely noise free and this existing noise contributes to the noise content when the noise from a certain noise source is measured. Knowing this, the actual noise content of the source can be determined by subtracting the background noise from the total noise.

Next, a loudspeaker is used as a sound source. This speaker is fed from a signal generator set at a particular frequency. The noise level is now measured. The actual noise content of this source is determined as explained in the previous paragraph. During this measurement, it is required to see if there exists any distortion or clipping at various sections of the system. This is achieved by observing the waveforms on a scope at various points. This gives an idea about how the system performs during measurements.

Further testing is carried out by injecting a sinusoidal waveform set at a certain frequency straight into the system without feeding it into the speaker. The waveforms at the input and the output of the input amplifier are observed. This provides an insight to the system performance when not measuring noise signals.

To evaluate the performance of the Reticon switched-capacitor filter the following method is adopted. As already stated before in the preceding sections a total of sixteen frequencies is generated by the baud rate generator and the Reticon. Now, each of these sixteen frequencies are generated one at a time and the waveform at the input and output of the Reticon

are observed on the scope. In this way the performance of the Reticon at lower and higher frequencies can be studied.

Finally, the speaker is given an input set at different frequencies and the noise levels are measured. To have a different noise source, the noise levels of a hairdryer are also measured.

To plot the graphs, the "LOGPLOT" routine available in the HP86B computer is used, with a few modifications. This program, written in BASIC, has the capability of plotting the amplitude in decibels as a function of frequency. For convenience the frequency is expressed in logarithmic form, as it is easier to handle. The plot routine is executed and the audio-spectrum of the noise source is obtained. The Y-axis of the plot is seen to be only for a limited range. This is to facilitate better viewing of the signals within a smaller range.

RESULTS AND ANALYSIS

Looking at the plot depicting the noise levels of the speaker output with the input to the speaker being a sinusoid set at 1 KHz, it can be observed that the fundamental occurs close to 1 KHz. The main harmonics seem occur close to 2 KHz and 3 KHz which is as expected. Observing the waveforms at various points of the system during measurement seem to indicate that there seems to be some noise generated which can be attributed to ground loops and inadequate grounding. This can be remedied by having a printed circuit board made for this system. This can eliminate grounding problems to a large extent.

Next, when a sinusoid was injected straight into the system without going through the speaker, it was observed that a fair amount of clipping existed at the output of the input amplifier. This could be because of the offset problems and the high gain of the amplifier. This problem was solved to a great extent by including offset adjustments in the amplifier circuits.

Next, the performance of the Reticon was evaluated as outlined earlier. It was found that the output of the Reticon maintained the basic sinusoid shape during the lower frequencies. But as the frequencies increased and approached 5 KHz the waveforms became distorted and became more triangular in shape. From this it could be concluded that the performance of the Reticon deteriorated and hence became unreliable at frequencies approaching 6 KHz. Figure 4.5 shows how the output of the Reticon changes as the frequency increases.

Next, the noise levels of the output of the speaker with the speaker set at different frequencies is studied. It can be seen that there exists a strong fundamental component with harmonics occurring as expected at multiples of the fundamental frequency. The same trait is observed when studying the plot for the hairdryer. Plots for the different input frequencies are included in this chapter. It can be concluded from the above testing methods and results obtained that the system performs as expected and that distortion occurs at higher frequencies, which can be eliminated by having a printed circuit board made for this system. Also, the performance of the Reticon is fairly reliable at lower frequencies but become distorted at frequencies approach-

hing 6 KHz. Hence the Reticon is recommended for use at lower frequencies and definitely not at frequencies above 6 KHz.

DRAWBACKS AND IMPROVEMENTS

Some of the drawbacks of the system being discussed include, the sensitivity of the baud rate generator, the performance and sensitivity of the microphone being used and the reliability of the components being used in the input analog section.

The AY-5-8116 baud rate generator can only generate sixteen frequencies. Also the frequencies generated are not uniformly spaced. Thus it is very difficult to observe the level of signal at other frequencies than those generated by the baud rate generator. Even the frequencies generated by the baud rate generator are different from those listed in the data sheet of the device. This shows that this device is not very accurate in its performance.

The noise is measured with the aid of a microphone which has to be sensitive to noise and rugged enough to withstand the industrial atmosphere. The microphone used here has a fairly uniform response upto 15 KHz and this could prove sufficient for most applications of measuring audio noise. But in other applications where the spectrum is required for higher frequencies, it is essential to obtain a high performance microphone.

The position of the microphone plays an important role in the recording of the input signal. The microphone, being omnidirectional in nature is susceptible to noise coming at it in

all directions. To make sure that only the valid signal is being recorded the microphone is placed near the noise source. This could help, but it is totally impossible to prevent other signals from being included along with the valid signal. Another reason for placing the microphone as near the noise source as possible is to see that the intensity of the noise level is not reduced with distance.

Another major drawback could be the reliability of the components used in the input analog section. The overall performance of this system could be improved considerably by using precision components. For example the input amplifier can be made a precision amplifier with very little offset and very high input impedance. The resistors and capacitors used can be made precision resistors and teflon capacitors.

The main advantage of the system lies in the simplicity of operation. It does not require expertise or a great deal of know-how to operate this system and can be easily accomplished by a layman.

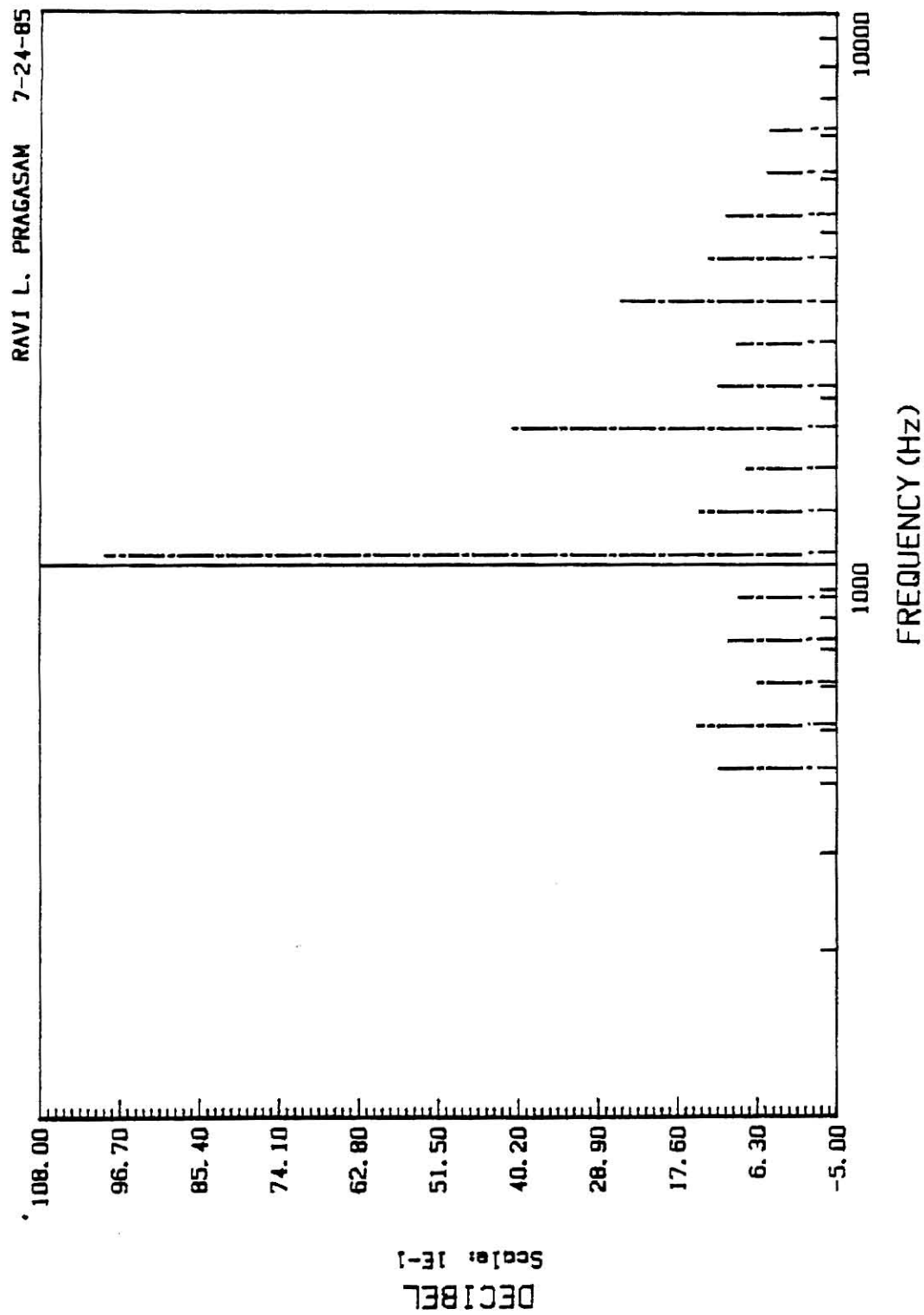


Fig. 4.1 AUDIO SPECTRUM ANALYZER OUTPUT (SPEAKER AT 1 KHz)

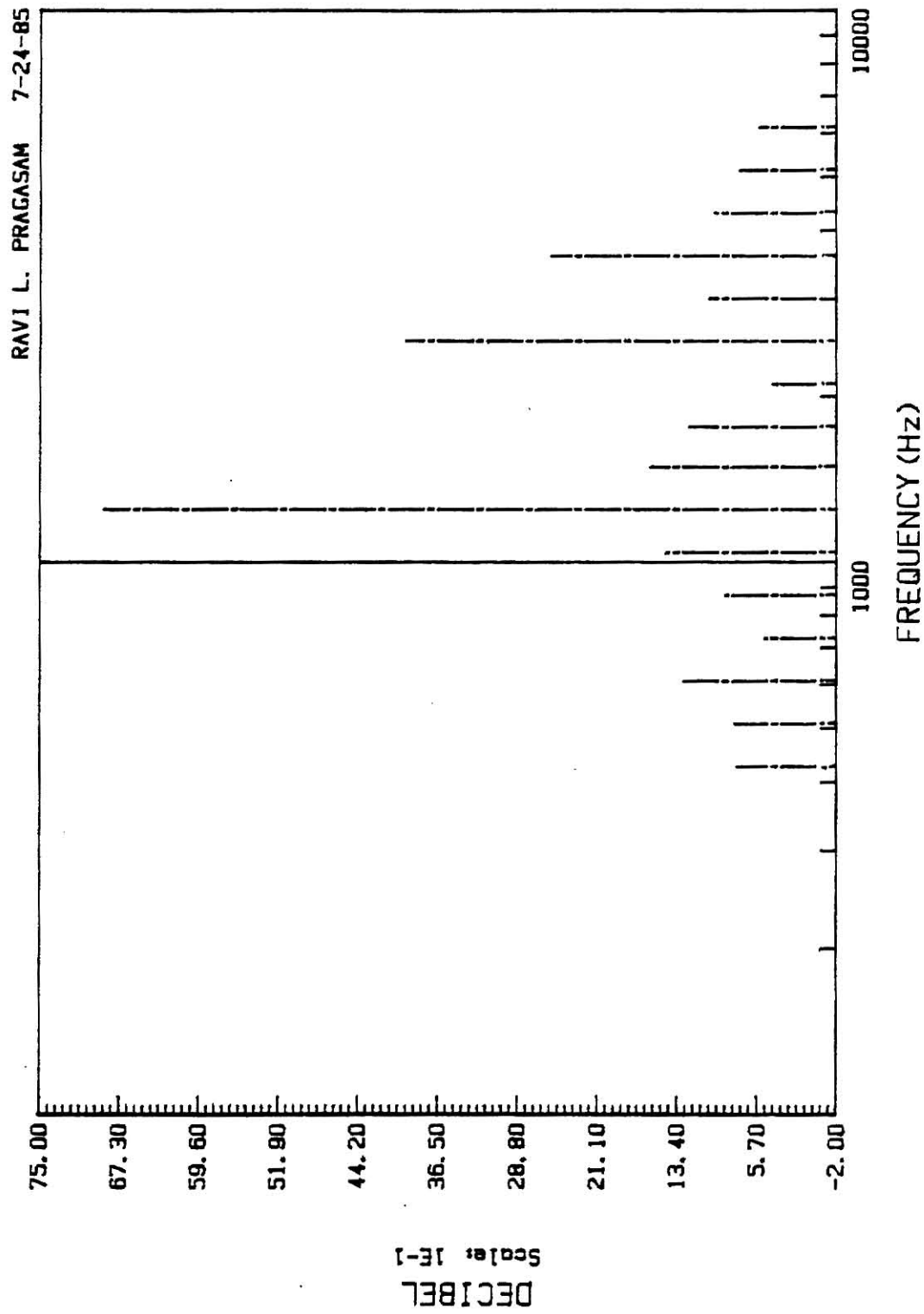


Fig. 4.2 AUDIO SPECTRUM ANALYZER OUTPUT (SPEAKER AT 1.2KHz)

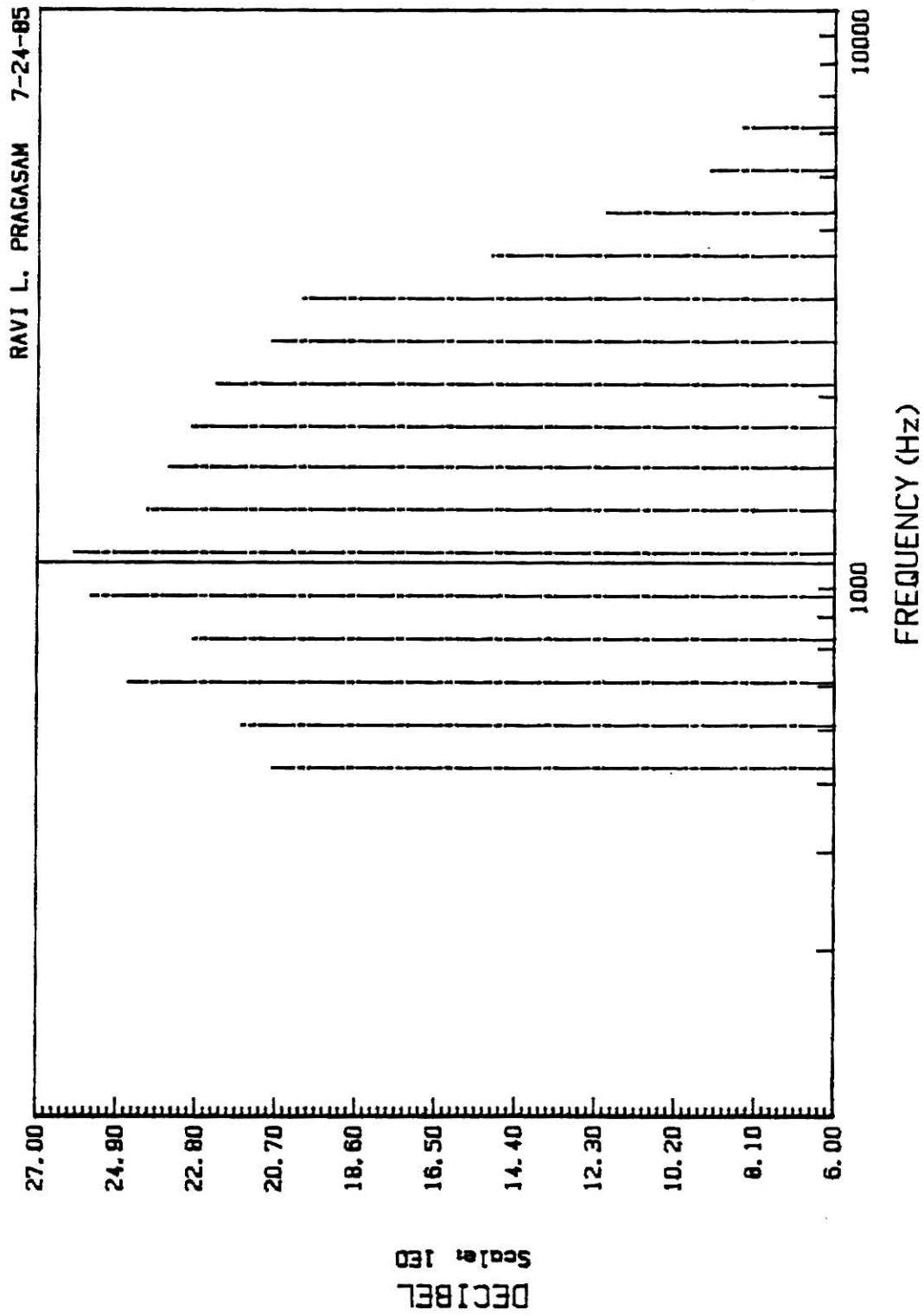


Fig. 4.3 AUDIO SPECTRUM ANALYZER OUTPUT (BACKGROUND NOISE)

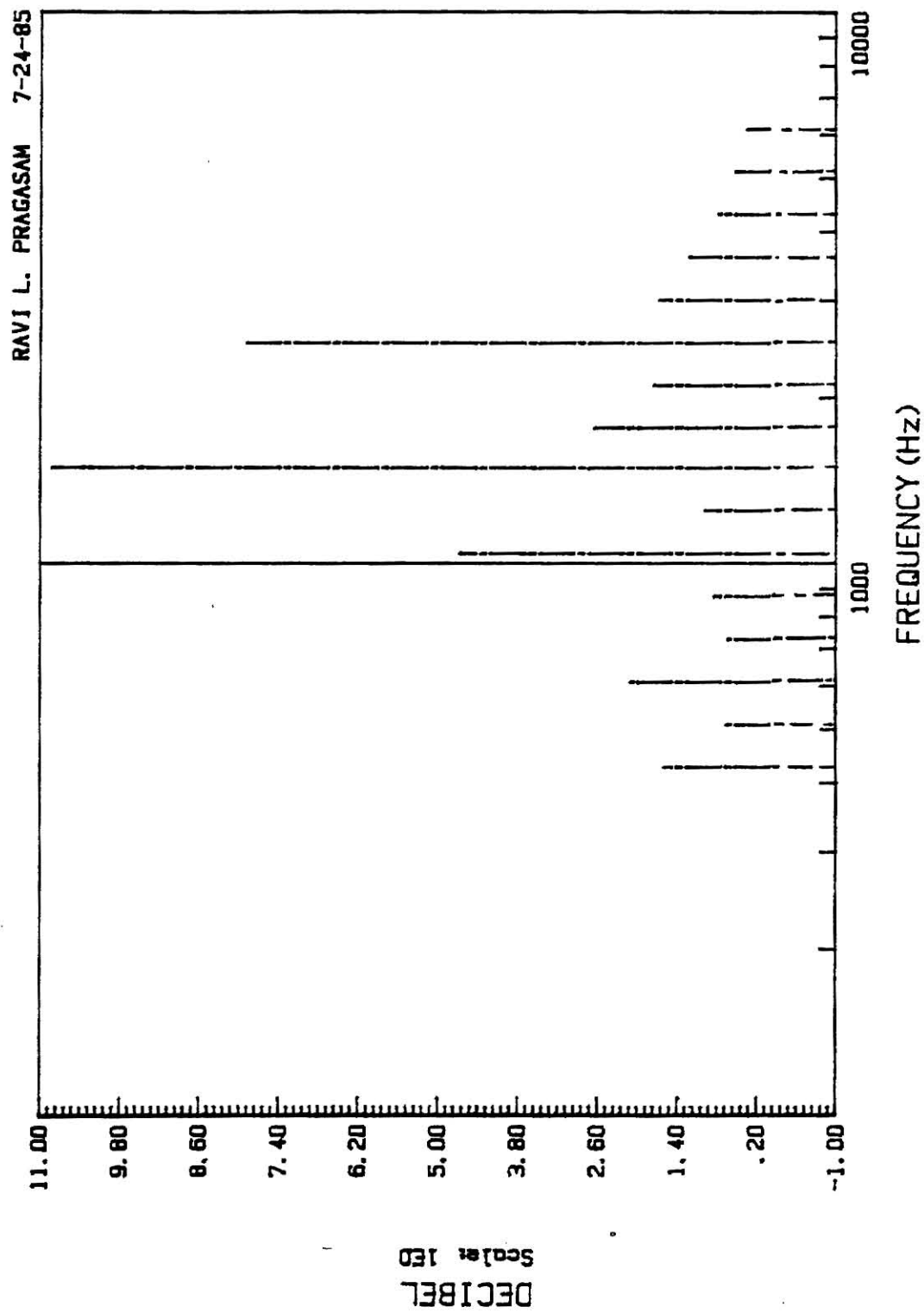


Fig. 4.4 AUDIO SPECTRUM ANALYZER OUTPUT (HAIRDRYER)

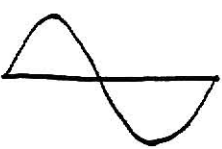
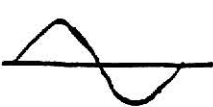
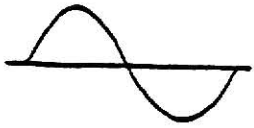














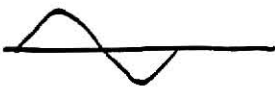

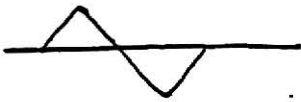
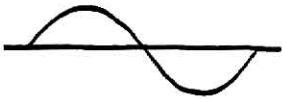
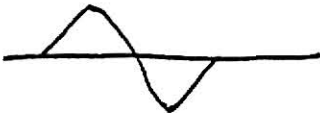

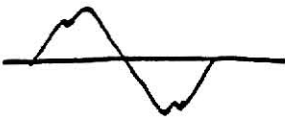



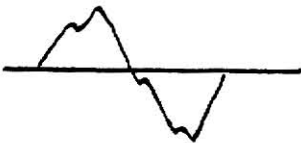

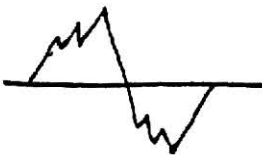


FREQ. IN Hz.	INPUT OF RETICON	OUTPUT OF RETICON
425.7		
509.4		
608.8		
727.9		
870.9		
1041.5		
1245.3		
1489.4		

Fig. 4.5 Response of Reticon for increasing frequency

FREQ. IN HZ.	INPUT OF RETICON	OUTPUT OF RETICON
1760.4		
2101.1		
2511.7		
3002.8		
3592.8		
4296.3		
5136.9		
6143.7		

CHAPTER V

APPLICATIONS

One of the major applications of the Spectrum Analyzer is as a noise and vibration analyzer. Rotating machinery can be noisy and can suffer from excessive vibration. Noise is generally irritating while vibration may cause premature failure. The MC68701 based Spectrum Analyzer can be used to resolve complex noise and vibration signals into constituent signals as a function of frequency, thereby generating a spectrum. This spectrum can be evaluated, in terms of amplitude, for predominant frequency components. Such tracing of noise or vibration sources allows corrective measures to be applied most effectively. One such method would be to take the base line signature of the vibration of any machine; this could be filed, and periodically recorded data could then be compared to the base line signature to see if significant variations have occurred. If such variations are observed then corrective action has to be applied before total breakdown occurs. Changes in the vibration level of machines indicate changes in the condition of the machine. Vibrations level increase as the machine deteriorates, parts work loose and bearing wear increases. As a result the noise level also increases, and this could serve as an early warning and enable effective maintenance and overhaul to be planned before breakdown.

Measurements made for a diagnosis of machine vibration depend upon the access to the machine and operating speed range. In the process of identification of machine faults it is

advisable to take and analyze as much data as possible. Such data can be used for fault identification and fault correction. This data can be used in problem solution or used as supporting information for any calculations that are needed to be made. The MC68701 based Spectrum Analyzer can be used for the acquisition of the data.

Another important application of the analyzer would be to use it for measuring acoustic intensity of engine noise and to evaluate the radiation of noise from vehicles. The dynamic forces generated within engines give rise to vibrations which are either adsorbed or transmitted through the engine structure. Those vibrations which transmit to the engine surface are then converted in part to pressure waves within the medium that surrounds the engine. Some of these waves are of resistive nature which propagate to the acoustic field and become the radiated noise emission of the engine. A study conducted by General Motors [17] for the measurements of noise emitted from engines, reveals that the directivity of noise radiated from engine/chassis systems, could be improved considerably by having two closely-spaced microphones to record the noise. The report in its findings states that acoustic intensity is related to the cross spectrum between the acoustic pressures of the two microphones used. This has facilitated in the development of a practical method of measuring acoustic intensity.

One more specific application of this analyzer could be in measuring the noise level in a grain elevator. In a grain

elevator there exist abundant machinery and that includes a lot of moving parts. As a result, a great deal of noise is generated. This noise can be periodically examined to see if the noise spectrum is as expected. If found to be different, this could be an early indication of component failures or improper operating conditions. Corrective actions are implemented to prevent permanent damages.

Discussed above are only a few of the many applications of the Spectrum Analyzer. This analyzer can be used in any noisy environment to serve as an early indicator of possible failures.

CHAPTER VI

OPERATING PROCEDURE

1. Connect the appropriate power supplies. Power supplies needed are +10 volts, -10 volts and +5 volts.
2. Connect the RS-232C link between the interface board and the computer to the second serial port of the NorthStar computer.
3. Connect the microphone to the input socket provided for it on the input analog section. Care should be taken to see that the microphone is placed as near as the noise source as possible without touching it.
4. Switch on the power to the computer system and load the Spectrum Analyzer program.
5. Switch on the power to the Spectrum Analyzer board and 'Reset' the system once before operation starts.
6. Type 'RUN' to execute the Spectrum Analyzer program. The noise levels in db corresponding to the various frequencies is obtained.
7. Plot the spectrum on the HP86B computer using the 'LOGPLOT' routine available on it. First an input data file has to be created with the all the frequency and db values being supplied. Then the 'LOGPLOT' routine is executed to obtain the spectrum of the noise source.

If the above enlisted steps are followed faithfully, the spectrum of the source can be obtained very easily.

BIBLIOGRAPHY

1. Nagbushan K. Bhaskara, Motorola 68701 Microcomputer Interface for the HP6940B Multiprogrammer, A Master's Report, 1983.
2. Neufito L. Fernandes, An Automated Laboratory Test System, A Master's Report, 1983.
3. Andrew C. Staugaard Jr., 6801, 68701, 6803 Microcomputer Programming and Interfacing.
4. Joseph J. Carr, Designing Microprocessor-Based Instrumentation, Prentice Hall Inc., 1982.
5. John B. Peatman, Microprocessor-Based Design, McGraw-Hill Inc., 1977.
6. Malmstadt, Enke and Crouch, Electronics and Instrumentation for Scientists, The Benjamin/Cummings Publishing Co., 1981.
7. Bernard Grob, Electronic Circuit and Applications, McGraw-Hill Book Company Inc., 1982.
8. Motorola MC68701 Microcomputer Unit Manual, Motorola Inc., 1980.
9. Motorola Lilbug Monitor for the MC6801LL1, Motorola Inc., 1980.
10. Motorola Single-Chip Microcomputer Data Manual, Motorola Inc., 1981.
11. Motorola Microprocessors Data Manual, Motorola Inc., 1981.
12. CMOS Databook, National Semiconductor Corporation, 1981.
13. MC68701 Programmer Manual, ET Labs, KSU, 1983.
14. NorthStar System Software Manual #25013B, Revision 2.1, 1980, NorthStar Computers Inc., 1440 Fourth Street, Berkeley, CA94710.
15. Okidata Microline 82A User's Manual, Okidata Corp., Mt.

Laurel, New Jersey 08054.

16. TI 700 Silent Printer, Model 743 KSR Data Terminal Operating Instructions, Texas Instruments Inc., Digital Systems Division, P.O. Box 1444, Houston, Texas 77001.
17. Dwight A. Blaser and Douglas A. Feldmaier, Research Publication on "Acoustic Intensity Measurements of Noise Emission from Engines", Engineering Mechanics Department, Oct. 11, 1981, General Motors Research Laboratories, Warren, MI 48090.

ACKNOWLEDGEMENTS

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I would like to express my heartfelt thanks to Dr. Gary Jonhson for allowing me to use his spinwriter and computer.

I express my gratitude towards my parents whose encouragement and constant support has contributed towards the successful completion of my graduate program.

Thanks are also due to my colleagues and friends for all their help, support and inspiration.

Appendix I

1. Cross assembler listing for the MC68701.
2. Program listing for the Spectrum Analyzer in North Star BASIC.

[illegible]

2. NorthStar program for the Spectrum Analyzer

This is the NorthStar program in BASIC entitled "SPAN" for the Spectrum Analyzer. This program provides the word pattern for the various frequencies and gets back the value of the input signal at each of those frequencies. It then calculates the decibel value of the signal and prints out the frequency and the corresponding decibel value.

```
10 DIM F(40),X(40),B(40)
```

```
20 F(17)=6143.7
```

```
30 F(18)=5136.9
```

```
40 F(19)=4296.3
```

```
50 F(20)=3592.8
```

```
60 F(21)=3002.8
```

```
70 F(22)=2511.7
```

```
80 F(23)=2101.1
```

```
90 F(24)=1760.4
```

```
100 F(25)=1489.4
```

```
110 F(26)=1245.3
```

```
120 F(27)=1041.5
```

```
130 F(28)=872.0
```

```
140 F(29)=727.9
```

```
150 F(30)=608.9
```

```
160 F(31)=509.4
```

```
170 F(32)=425.7
```

```
180 FOR I=17 TO 32 STEP 1
```

```
190 PRINT#1,"&",I*256,"$"
200 FOR J=1 TO 1000
210 NEXT J
220 INPUT#1,"?",A$
230 X(I)=VAL(A$)
240 B(I)=20*(LOG(X(I))/2.3)
250 PRINT" ",F(I)," ",B(I)
260 NEXT I
270 END
```

Appendix II

1. Data sheets for the MC68701 Microcomputer chip.
2. Data sheets for the ADC0816 A/D chip.
3. Data sheets for the Reticon switched capacitor filter.


MOTOROLA

MC68701

Advance Information

MC68701 MICROCOMPUTER UNIT (MCU)

The MC68701 is an 8-bit single chip microcomputer unit (MCU) which significantly enhances the capabilities of the M6800 family of parts. It can be used in production systems to allow for easy firmware changes with minimum delay or it can be used to emulate the MC6801/03 for software development. It includes an upgraded M6800 microprocessor unit (MPU) with upward source and object code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned multiply. The MCU can function as a monolithic microcomputer or can be expanded to a 64K byte address space. It is TTL compatible and requires one +5 volt power supply for nonprogramming operation. An additional Vpp power supply is needed for EPROM programming. On-chip resources include 2048 bytes of EPROM, 128 bytes of RAM, Serial Communications Interface (SCI), parallel I/O, and a three function Programmable Timer. A summary of MCU features includes:

- Enhanced MC6800 Instruction Set
- 8 x 8 Multiply Instruction
- Serial Communications Interface (SCI)
- Upward Source and Object Code Compatibility with the MC6800
- 16-Bit Three-Function Programmable Timer
- Single-Chip or Expanded Operation to 64K Byte Address Space
- Bus Compatibility with the M6800 Family
- 2048 Bytes of UV Erasable, User Programmable ROM (EPROM)
- 128 Bytes of RAM (64 Bytes Retainable on Powerdown)
- 29 Parallel I/O and Two Handshake Control Lines
- Internal Clock Generator with Divide-by-Four Output
- -40 to 85°C Temperature Range

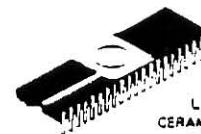
GENERIC INFORMATION

Package Type	Frequency (MHz)	Temperature	Generic Number
Ceramic L Suffix	1.0	0°C to 70°C	MC68701L
	1.0	-40°C to 85°C	MC68701CL
	1.25	0°C to 70°C	MC68701L-1
	1.25	-40°C to 85°C	MC68701CL-1
	1.5	0°C to 70°C	MC68A701L
	2.0	0°C to 70°C	MC68B701L

MOS

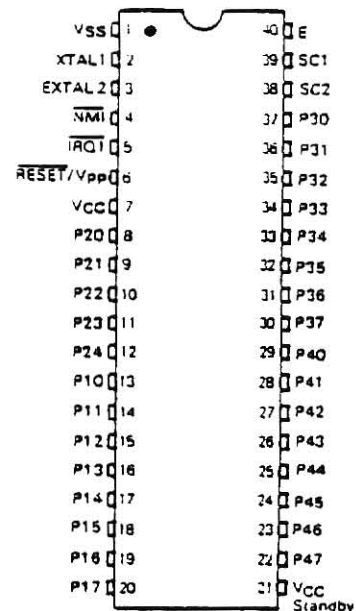
(N-CHANNEL, SILICON-GATE,
DEPLETION LOAD)

MICROCOMPUTER WITH EPROM



L SUFFIX
CERAMIC PACKAGE
CASE 715

PIN ASSIGNMENT



MC68701

CONTROL TIMING ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0$, $T_A = 0$ to 70°C)

Characteristic	Symbol	MC68701		MC68701-1		MC68A701		MC68B701		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Frequency of Operation	f_0	0.5	1.0	0.5	1.25	0.5	1.5	0.5	2.0	MHz
Crystal Frequency	f_{XTAL}	2.0	4.0	2.0	5.0	2.0	6.0	2.0	8.0	MHz
External Oscillator Frequency	f_0	2.0	4.0	2.0	5.0	2.0	6.0	2.0	8.0	MHz
Crystal Oscillator Start Up Time	t_{rc}	—	100	—	100	—	100	—	100	ms
Processor Control Setup Time	t_{PCS}	200	—	170	—	140	—	110	—	ns

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ Vdc} \pm 5\%$, $V_{SS} = 0$, $T_A = T_L$ to T_H , unless otherwise noted)

Characteristic	Symbol	MC68701			MC68701C			Unit	
		Min	Typ	Max	Min	Typ	Max		
Input High Voltage RESET Other Inputs *	V_{IH}	$V_{SS} + 4.0$ $V_{SS} - 2.0$	—	V_{CC} V_{CC}	$V_{SS} + 4.0$ $V_{SS} + 2.2$	—	V_{CC} V_{CC}	V	
Input Low Voltage RESET Other Inputs *	V_{IL}	$V_{SS} - 0.3$ $V_{SS} - 0.3$	—	$V_{SS} + 0.4$ $V_{SS} + 0.8$	$V_{SS} - 0.3$ $V_{SS} - 0.3$	—	$V_{SS} - 0.4$ $V_{SS} - 0.8$	V	
Input Current, See Note ($V_{in} = 0$ to 2.4 V)	Port 4 SCI	— I_{in}	— —	0.6 1.0	— —	— —	1.0 1.6	mA	
Input Current ($V_{in} = 0$ to 5.25 V)	NMI, IRQ1	I_{in}	—	1.5	2.5	—	1.5	5	μ A
Input Current ($V_{in} = 0$ to 0.4 V) ($V_{in} = 4.0$ V to V_{CC})	RESET/Vpp	I_{in}	—	-2.0	—	—	-2.0	—	mA
High-Z (OH State) Input Current ($V_{in} = 0.5$ to 2.4 V)	Ports 1, 2, and 3	I_{TSI}	—	2	10	—	2	20	μ A
Output High Voltage ($I_{Load} = -55 \mu$ A, $V_{CC} = \text{Min}$) ($I_{Load} = -100 \mu$ A, $V_{CC} = \text{Min}$)	Port 4, SC1, SC2 Other Outputs	V_{OH}	$V_{SS} + 2.4$ $V_{SS} + 2.4$	— —	— —	$V_{SS} + 2.4$ $V_{SS} + 2.4$	— —	— —	V
Output Low Voltage ($I_{Load} = 2.0$ mA, $V_{CC} = \text{Min}$)	All Outputs	V_{OL}	—	—	$V_{SS} + 0.5$	—	—	$V_{SS} + 0.6$	V
Darlington Drive Current ($V_O = 1.5$ V)	Port 1	I_{OH}	1.0	2.5	10.0	1.0	2.5	10.0	mA
Internal Power Dissipation (Measured at $T_A = T_L$ in Steady-State Operation)	P_{INT}	—	—	1500	—	—	1500	mW	
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f_0 = 1$ MHz)	Port 3, Port 4, SCI Other Inputs	C_{in}	— — —	— — —	12.5 — 10.0	— — —	— — 10.0	— — 12.5	pF
V_{CC} Standby	Powerdown Powerup	V_{SBB}	4.0 4.75	— —	5.25 5.25	4.0 4.75	— —	5.25 5.25	V
Standby Current	Powerdown	I_{SBB}	—	—	11.0	—	—	8.0	mA
Programming Time Per Byte ($T_A = 25^\circ\text{C}$)	t_{pp}	25	—	50	25	—	50	ms	
Programming Voltage ($T_A = 25^\circ\text{C}$)	V_{pp}	20.0	21.0	22.0	20.0	21.0	22.0	V	
Programming Current ($V_{RESET} = V_{pp}$, $T_A = 25^\circ\text{C}$)	I_{pp}	—	30	50	—	30	50	mA	

* Except mode programming levels; see Figure 15.

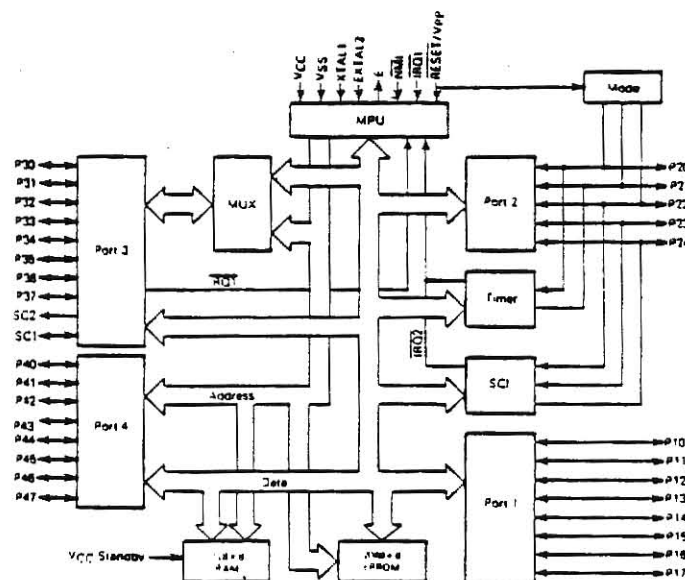
NOTE: RESET/Vpp I_{in} differs from MC6801 and MC6803 values.

PERIPHERAL PORT TIMING (Refer to Figures 3-6)

Characteristics	Symbol	MC68701		MC68701-1		MC68A701		MC68B701		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Peripheral Data Setup Time	t_{POSH}	200	—	200	—	150	—	100	—	ns
Peripheral Data Hold Time	t_{PODH}	200	—	200	—	150	—	100	—	ns
Delay Time, Enable Positive Transition to \overline{CS} Negative Transition	t_{QSD1}	—	350	—	350	—	300	—	250	ns
Delay Time, Enable Positive Transition to \overline{CS} Positive Transition	t_{QSD2}	—	350	—	350	—	300	—	250	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid	t_{PVD}	—	350	—	350	—	300	—	250	ns
Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid	t_{CMOS}	—	2.0	—	2.0	—	2.0	—	2.0	μs
Input Strobe Pulse Width	t_{PWIS}	200	—	200	—	150	—	100	—	ns
Input Data Hold Time	t_{IH}	50	—	50	—	40	—	30	—	ns
Input Data Setup Time	t_{IS}	20	—	20	—	20	—	20	—	ns

MC68701

MC68701 MICROCOMPUTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{in}	-0.3 to +7.0	V
Operating Temperature Range MC68701 MC68701C	T _A	T _L to T _H 0 to 70 -40 to 85	°C
Storage Temperature Range	T _{stg}	0 to 85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{CC}. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance Ceramic Package	θ _{JA}	50	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT} + P_{PORT}

P_{INT} = I_{CC} × V_{CC}, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications P_{PORT} < P_{INT} and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J - 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D - (T_A + 273^\circ\text{C}) + \theta_{JA} P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.



A to D, D to A

ADC0816, ADC0817 8-Bit μ P Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16 single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE[®] outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin,

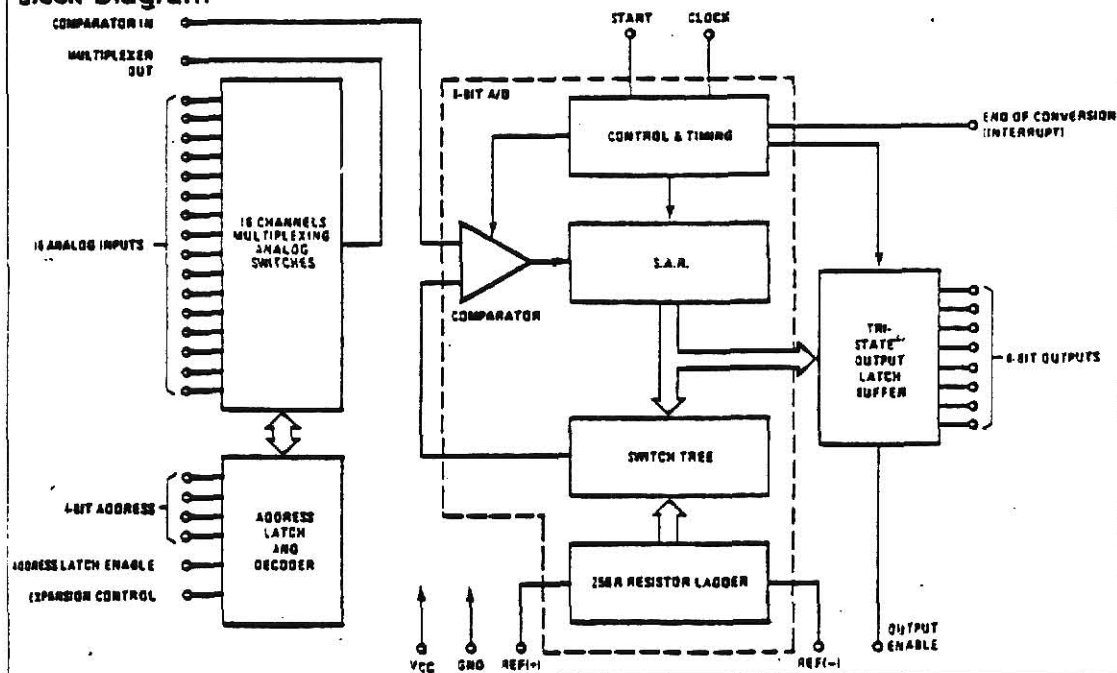
8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution — 8-bits
- Total unadjusted error — $\pm 1/2$ LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μ s
- Single supply — 5 V_{CC}
- Operates ratiometrically or with 5 V_{CC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T²L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range —40°C to +85°C or —55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE[®] output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

[®]TRI-STATE[®] is a registered trademark of National Semiconductor Corp.

Block Diagram



ADC0816, ADC0817

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	5.5V
Voltage at Any Pin Except Control Inputs	-0.3V to ($V_{CC} + 0.3V$)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	-0.3V to 15V
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	375 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0816CJ	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Range of V_{CC} (Note 1)	4.5V to 5.5V
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: $V_{CC} = 5V_{DC} = V_{REF(+)}$, $V_{REF(-)} = \text{GND}$, $V_{IN} = V_{\text{COMPARATOR IN}}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640 \text{ kHz}$ unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
ADC0816 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			$\pm 1/2$ $\pm 3/4$	LSB LSB
ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			± 1 $\pm 1 1/4$	LSB LSB
Input Resistance	From $\text{Ref}(+)$ to $\text{Ref}(-)$	1.0	4.5		k Ω
Analog Input Voltage Range	(Note 4) $V(+)$ or $V(-)$	$\text{GND}-0.10$		$V_{CC}+0.10$	V_{CC}
$V_{REF(+)}$ Voltage, Top of Ladder	Measured at $\text{Ref}(+)$		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$ Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$ Voltage, Bottom of Ladder	Measured at $\text{Ref}(-)$	-0.1	0		V
Comparator Input Current	$f_c = 640 \text{ kHz}$, (Note 6)	-2	± 0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ $4.5V \leq V_{CC} \leq 5.5V$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise noted.
ADC0816CCJ, ADC0816CCN, ADC0817CCN $4.75V \leq V_{CC} \leq 5.25V$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER					
R_{ON} Analog Multiplexer ON Resistance	(Any Selected Channel) $T_A = 25^\circ\text{C}$, $R_L = 10\text{k}$ $T_A = 65^\circ\text{C}$ $T_A = 125^\circ\text{C}$		1.5	3 6 9	k Ω k Ω k Ω
ΔR_{ON} Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10\text{k}$		75		Ω
$I_{OFF(+)}$ OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$ OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}	-200 -1.0			nA μA
CONTROL INPUTS					
V_{INH} Logical "1" Input Voltage		$V_{CC}-1.5$			V
V_{INL} Logical "0" Input Voltage				1.5	V
I_{INH} Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	μA
I_{INL} Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	-1.0			μA
I_{CC} Supply Current	$f_{CLK} = 640 \text{ kHz}$		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ — $4.5V < V_{CC} < 5.5V$, $-55^{\circ}C < T_A < +125^{\circ}C$ unless otherwise noted.
 ADC0816CCJ, ADC0816CCN, ADC0817CCN — $4.75V < V_{CC} < 5.25V$, $-40^{\circ}C < +85^{\circ}C$ unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
DATA OUTPUTS AND EOC (INTERRUPT)					
$V_{OUT(1)}$	Logical "1" Output Voltage $I_O = -380\mu A$, $T_A = 85^{\circ}C$ $I_O = -300\mu A$, $T_A = 125^{\circ}C$	$V_{CC} - 0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage $I_O = 1.8\text{ mA}$			0.45	V
$V_{OUT(EOC)}$	Logical "0" Output Voltage EOC $I_O = 1.2\text{ mA}$			0.45	V
I_{OUT}	TRI-STATE [®] Output Current $V_O = V_{CC}$ $V_O = 0$	-3.0		3.0	μA μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20\text{ ns}$ and $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(Figure 5)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(Figure 5)		100	200	ns
t_s	Minimum Address Set-Up Time	(Figure 5)		25	50	ns
t_h	Minimum Address Hold Time	(Figure 5)		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ (Figure 5)		1	2.5	μs
$t_{HD} t_{HS}$	OE Control to Q Logic State	$C_L = 50\text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
$t_{HD} t_{OH}$	OE Control to HI-Z	$C_L = 10\text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
t_c	Conversion Time	$f_c = 640\text{ kHz}$, (Figure 5) (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(Figure 5)	0		$8 + 2\mu s$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE [®] Output Capacitance	At TRI-STATE Outputs. (Note 7)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A Zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of $7 V_{CC}$.

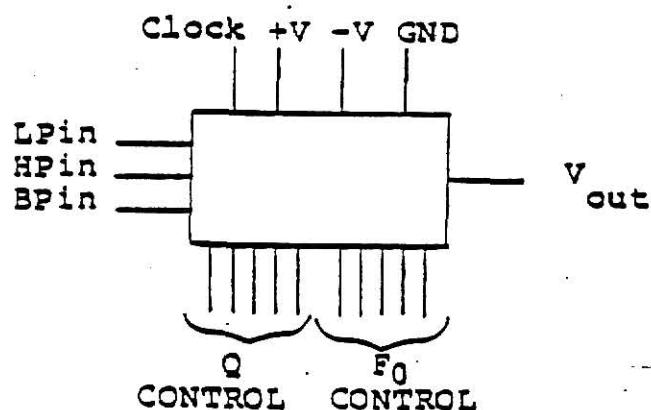
Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply range by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{CC} to $5 V_{CC}$ input voltage range will therefore require a minimum supply voltage of $4.900 V_{CC}$ over temperature variations, initial tolerances and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See Figure 3. None of these A/Ds requires a zero or full-scale adjust. However, if an accurate code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 12.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

3. Data sheets for the Reticon SCF



V _{ss}	(1	18)	HPin
Q ₀	(2	17)	F ₀₀
Q ₁	(3	16)	F ₀₁
Q ₂	(4	15)	F ₀₂
Q ₃	(5	14)	F ₀₃
Q ₄	(6	13)	F ₀₄
Clock	(7	12)	V _{out}
GND	(8	11)	V _{DD}
BPin	(9	10)	LPin

RS620 Pin Out Diagram

Functional block diagram of

RS620

TABLE I Filter Select Table

Filter Type	Connections		
	LPin	HPin	BPin
Lowpass	Vin	GND	GND
Highpass	GND	Vin	GND
Bandpass	GND	GND	Vin
Notch	Vin	Vin	GND
All-pass	Vin	Vin	Vin
Sine Wave *	GND	GND	Vout
Oscillator			

* Q must be set to 11101 for oscillator mode operation.

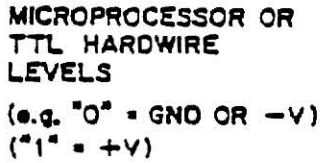


Figure 5 R5620 Test Circuit

TABLE II R5820 Q, F₀ Programming Table

Q	CODE Q ₄ ...Q ₀	F _C /F ₀	CODE F ₀₄ ...F ₀₀
.57	00000	200.0	00000
.65	00001	191.3	00001
.71	00010	182.9	00010
.79	00011	174.9	00011
.87	00100	167.2	00100
.95	00101	159.9	00101
1.05	00110	152.9	00110
1.2	00111	146.2	00111
1.35	01000	139.8	01000
1.65	01001	133.7	01001
1.95	01010	127.9	01010
2.2	01011	122.3	01011
2.5	01100	116.9	01100
3.0	01101	111.8	01101
3.5	01110	106.9	01110
4.25	01111	102.3	01111
5.0	10000	97.8	10000
5.8	10001	93.5	10001
7.2	10010	89.4	10010
8.7	10011	85.5	10011
10.0	10100	81.8	10100
11.5	10101	78.2	10101
13.0	10110	74.8	10110
15.0	10111	71.5	10111
17.5	11000	68.4	11000
19.0	11001	65.4	11001
23.0	11010	62.5	11010
* 28.0	11011	59.8	11011
* 35.0	11100	57.2	11100
* 40.0	11101	54.8	11101
* 80.0	11110	52.3	11110
* 150.0	11111	50.0	11111

*These values are maximum. Minimum values are greater than $\frac{1}{2}$ Q. All other Q have a tolerance of $\pm 10\%$ and typically are within a few percent.

TABLE IV
PERFORMANCE STANDARDS*

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Clock to Center Frequency Ratio (7)	F_c/F_0 ($=2 \times f_s/f_0$)		See Table II		
Q: (7)			See Table II		
Supply Current	I_D		4.5		mA
Maximum output current	I_o		4		mA
Output Voltage Swing $Q \geq 1$	V_{out}		14		volts p-p
Output Noise (5) $Q=1$			270		μV
Dynamic Range (6) $Q=1$ $Q=40$			94 84		dB
Total Harmonic Distortion (6) @ 1 KHz			0.2		%
Insertion Loss			0		dB

* $V_+ = +10V$, $V_- = -10V$, $f_0 = 2$ KHz, $25^\circ C$

- (1) All devices are internally gate-protected for static immunity. Applying AC signals or clock to chip with power off may exceed negative limit.
- (2) Trigger voltage is referenced to ground (TTL compatible).
- (3) For low-end Q values, the external clock rate may be extended to 2 MHz.
- (4) Sample rate = 1/2 external master clock rate.
- (5) Broadband to one-half the sample rate.
- (6) 14 Volts p-p input.
- (7) Q and f_c/f_0 control lines and clock are TTL or CMOS compatible.

THE MC68701 BASED SPECTRUM ANALYZER

by

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B.E., College of Engineering-Madras, India, 1981

M.E., Madras Institute of Technology, India, 1983

AN ABSTRACT OF A MASTER'S REPORT

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

KANSAS STATE UNIVERSITY

Manhattan, Kansas

1985

ABSTRACT

A system to determine and plot the audio spectrum of a noise source has been designed and developed. The system makes use of the Motorola MC68701 microcomputer chip to provide communication between the input analog signal and any computer which uses the RS-232C standard. The computer in this instance is the NorthStar computer. In operation, the input audio signal is fed via microphones to the input analog section. Here, the signals are amplified, filtered, converted to a DC value and then fed to an analog to digital converter. The start convert signal to the A/D converter is supplied by the MC68701. After conversion, the data is passed on to the MC68701, where it is converted from binary to BCD to ASCII and sent serially to the computer. At the computer end the data is received and the decibel value of the signal is computed. The computed values are then plotted against frequency to obtain the audio spectrum.