NITROGEN IMPLANTATION IN N-TYPE AND P-TYPE SILICON

by

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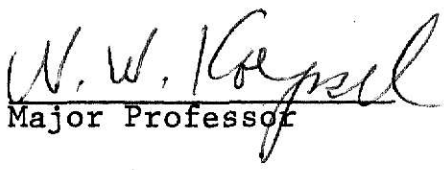

Major Professor

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CHAPTER I

INTRODUCTION

1.1 Background

The changes in physical property of a solid target specimen by bombordment with a flux of energetic atomic particles, has been known for several decades. During the 1930's nuclear physicists made use of an early ion accelerator which was available to them, but they failed to observe visible modifications of certain target materials. If they made any observation, it was regarded as a troublesome side-effect. In the early 1940's when nuclear reactors were developing, the situation became different. E. P. Wigner (1) in 1942 studied the theoretical aspects of the materials which were for the first time subjected to intense irradiation by fast neutrons.

New studies in the growing field of nuclear physics soon led to the knowledge of the energy of an ion penetrating to different depths of a solid target. This led to the theory of ion penetration through matter. This concept was first identified by Bohr (2) in 1948.

The idea of introducing impurities into semiconductors was first initiated by R. S. Ohl (3) in 1952; and in 1954, Shockley (4) filed a patent in which he used an ion beam to produce highly controlled semiconductor materials. The first attempt to implant a conventional dopant into semiconductors appears to

have been done in 1955 by Cussins (5). He was able to form the p-type conductivity, but the effect seemed to disappear after 500 ^{o}C anneal. After Cussins' work, the field appears to have slowed down until 1961 when Alvager and Hansen (6) made the first practical device that depended on the chemical properties of implanted ions.

A slow but steady series of publications continued to appear. Some advantages of ion implantation were realized; but the properties of junction produced were not reported, and no reference was made to annealing. These publications were widely read and studied, and this stimulated the interest of scientists who were studying ways of improving junction devices in silicon.

Ion implantation for use in industry was initiated with the early work at the Ion Physics Corporation in Massachusetts. Lack of close communication between the semiconductor device industries hindered the development of new technology. Then it was perhaps natural that the next stimulus should come from laboratories which were exploring the use of ion beams in research.

Much of the attractiveness of implantation comes from the fact that the dopant ion may be of any species which can be produced in an ion source. The large degree of control which the researchers have over the ion energy, as well as their control over the substrate parameters such as temperature and orientation, affords them a high degree of regulation over the penetration depth and the concentration profile of implanted ions. Ion implantation provides an alternative method of introducing

dopant atoms into the lattice. For example, a dopant can be implanted at temperatures at which normal diffusion is completely negligible. Thus, one potential application of ion implantation is that it might allow the investigation of the properties of species which cannot be introduced into semiconductors by conventional means.

The major factors governing the successful exploration of ion implantation are the range distribution of the implanted atoms, the amount and the nature of the lattice disorder that is created, and the electrical characteristics that result from implantation and subsequent annealing treatment.

Application of ion implantation outside the semiconductor field is wide and has been explored by some researchers. But ion implantation for use outside the semiconductor field has not been fully developed yet. There are many potential areas, such as using ion implantation for studying superconductivity and corrosion which have potential in the future. It should also be mentioned here that the use of ion implantation has not been completely explored in all areas of the semiconductor electronics. One of these areas which has received some attention recently is to bombard the surface of the silicon with oxygen and nitrogen to achieve a layer of protective film.

1.2 Ion Implantation System

An ion implantation system varies widely depending on the needs of the particular application. A basic block diagram of an ion implantation system is shown in Figure 1.2.1. The type of ion beam systems that have been most fully developed are used in various areas of nuclear research. Proton and heavy-ion accelerators provide energies up to many Mev, some of them with high ion beam current. Much of this technology is applicable to ion implantation, and many of the first generation ion implantation system designs have been based on such prior work.

A typical ion implantation system is shown in Figure 1.2.2, which has an ion source in which some but not all ion species could be produced. After the ions are produced they are extracted and accelerated through a mass analyzing magnet. One important aspect of a mass analyzed ion beam that is not always fully appreciated is that only one ion species, and in some cases a particular isotope of the element, will pass through the magnet. After the ions are selected they are focused and guided to the target, where the ion beam current and the temperature of the target can be monitored.

Ion implantation systems must have the following requirements:

1. They must have a relatively high beam current.
2. This beam current must be distributed uniformly over the target.

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BLOCK DIAGRAM OF ION IMPLANATION SYSTEM

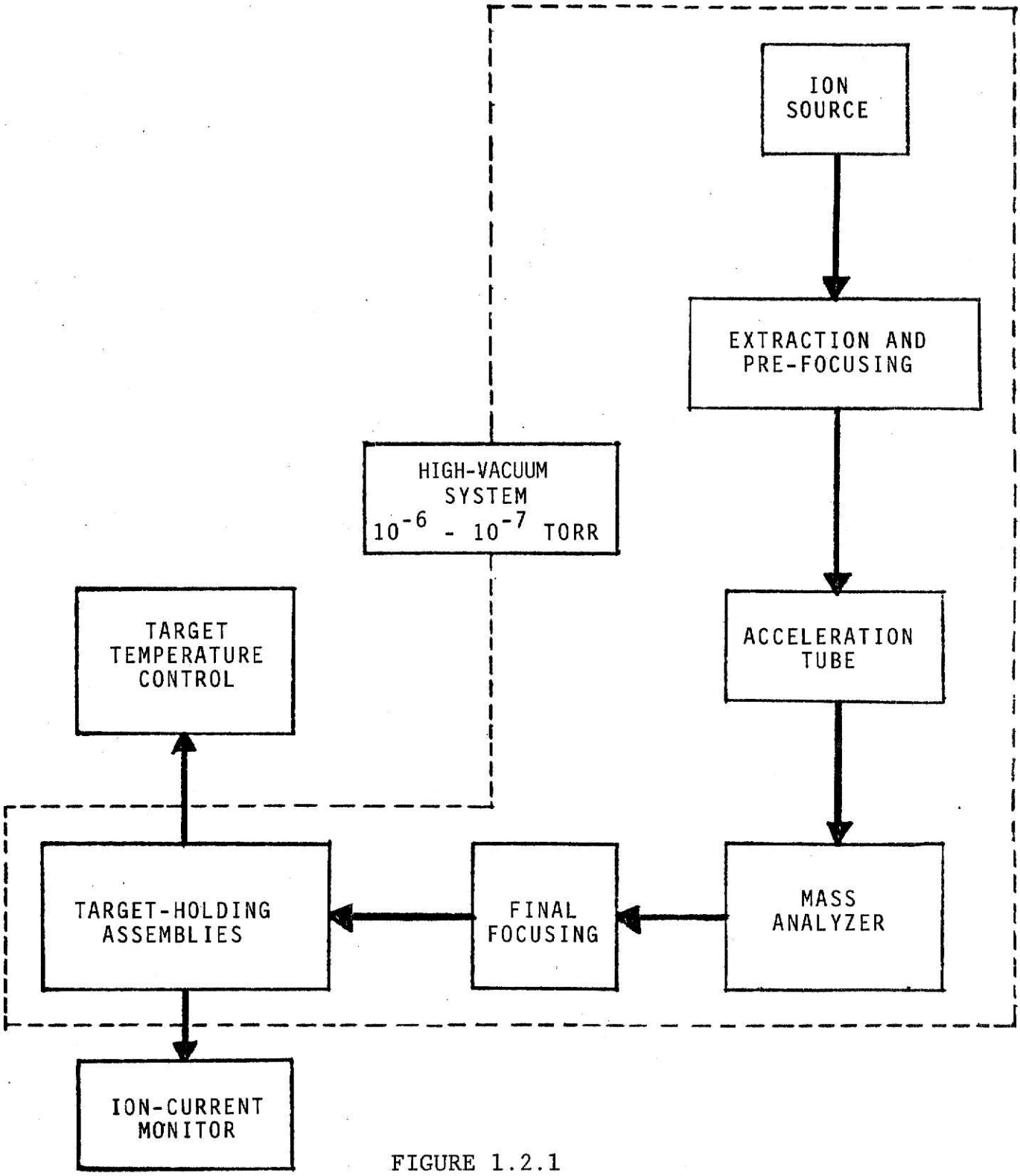


FIGURE 1.2.1

3. The equipment that is used in an ion implantation system must be operational and reliable.
4. They must be simple so that they can be operated by relatively untrained personnel.
5. Ion implantation systems must be as economical as possible.

One can differentiate two functional types of ion implantation systems -- one with much built-in flexibility in ion source, energy, etc.; and second, the type of system designed specifically for manufacturing a specific semiconductor device, that is, a system with a restricted parameter and relatively narrow capabilities. These systems are used respectivly for the research and the development of semiconductor processes and for manufacture of developed devices and integrated circuits.

The cost of a system is obviously an important factor. The cost is usually influenced primarily by the ion energy and the required pumping system. For example, if the required pumping capability is in a range of 10^{-8} TORR, the system will cost a lot more than a system with the range of 10^{-5} TORR. It should be mentioned here that there are some secondary factors that will influence the cost of a system. The choice of mass separator and the means for the beam acceleration can be considered as secondary factors. Appendix F has some definitions of the important terms which are of interest in ion implantation.

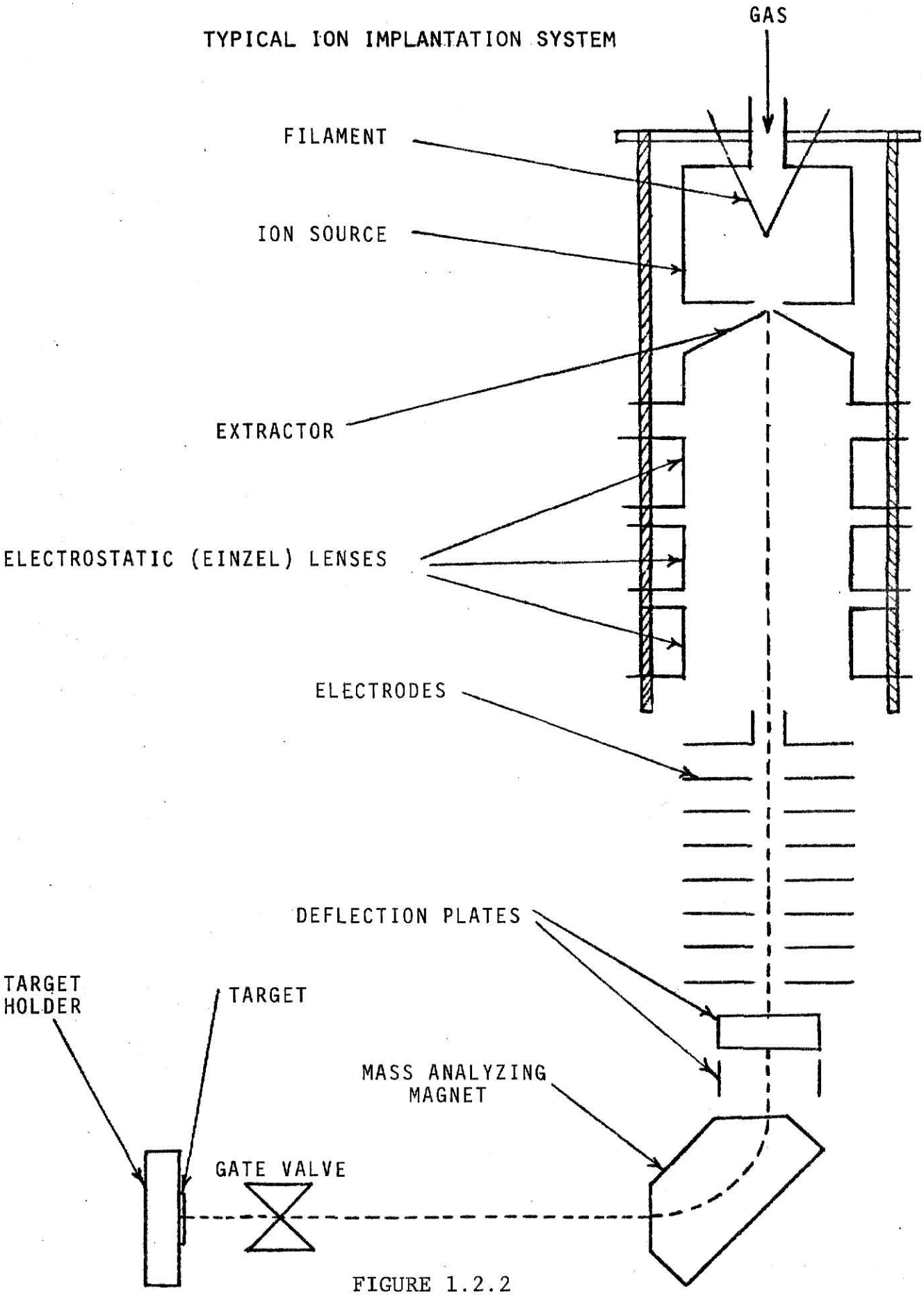

TYPICAL ION IMPLANTATION SYSTEM
GAS
FILAMENT
ION SOURCE
EXTRACTOR
ELECTROSTATIC (EINZEL) LENSES
ELECTRODES
DEFLECTION PLATES
TARGET HOLDER
TARGET
MASS ANALYZING MAGNET
GATE VALVE

FIGURE 1.2.2

1.3 Purpose of Study

The purpose of this study was to use the 600 KV Cockcroft-Walton accelerator available in the Department of Electrical Engineering at Kansas State University to implant nitrogen in both p-type and n-type silicon and find out how well the samples have been implanted using different measurements.

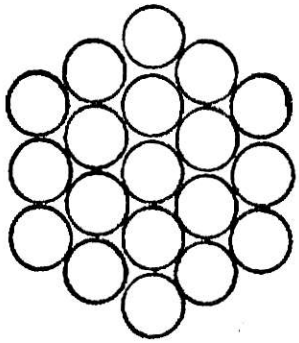
1.4 Limitation

This study was done under two limitations. First, at the time when the accelerator was used, the mass-separating magnet was not mounted which could have eliminated unwanted species. These unwanted species could have been from filament in the ion source or just double ionized or triple ionized atoms. Secondly, the nitrogen ion is not the best dopant for silicon because of its small mass.

CHAPTER II

2.1 Theory of Ion Implantation

Introduction of atoms into the surface layer of a solid substrate by bombardment of the solid with ions will change the mechanical, the electrical, the optical and the superconducting properties of that solid. Therefore, in the process of ion implantation after the energetic ion comes to rest and equilibrium has occurred, the implanted atom can be in a position in which it serves to change the electronic properties of the substrate lattice, i.e. doping occurs. Looking at a model of a crystal lattice in Figure 2.1.1, one can see that there exist in certain crystallographic directions, fairly open planes and channels among the rows of atoms. The ions from a well directed beam, when travelling toward such a channel, are able to penetrate deeply into the crystal lattice before coming to rest. The directions that allow large amounts of this channeling of the ions are limited (8). When the crystal is examined from other directions than along a channel or a plane, the atoms appear more randomly oriented. However, even when ions are injected along a non-channeling direction, it is difficult to prevent channeling completely (9). If one wishes ions to cause a semiconductor crystal to change its conduction characteristics, their introduction must result in the creation of mobile charge carriers, either electrons or holes.



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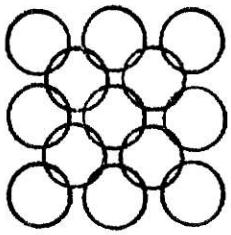

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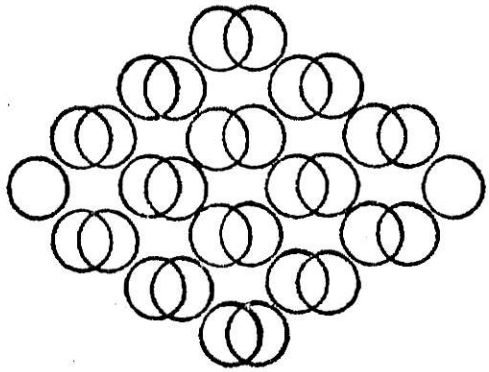


(c) <110>

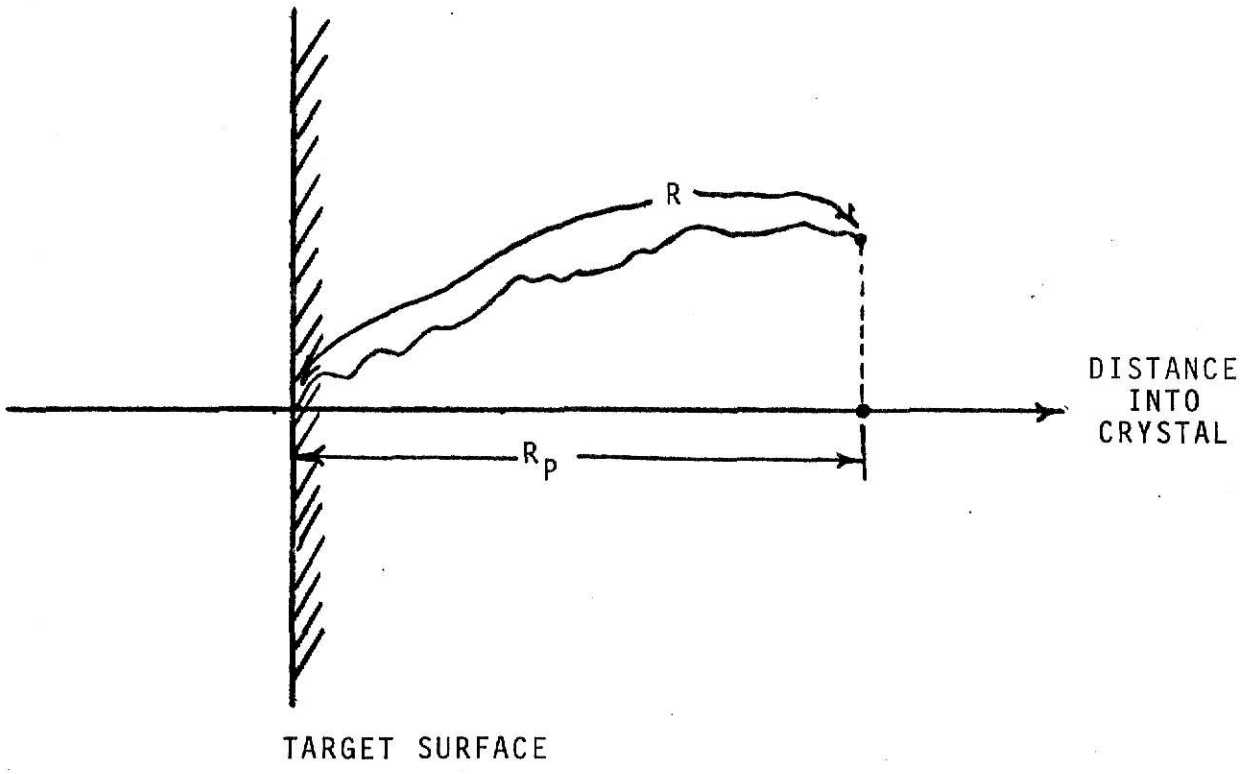
FIGURE 2.1.1 Diamond shape silicon lattice atoms

Not all ions striking the surface will pass freely down the open channels of the lattice, but many will strike the surface layer of lattice atoms. These collisions will cause dislocation of the lattice atoms within the first few hundred or thousand atomic layers of the surface (radiation damage) (10). This surface damage can, to a certain extent, be continuously annealed out by maintaining the crystal at a high enough temperature that the displaced atoms can, by thermal motion, return to lattice sites before another ion arrives in the vicinity. This temperature may be less than 250 ^{o}C for silicon for moderate ion bombardment rates.

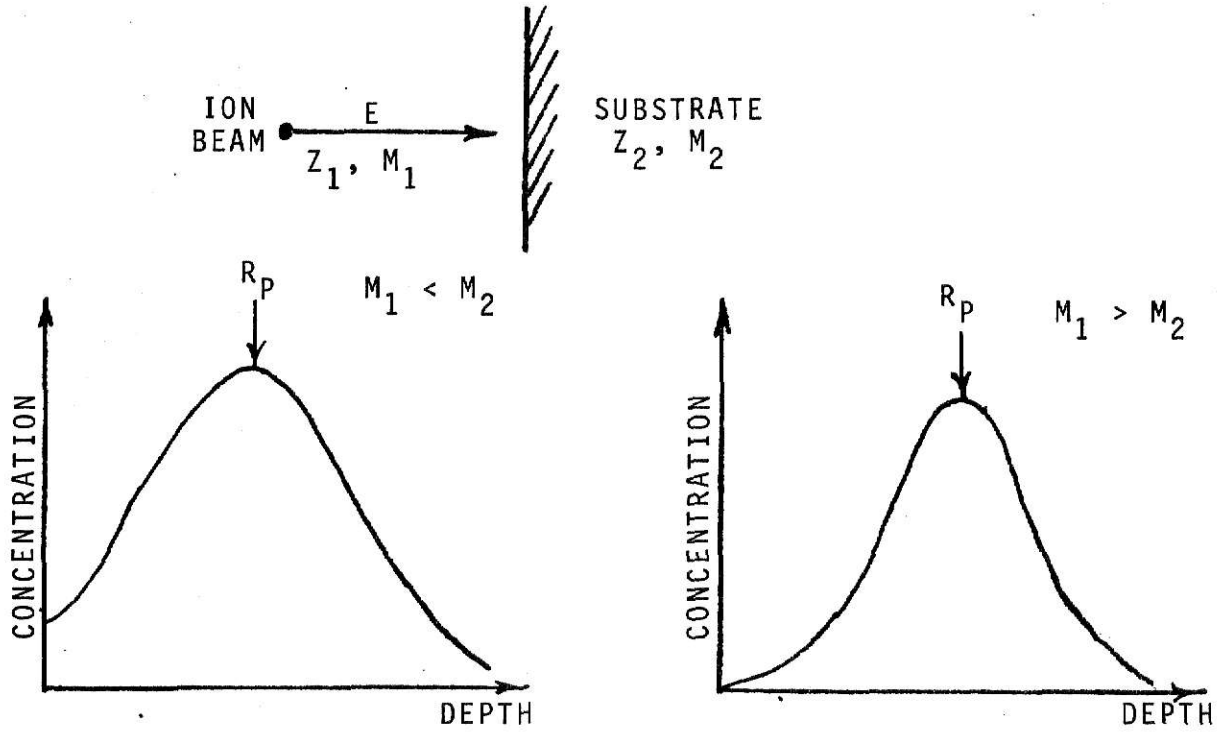
Two types of collisions occur when ions enter the surface of a substrate -- electronic collision and nuclear collision. Electronic collisions are the result of energy transfer between the electrons of the incident and the target atoms. These electrons may be excited to higher energy states or removed entirely. Nuclear collisions involve the stronger electrostatic force interactions between the nuclei of the incident and the target atoms. The effect of these two collision phenomena are called electronic stopping and nuclear stopping.

2.2 Range Distribution

A travelling ion entering a target surface will come to rest after collisions with the target nuclei and the electrons. The total distance that the ion will travel before coming to



(a) Range and Projected Range



(b) The Depth Distribution of Implanted Atoms in Amorphous Target [from Mayer 1970 (9)]

FIGURE 2.2.1

rest is called range. The projection of this distance over the direction of incidence is called projected range. The range (R) and the projected range (R_p) are shown in Figure 2.2.1 (a).

Because both the number of collisions and the energy transferred per collision are random variables, all ions of a given type and an initial energy will not have the same range. Rather, there will be a distribution of stopping points in space or a range distribution which must be characterized by a mean ion range, and a standard deviation in the ion range. The projected range must also be described statistically. The random profile according to theory (11) should be a Gaussian distribution as shown in Figure 2.2.2. The peak of the distribution is R_p from the target surface with standard deviation of ΔR_p. Therefore, one can write the Gaussian distribution for a random profile,

$$n(x) = \frac{1}{\Delta R_p \sqrt{2\pi}} \text{EXP.} \left[- \frac{(x - R_p)^2}{2(\Delta R_p)^2} \right]$$

This equation is seen to be similar to the relation for the concentration due to diffusion from a limited source (for S impurities per unit surface area).

$$n(x, t) = \frac{S}{\sqrt{\pi D_c t}} \text{EXP.} \left[- \frac{x^2}{4 D_c t} \right]$$

where D_c is the diffusion constant and t is the diffusion time. This distribution peaks at the surface (x = o) and is time dependent. Therefore, as shown above, the range distribution is approximately Gaussian in shape, and the depth distribution of

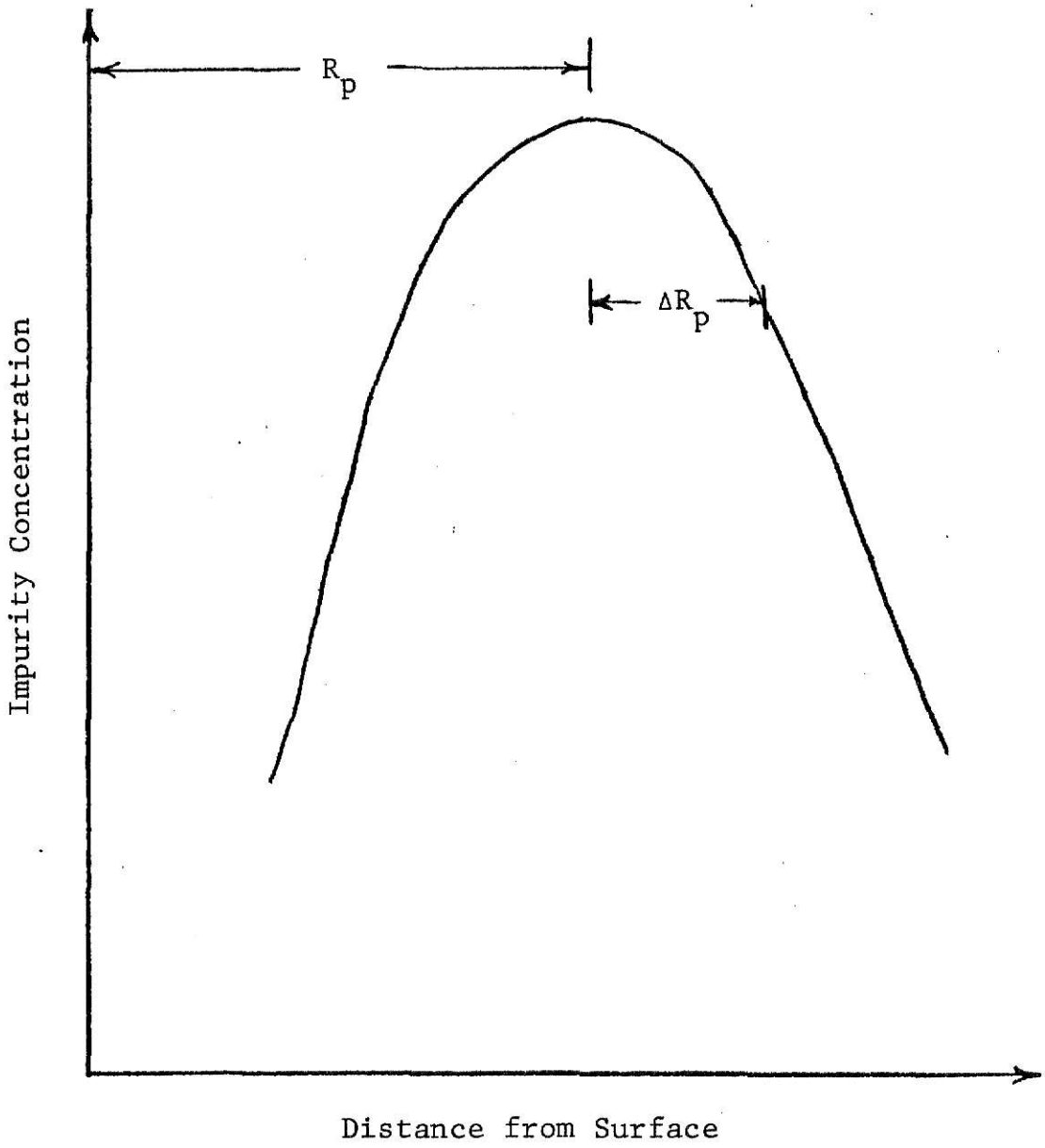


FIGURE 2.2.2 Gaussian Distribution for the Random Profile

the implanted atoms for the case in which the ion mass is greater or less than the mass of the substrate is shown in Figure 2.2.1 (b).

For reference, the corresponding equation for concentration due to diffusion from an infinite source, with a negligible initial impurity concentration, is given by

$$n(x, t) = n_o \left[1 - \text{erf}\left(\frac{x}{2\sqrt{D_c t}}\right)\right]$$

where the surface concentration of the impurity atoms is maintained by the source at n_o.

2.3 Basic Energy-Loss Equation and Projected Range Statistics

As was mentioned before, there are two forms of collisions when ions enter the surface of a target, (1) electronic collision which results when the energy transfer occurs between the electrons of the incident and the target atoms, and (2) nuclear collision which involves interaction between the nuclei of the incident and the target atoms. Therefore, there will be two energy losses associated with these collisions. It is assumed that these two forms of energy losses are independent of each other. After this assumption is made, one can write,

$$\frac{-dE}{dx} = N\left[S_n(E) + S_e(E)\right] \qquad (2.3.1)$$

where

E is the energy of the particle at a point x

$S_e(E)$ is the electronic stopping power

$S_n(E)$ is the nuclear stopping power

N is the average number of target atoms per unit volume

The equation 2.3.1 can be integrated to find the total distance R that an ion of initial energy E_o will travel before coming to rest.

$$R = \frac{1}{N} \int_o^{E_o} \frac{dE}{[S_n(E) + S_e(E)]} \qquad (2.3.2)$$

Therefore, the total range is simple to calculate but is not usually the quantities that are measured experimentally. The quantities of experimental interest are the projected range and the standard deviation of projected range.

The differential equation for computing $\bar{R}_p$ was derived by Lindhard et al. (11). The differential equation has the solution,

$$\bar{R}_p = \int_o^{E} \frac{dE'}{\beta_1(E')} \text{ EXP.} \left[\int_E^{E'} \frac{\alpha_1(x)dx}{\beta_1(x)} \right] \qquad (2.3.3)$$

For this case, the energy transfer T is small compared to the total energy of the particle where α_1, and β_1 are defined in terms of S_n and S_e:

$$\alpha_1(E) = \frac{\mu}{2} N \frac{S_n(E)}{E}$$

$$\beta_1(E) = N \left[S_n(E) + S_e(E) - \frac{\mu}{2} \frac{\Omega^2_n(E)}{E} \right]$$

and

$$\mu = \frac{M_2}{M_1}$$

$$\Omega^2_n(E) = \int_o^\infty T^2 2\pi p dp$$

where P is the impact parameter. The standard deviation $\overline{\Delta R_p}$ is also derived by Lindhard et al. (11). The values of R_p and $\overline{\Delta R_p}$ have been calculated using computers to evaluate the above integrals for several types of ions, substrates, and energies. Some of the values are shown in Table I.

2.4 Damage Creation and Channeling Effects

As was mentioned before, when ions enter the surface of a substrate before coming to rest, they make many violent collisions with the lattice atoms, removing them from their location. These displaced atoms can in turn displace others, and the result will be a very damaged area where the ions enter the substrate. Lattice disorder is shown in Figure 2.4.1 for low energy where individual regions are created and for high energy where an amorphous layer is created. Of course, the total amount of disorder and the distribution in depth depends on the ion species, the temperature, the energy, the total dose and the channeling effects.

TABLE I

Calculated value of projected range and standard deviation for various ions in silicon (from Lindhard et al.)

(values of R_p and ΔR_p are quoted in A^o)

Energy (Kev)		20	40	60	80	100	120	140
B	R_p	714	1413	2074	2695	3275	3802	4289
	(ΔR_p)	276	443	562	653	726	793	855
N	R_p	491	961	1414	1847	2260	2655	3044
	(ΔR_p)	191	312	406	479	540	590	633
Al	R_p	289	564	849	1141	1438	1737	2036
	(ΔR_p)	107	192	271	344	412	476	535
P	R_p	255	488	729	976	1228	1483	1740
	(ΔR_p)	90	161	228	291	350	405	459
Ga	R_p	155	272	383	492	602	712	823
	(ΔR_p)	37	64	88	111	133	155	176
As	R_p	151	263	368	471	574	677	781
	(ΔR_p)	34	59	81	101	122	141	161
In	R_p	133	223	304	381	456	529	601
	(ΔR_p)	23	38	51	63	75	86	97
Sb	R_p	132	221	300	376	448	519	590
	(ΔR_p)	22	36	49	60	71	82	92

Lattice Disorder

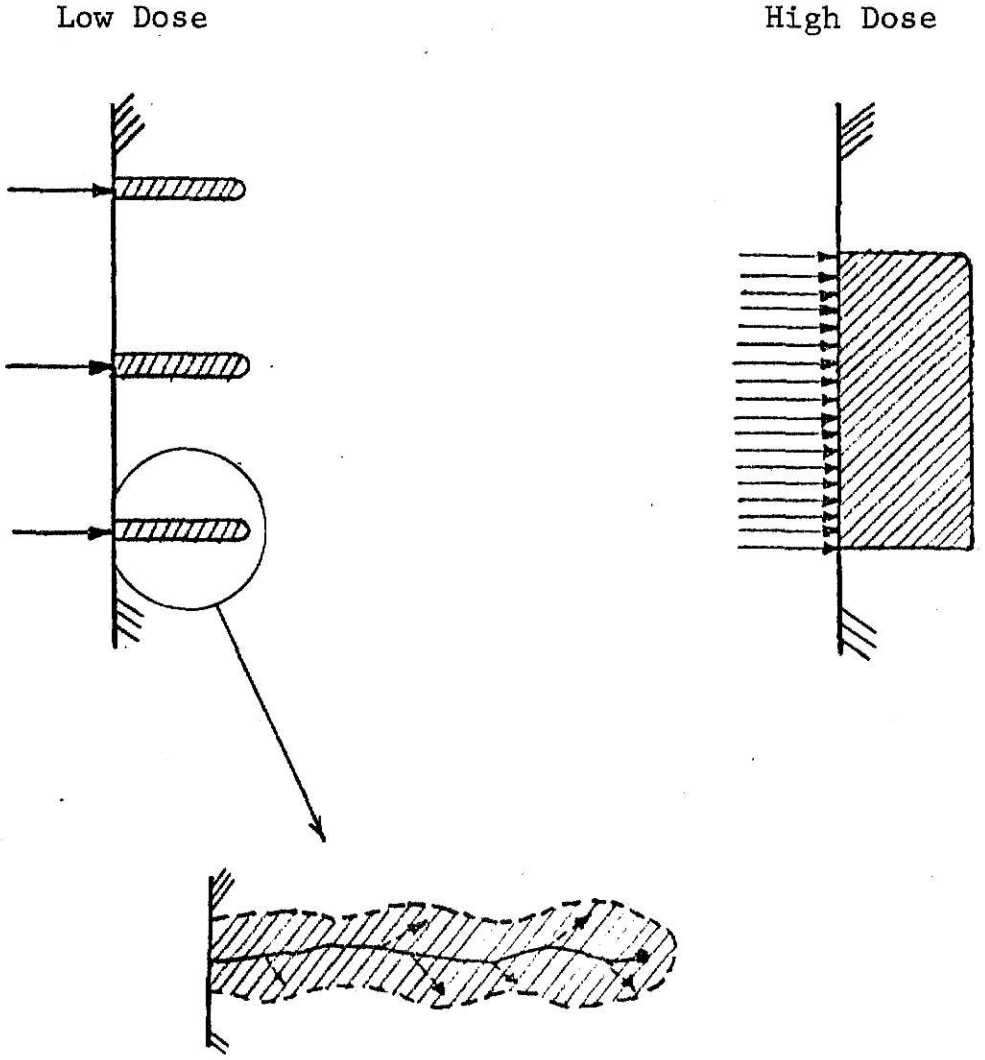


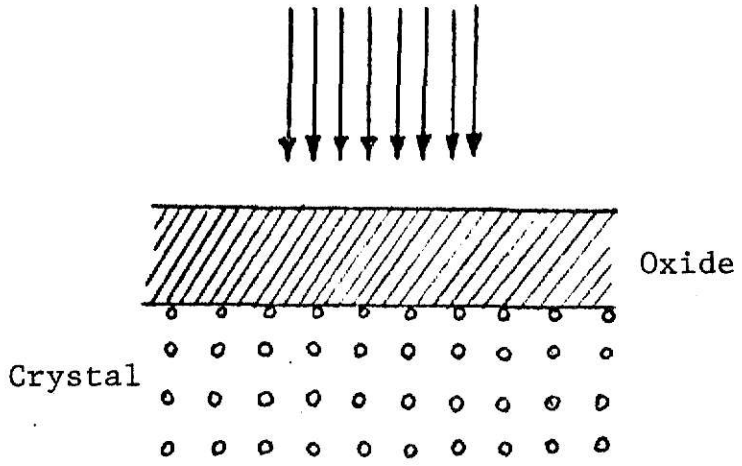
FIGURE 2.4.1 Disorder is produced in room temperature implantation. For low dose the individual regions are created and for high dose amosphous layer is created [from Mayer 1970 (9)].

Some of these disorders can be observed using a scanning electron microscope and electron diffraction. These techniques, along with some theoretical treatment of the ion interactions in a solid, have provided a tool for the evaluation of the implantation processes, but still up to this point there are many details about damage creation that is not known.

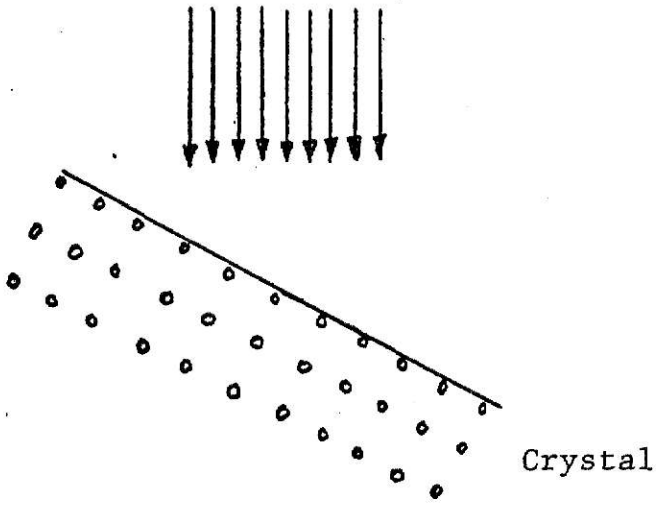
One thing that is clear is the relationship between the substrate temperature and the amount of damage that is produced in a crystal. If the temperature of the substrate is above room temperature during implantation, then the amount of damage will be lower because of the lattice vibrations. Also the total amount of energy which an incident ion transfers to the target atoms will be an important quantity in determining how much damage can be produced.

As was discussed before, channeling occurs when an incident ion, having its direction of motion aligned with a low-index crystallographic direction, undergoes a much lower rate of energy loss in the material, and so penetrates deeper inside the substrate. The channeling effect has two important consequences in ion implantation (9). One is that it influences the implanted dopant profile, and thus the junction depth. Secondly, it provides a technique for evaluating directly both the lattice location of the implanted dopant atoms and the number of displaced lattice atoms.

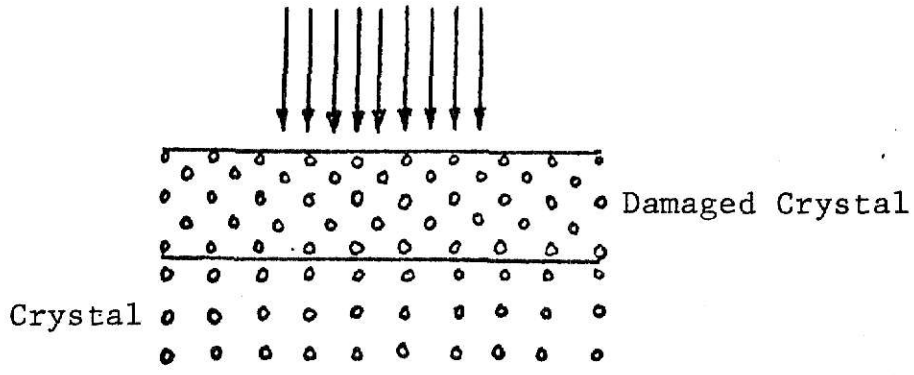
The channeling effect is very difficult to prevent in most cases, but it could be minimized if the orientation of the substrate is considered. Figure 2.4.2 illustrates three ways of



(a) Implant Through Oxide Layer



(b) Make an Angle with Beam Direction



(c) Predamage the Crystal Surface

FIGURE 2.4.2 Illustration of three ways of preventing channeling of implantation.

preventing channeling. In Figure 2.4.2 (a) for preventing channeling, one can implant through a thin layer of oxide; and in Figure 2.4.2 (b) it is shown that for preventing channeling, the crystal can be set at an angle to the direction of the incidence beam. In Figure 2.4.2 (c), the crystal is predamaged to prevent channeling. Of course as was mentioned before, it is impossible to prevent channeling completely. All that one can do is to minimize this effect.

2.5 Annealing Treatment

When ions of different energy enter the surface of a substrate and collide with the atom of the target, these collisions will cause damages to the structure of the crystal. These damages can be repaired to some extent by thermal treatment, i.e. by heating the crystal to some temperature to gain back its original crystal structure.

In the silicon substrate after implantation, there will appear a milky color in the silicon surface. After annealing it to 650 ^{o}C, the milky color seems to disappear. This suggests some type of crystal recovery after the annealing treatment. Not in all cases will the annealing treatment cause 100 per cent crystal damage recovery. In the case of a high energy implantation, the crystal damage will be so great that post annealing will not bring back the original crystal structure.

Control of the substrate temperature during implantation will also minimize the damage, and control of the temperature

of the sample during implantation places additional requirements on the design of the target chambers by requiring accurate and uniform heating or cooling environments. For some substrates like GaAs, or certain device applications, it may be desirable to maintain the substrate at an elevated temperature during the implantation in order to anneal the damage as it is created.

2.6 The Electrical Properties of Ion Implanted Regions

Since many dopants have different properties when they are implanted into a substrate, the electrical properties of the ion implanted regions are not always easy to measure. Also there are many parameters that could change the electrical properties of the ion implanted regions. Some of these parameters are ionic energy, target temperature during the implant, post annealing treatment, and predamage and postdamage of the implanted regions. Therefore, it is very important to have in mind these parameters when one is trying to further discover the electrical properties of the ion implanted regions.

For finding the complete electrical properties of ion implanted regions, it is required to find the carrier type, the sheet resistivity, the profiles in depth of the carrier concentration, and the carrier mobility. In the following, a brief discussion of these measurements is given.

(1) Carrier Type - Finding the carrier type is very simple and fast, and it only requires two probes and a voltmeter. The two probes are made of the same metal but at different temperatures. Normally the semiconductor is in thermal equilibrium; but when a small region is heated, the electrons, for example in a n-type semiconductor, will have high velocities and diffuse away from the region making it positive with respect to the area at the lower temperature. This principle can be used by connecting probes to a sensitive voltmeter. If the semiconductor is n-type, the hot probe will be positive with respect to the cold probe; and if the semiconductor is p-type, the hot probe will be negative with respect to the cold probe.

(2) Sheet Resistivity - The measurement for sheet resistivity has been accomplished using a four point probe. In order to use this technique, the substrate must be clear of any oxide, i.e. the 15 to 20 A^{O} of oxide that forms on the surface of the substrate in room temperature must be removed in order to have reproducible measurements. A four point probe measurement apparatus is shown in Figure 2.6.1 in which basically one would apply a constant current through the two outer probes and measure the voltage across the two inner probes. The resistivity can be calculated from

$$\rho = \frac{\pi}{\mathrm{Ln}2} \frac{V}{I} \cdot t$$

and

$$\rho = \frac{1}{\sigma} = \frac{1}{q\mu N}$$

where

METHODS OF MEASURING THE ELECTRICAL PROPERTIES

OF ION IMPLANTED REGIONS

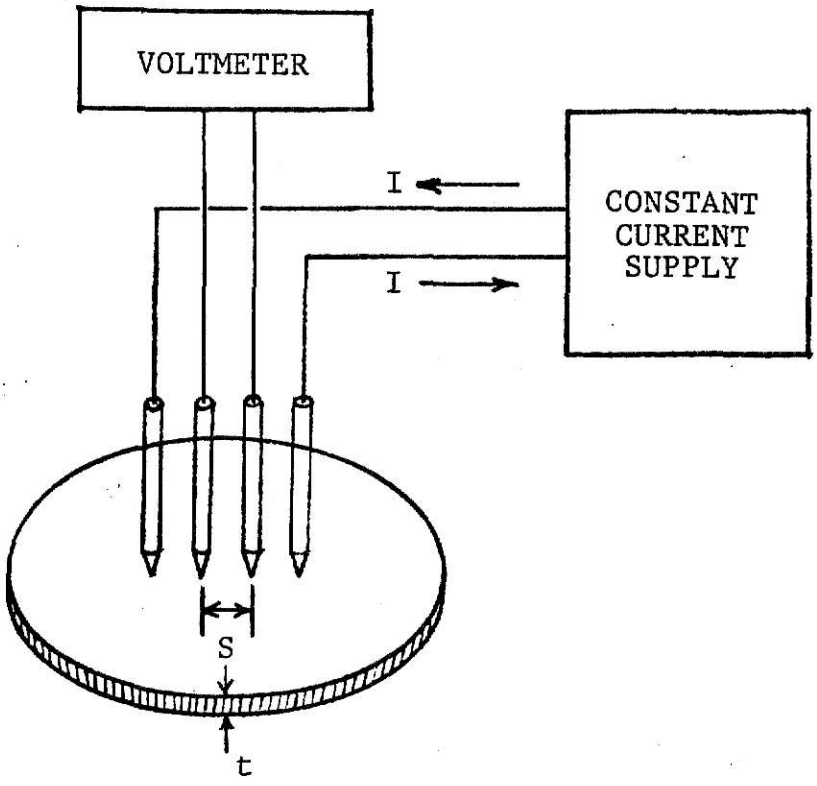


FIGURE 2.6.1 Four Point Probe Resistivity Measurements

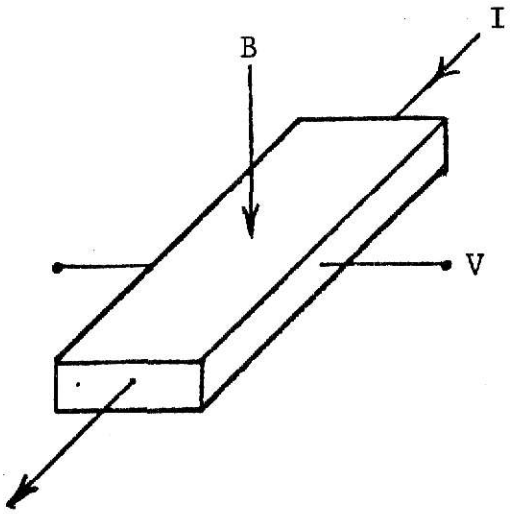


FIGURE 2.6.2 Hall Effect Measurement

ρ is resistivity

V is measured voltage

I is applied current

t is substrate thickness

σ is conductivity

q is electronic charge

μ is average mobility

N is average carrier concentration ($atoms/cm^3$)

This formula holds for the case when the spacing between the probes is greater than the thickness of the substrate, i.e. S > t. A graph of resistivity vs. impurity concentration for both n and p-types is shown in Figure 2.6.3.

(3) Carrier Concentration and Carrier Mobility - The measurement of the carrier concentration and the carrier mobility can be performed using the Hall effect measurement. The set-up for this measurement is shown in Figure 2.6.2. The basic set-up is that one applies a current through two sides of the geometrical bar and applies a magnetic field perpendicular to this current; then the voltage can be measured across the other two sides of the bar. The polarity of this voltage depends on the relative direction of the current, the magnetic field, and the type of carrier. Then the sheet resistivity is given by

$$R_s = \frac{V_R}{I} \cdot \frac{W}{L}$$

where

V_R is the measured voltage without the magnetic field applied

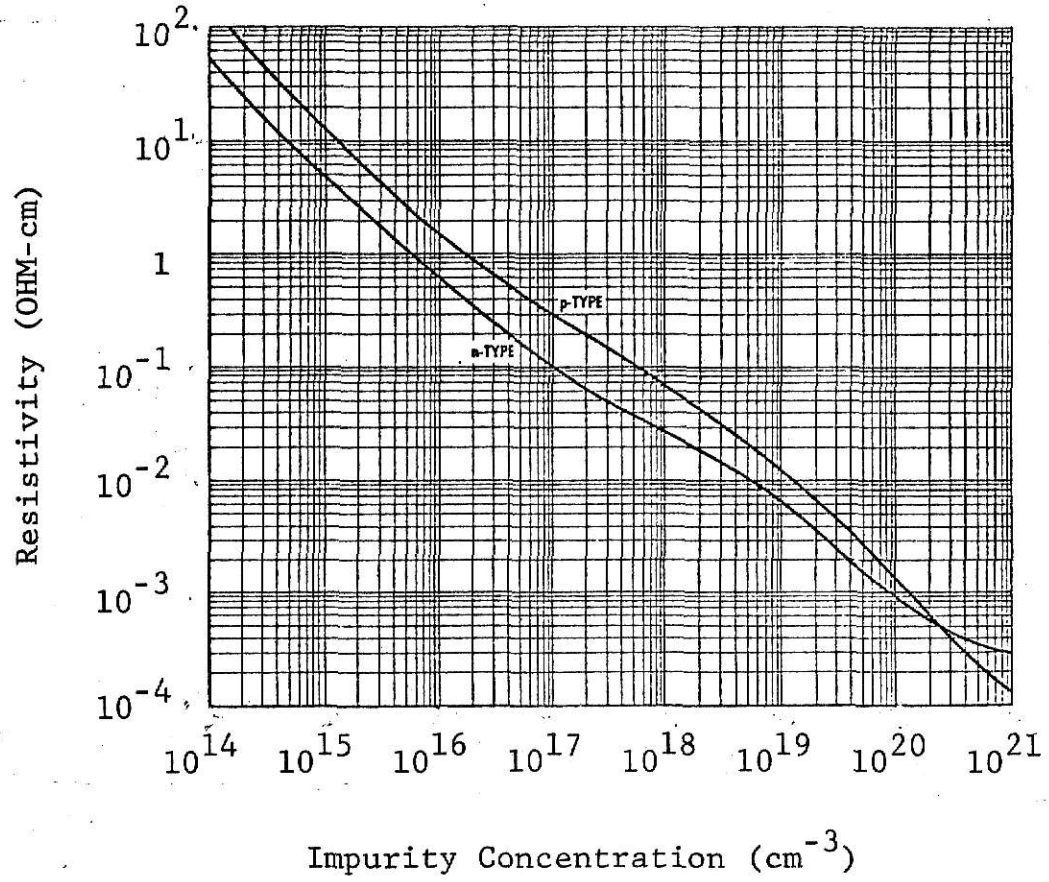


FIGURE 2.6.3 Resistivity of p-type and n-type silicon as a function of impurity doping concentration at 300 ^{o}K [from Richman (24)].

W is the width of the bar

L is the length of the bar

One can also find the surface carrier density C_s using the following equation

$$C_s = \frac{1}{R_s q \mu_d} \text{ (carrier/cm}^2\text{)}$$

where

μ_d is the drift mobility

The Hall coefficient can be calculated as

$$R_{HS} = \frac{V_H}{I} \cdot \frac{10^8}{B} \left[\frac{\text{cm}^2}{\text{coulomb}}\right]$$

where

B is the magnetic field strength (Gauss)

The four point probe and the Hall effect measurements described will allow one to find the carrier concentration and the mobility of the ion implanted region, but will not give any information on the distribution and the depth of the impurity centers responsible for the carriers.

The capacitance-voltage measurement, which is a relatively simple and fast method, can be used to find the depth profile of electrically active impurities. The following section will discuss the capacitance-voltage measurement.

Capacitance-Voltage Measurement

The capacitance-voltage (C-V) measurement is a well developed technique for finding the profile of ion implanted regions. In this measurement one must form a metal oxide semiconductor (MOS)

capacitor, which can be constructed simply by growing a thin layer of oxide (1000-2000 A^0) on the top of a substrate which this oxide forms the dielectric material of the capacitor. Then aluminum is evaporated on both sides of the substrate which forms the two plates of the capacitor. These are shown in Figure 2.6.4. When the MOS capacitor is formed, then the C-V measurement may be made by superimposing a small AC voltage upon a DC bias. A capacitance meter is used for measuring the capacitance; and for recording these data, a X-Y plotter is used to plot the C-V curve. One will learn more regarding these C-V curves in later chapters. Some advantages of the C-V measurement are as follows:

(1) It is fast and easy to make.

(2) It can be used in the middle of fabrication of an MOS device.

(3) The distribution of the electrically active centers can be found without the use of layer-removal techniques.

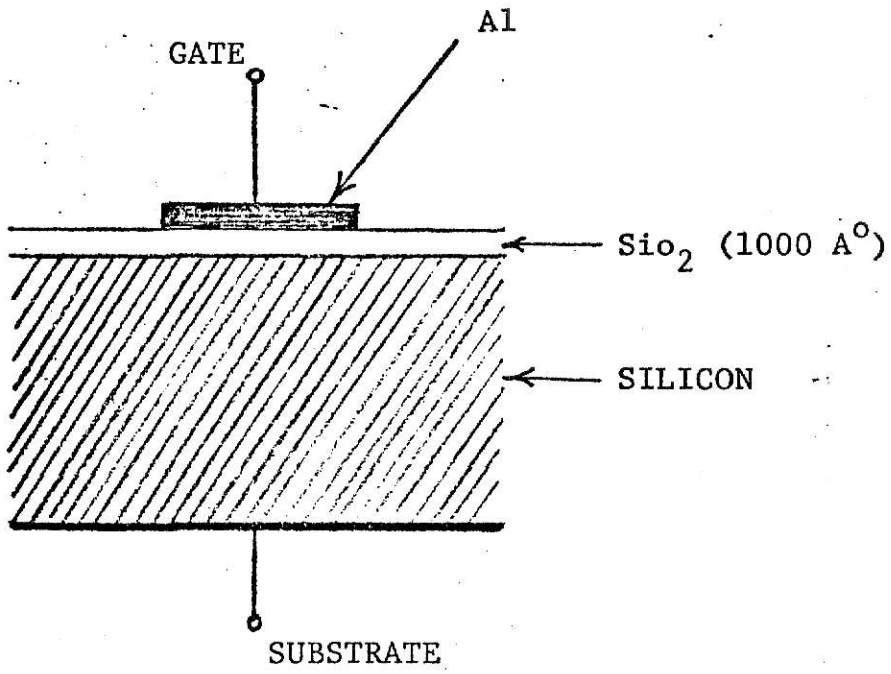


FIGURE 2.6.4 MOS Capacitor for C-V Measurement

CHAPTER III

3.1 Introduction

After discussing some important facts about ion implantation principles, it is necessary to discuss some properties of semiconductor materials which are important in the understanding of solid state electronics. These properties will be basically the atomic structure of semiconductor materials, the conduction processes in semiconductors, energy bands and the discussion of a p-n junction which is essential to any electronic device. Without understanding the physical and the electrical properties of semiconductor materials, it is impossible to fabricate any device from them. Therefore, it is important to discuss the physics that are involved in semiconductor materials.

3.2 The Atomic Structure of Semiconductors

All substances, whether they occur in a liquid, a solid, or a gaseous form, are composed of atoms. These atoms contain a nucleus around which two electrons revolve in a manner similar to that in which planets of the solar system orbit around the sun. A force of attraction, called an electric force, exists between the electrons and the nucleus and permits the electrons, which normally repel one another, to travel in orbit about the nucleus.

Contained within the nucleus are two additional subatomic particles, protons and neutrons. The atom is in its normal state when the number of protons within the nucleus is equal to the number of orbital electrons (7). The number of neutrons may or may not be equal to the number of protons. Every electron and every proton possesses a distinct electrical property known as charge. Arbitrarily, the electron is considered to possess a negative charge, and the proton is assumed to have an equal positive charge. The neutron has no charge, i.e. it is electrically neutral. Since the negative charge of each electron and positive charge of each proton are of the same magnitude but of opposite polarity, the atom, in its normal state, is electrically neutral. It is important to realize that the electrons of every atom are identical. The atoms of one element are distinguished from those of another element in terms of the number of orbital electrons and the number of protons in the nucleus. All of the elements are arranged in order of increasing mass. It is found that each element contains one more electron than its immediate predecessor on the list.

In 1925, Louis de Broglie set forth the hypotheses that all natural particles, such as electrons, possess the dual characteristics of both a particle and a wave, and that the orbits along with the electrons move must be an integral number of wavelengths (13). Therefore, the electrons of an atom can appear only at specific energy levels. Although no more than one electron can exist at any given energy level, it is customary to

group the permissible energy levels into shells and subshells. The maximum number of electrons in a particular shell is equal to $2n^2$, where n is the shell number, counting from the nucleus.

When semiconductor atoms are combined with other atoms of the same type, they share each other's four valence electrons; consequently, each atom appears to have eight valence electrons that completely fill their outermost subshell. This electron sharing is called covalent bonding, and the resulting structure is known as a crystal. See Figure 3.2.1.

3.3 Conduction in Semiconductors

One can assume a crystal having a structure like that shown in Figure 3.2.1. At a temperature of absolute zero (-273 ^{o}C), every valence electron is involved in a covalent bond and is associated with its parent atom. Since there are no free electrons, the crystal is a perfect insulator.

At room temperature (about 25 ^{o}C), however, the situation changes. Some of the valence electrons acquire sufficient additional energy, as a result of the application of heat to break their atomic bonds and wander through the crystal lattice. Since some of the atoms are then left with a deficiency of electrons, they become ions, and the crystal is said to be in an ionized state. Although here heat is the energy, an electric field or an incident light can also provide this ionizing energy. Thus, if an electric field is applied across the crystal, the free

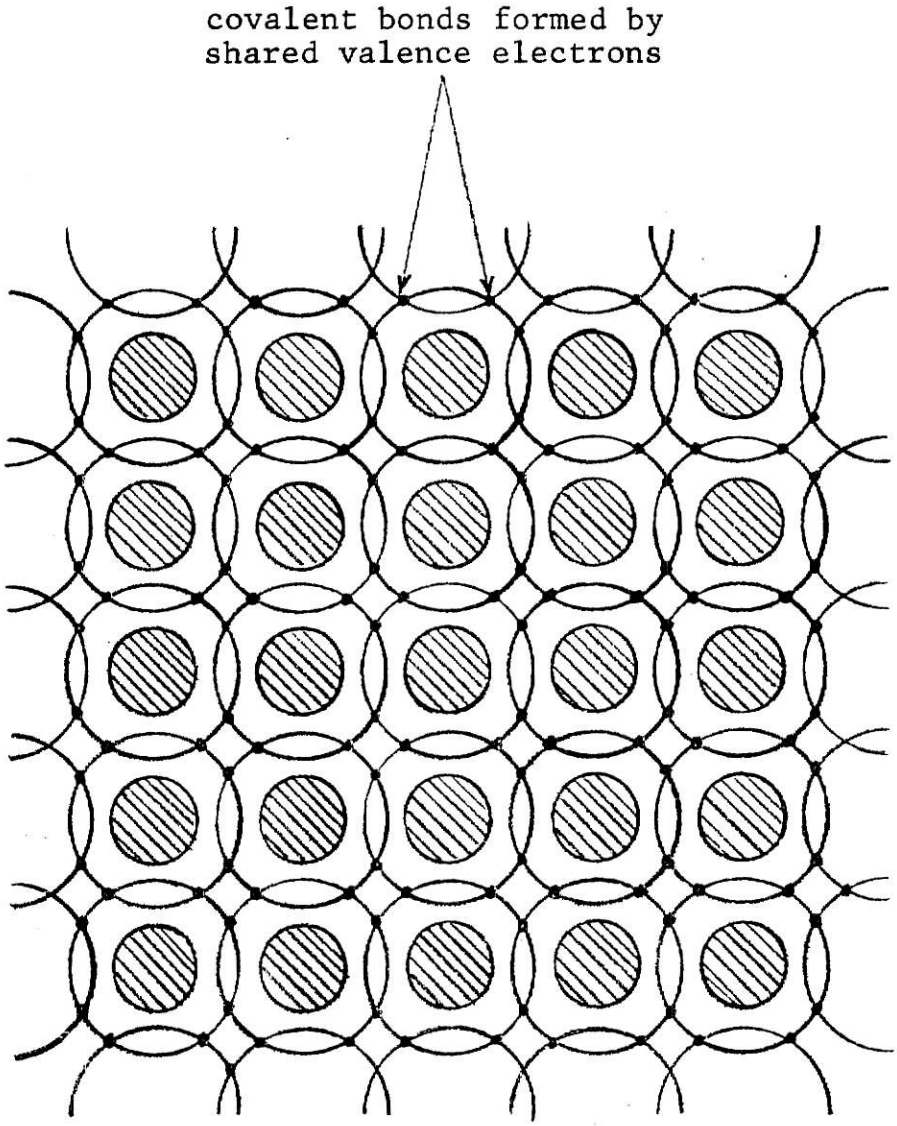


FIGURE 3.2.1 Formation of a Silicon Crystal

electrons move toward the positive terminal of the electric field source. This movement constitutes a current.

Another method of supporting a current in a semiconductor involves so called holes. When a covalent bond between two electrons is broken, a vacancy is created in the outer shell of an atom. This vacancy is called a hole. An electron from a nearby covalent bond may break its own bond and move to the previous vacancy. In doing so, the electron does not acquire the additional energy needed to become free in the usual sense, but rather retains its valence energy (14). When the electron moves from the nearby bond to the original vacancy, a new hole is created at the bond that the electron left. Another electron, in turn may leave its bond and move into this new hole, leaving yet another hole behind. In effect then, one has a current consisting of holes.

As was mentioned before, when conduction by holes takes place, the electrons concerned with the movement of the holes retain their valence energy. Since the absence of an electron from a covalent bond represents a localized positive charge (the atoms are neutral only when all valence electrons are present), the hole is thought of as a particle similar to the electron but having a positive charge. On this basis, holes are considered to be particles of a definite mass (like electrons) and to move in a direction opposite to the movement of the electrons. However, it should be noted that the concept of a hole is simply a concept used to describe the jumping movement of the electrons.

To sum up, current may be conducted by two processes in a pure semiconductor. In the first process, electrons acquire enough additional energy to break their covalent bonds and to be free to wander through the crystal lattice. These free electrons are then said to be in a conduction band. In the second process, electrons retain their valence energy and simply move from one atom to the other; that is, they remain in a valence band. This constitutes a movement of the holes.

3.4 Band Theory

One of the important key concepts for the understanding of solid state and the semiconductor phenomena is known as energy bands, which will allow one to correctly predict the behavior of solids under different circumstances. For example, the band theory permits one to classify solids as conductors, semiconductors and insulators and to study the conduction process in solids in some detail. The band theory is essential in understanding many light sensitive as well as light emission-absorption phenomena in solids and is important in explaining the different species of charge carriers in solids.

A basic band energy diagram for insulators, conductors and semiconductors is shown in Figure 3.4.1. In the case of insulators (Figure 3.4.1 [a]), there is a wide band gap energy E_g. The valence band here is the highest completely full band at absolute zero degree. In this case and also in the narrow band

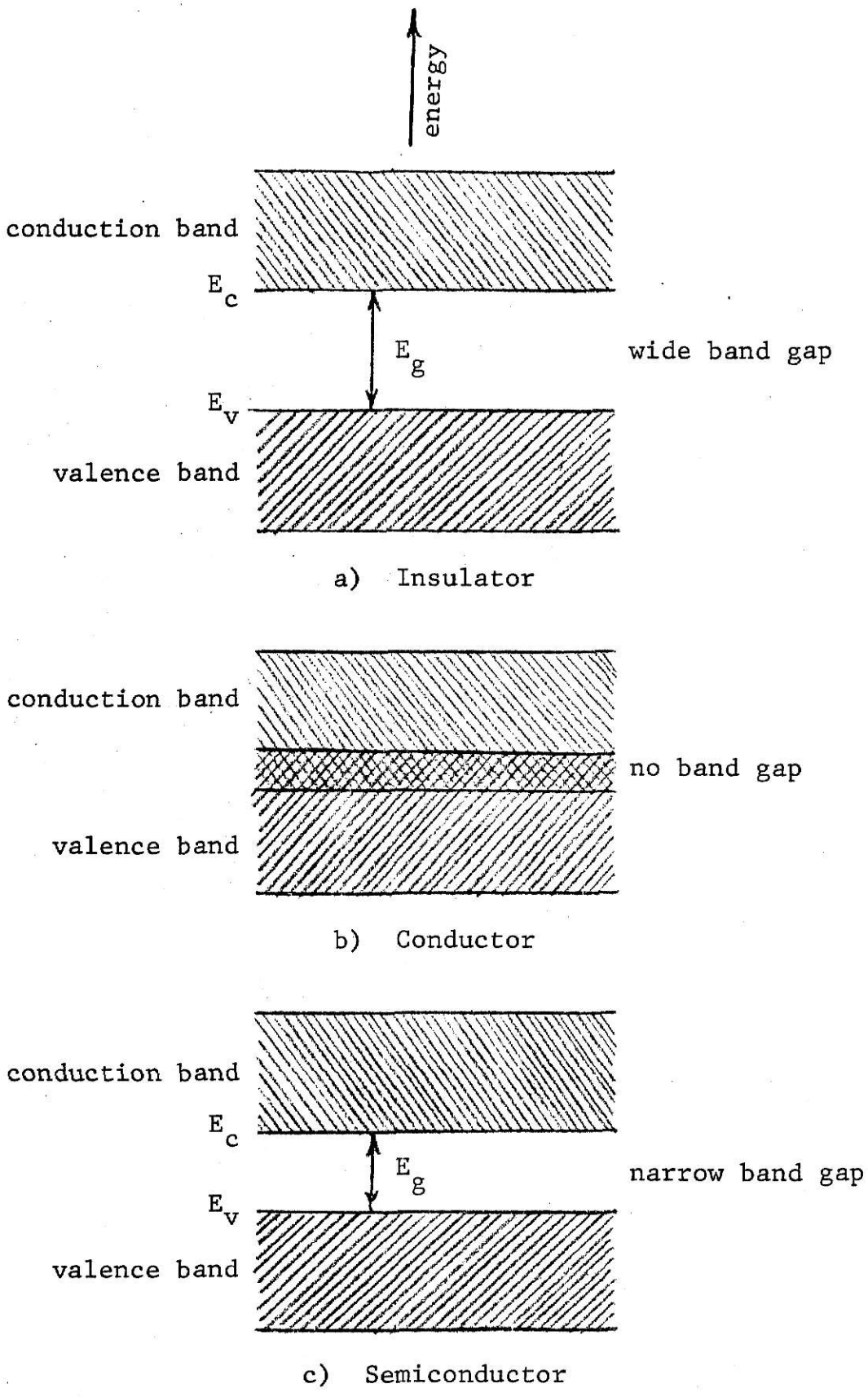


FIGURE 3.4.1 One-Dimensional Energy Band Diagram

gap solids (semiconductors), such a band arises from the electronic states corresponding to the valence electrons of the host atoms. The conduction band, which is the next higher band to the valence band, is completely empty at absolute zero degree temperature.

One can observe that neither a completely empty nor a completely full band can lead to electrical conduction. It is easy to understand how an empty band cannot contribute because there are no charged particles to contribute to the current flow. A completely full band also cannot lead to conduction because of the Pauli Exclusion principle (15).

Figure 3.4.1 (b) shows an energy band diagram of a solid with overlapping bands which are only partially full. Hence in such a solid, the electrons find plenty of available electronic states close to their energy. So it is quite easy for an electron to go from an occupied state to a nearly unoccupied state without violating the Pauli Exclusion principle. One expects then that such a solid will easily conduct electricity. Such a solid is a conductor.

Figure 3.4.1 (c) shows the energy band diagram of a solid which has a narrow band gap. Such a solid turns out to be a semiconductor. Here too, all bands up to and including the valence band are completely full at an absolute zero degree temperature. All bands including and above the conduction band are empty at absolute zero temperature. Thus for exactly the same reason as the insulator, it is expected that semiconductors

will not conduct at all at absolute zero temperature. As the temperature is raised above absolute zero, electrons will leave the valence band and go into the conduction band.

3.5 P-N Junction

Conduction in semiconductors can take place by movements of either electrons or holes. If the carrier type is changed abruptly by some means, the resulting structure is known as a p-n junction. A p-n junction may be formed from a single crystal intrinsic semiconductor by doping part of it with acceptor impurities and the remainder with donors. The precise distance over which the change from a p to an n type semiconductor occurs varies with the fabrication technique (16).

Since a p-type crystal has a high density of excess holes, and an n-type material has a high density of excess electrons, there is a diffuse flow of holes from the p-type to the n-region where they are known as minority carriers. There is a similar flow of electrons from the n-type to the p-region. This flow is only temporary, and after some time the carriers recombine. As the exchange of holes and electrons begins, the holes departing from the p-region leave behind them negatively charged immobile acceptor atoms. Similarly, electrons departing from the n-region leave behind them positively charged immobile donor atoms. This results in a negative space charge in the p-region and a positive space charge in the n-region with a field between the two regions. The magnitude of this space charge or depletion

regions are such that the net negative and positive charges are equal, and the crystal is electrically neutral. Thus, a p-n junction has a built-in electric field and a corresponding built-in potential across it (15).

Depending on polarity, an external voltage, when applied to a p-n junction, acts either to reduce or to increase the built-in potential. If the polarity of the applied voltage is such that the built-in potential is reduced, the junction is said to be forward biased. Under this condition, a junction would allow a substantial amount of current to pass through it. When the polarity of the applied voltage is such that the built-in potential is increased, the junction is said to be reverse-biased. Practically no current passes under this condition.

It is important to point out that if an alternating voltage were impressed across a p-n junction, the junction would be alternately forward and reverse biased. This means that current would flow through the crystal and externally every half cycle. This process of converting alternating current to an unidirectional current is called rectification.

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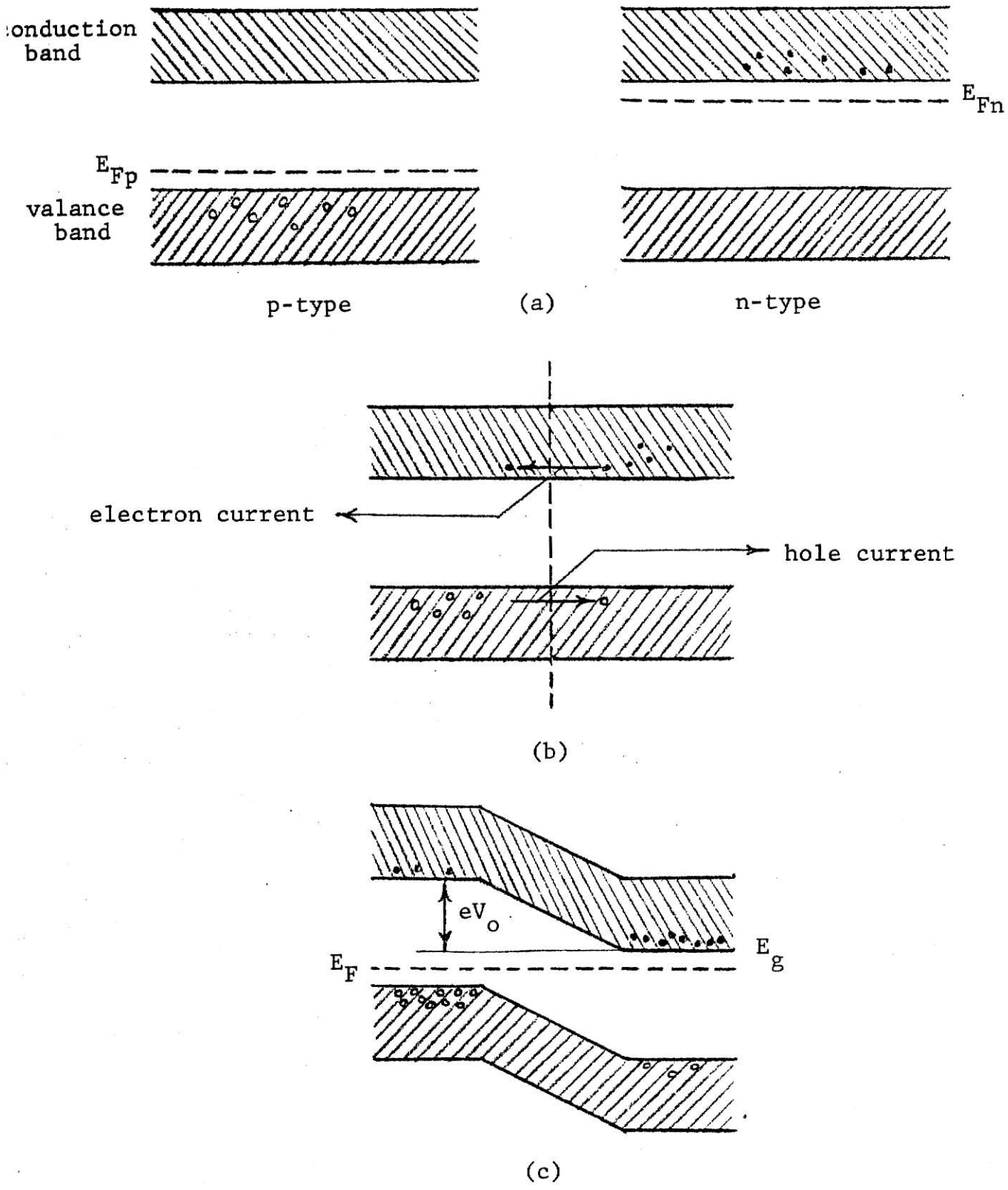


FIGURE 3.5.1 Hypothetical contact between p-type and n-type semiconductors with their band diagram (a) before contact, (b) just after contact, and (c) in equilibrium.

CHAPTER IV

4.1 Introduction

After introducing in Chapters I and II the principles that are involved in an ion implantation system and some brief discussions about the properties of semiconductors, one is able to combine these principles with device fabrication principles to construct some practical devices. The measurement of these devices can be used to actually evaluate properties of the ion implanted region.

Part of this chapter also will cover the scanning electron microscope study of ion implanted regions, and the results of some of the different measurement will be given. Also the steps that are involved in the fabrication of the Insulated Gate Field Effect Transistor (IGFET) will be mentioned, and the pictures of actual fabricated transistors will be presented.

4.2 Device Fabrication

Dramatic and rapid changes have occurred in semiconductor device fabrication in a relatively short time. These changes have helped the field to grow; and consequently, many different devices have been fabricated using different methods of fabrication. Device manufacturers in the last few years have paid a lot of attention to the fabrication of new devices using ion

implantation which is an alternative way to dope semiconductors. With the help of ion implantation, it has been found possible to produce on a single homogeneous chip of silicon crystal, resistances, capacitors, p-n junctions, bipolar and monopolar MOSFET transistors, as well as means of interconnecting the various regions of the silicon chip. The technology also provides the means with which to protect the surface of the device with a protective layer of insulating oxide which helps to stablize the semiconductor device characteristics as well as materially reduce leakage currents.

The procedure that was adopted for this study was to do the following:

1. Clean the silicon substrates. The cleaning procedure is given in Appendix A.

2. Ion implant some area of the silicon substrates using the Cockroft Walton accelerator which was available.

3. For a preliminary measurement, use a four point probe to measure the resistivity of the non-implanted regions and the implanted regions before and after annealing, and then compare them together.

4. Grow a thin layer of oxide (1000 A^{o}) using steam oxidation. See Appendix B.

5. While keeping the silicon substrate clean, apply the photoresist technique to open the windows in the oxide layer. See Appendix C for more detail about the photoresist processes.

6. Evaporate aluminum in the vacuum system (1 X 10^{-5} TORR) on the top of the silicon wafer.

7. Apply photoresist again; and using the metalization mask, etch some areas of the aluminum.

8. Perform capacitance-voltage measurements on the non-implanted and the implanted regions.

Tables II and VI will summarize some of the important parameters on the different samples. In these tables the samples are identified, and the main purpose of these tables are to give the readers an overall view of the sample parameters and in what condition they were implanted. On samples 2A, 3A and 5A, a thick layer of oxide was grown to be used at a later time; but they were not used, and no implantation was performed on them. Also on samples 9A and 10A, no implantation was performed.

4.3 Damage Study

As was mentioned in Chapter II, damage study can be conducted using a scanning electron microscope. There are few other methods that could be used to find more about damage creation. It is beyond this work to do any extensive damage study. The equipment that was used here is a scanning electron microscope available in the Entomology Department at Kansas State University. At first after the samples were implanted, they were taken to the Entomology Department and were studied under the electron microscope. At high magnification, the surface damage was not seen at first on some of the samples. The reason for this was that no coating of any type was evaporated on the surface, and the surface was not conducting properly. After a thin coat of Pd-Au was

TABLE II. Summary of sample parameters. Nitrogen implanted on n-type silicon.

Sample # *(n-type)	Energy (KV)	Beam Current (μA)	Implanted Time (Minutes)	Ion Dose (ions/cm^2)	Impurity Concentration (atoms/cm^3)	Maximum Anneal Temp. (^{o}C)
1A	70	1.5	5	$2.81X10^{15}$	$1.5X10^{15}$-$2X10^{15}$	650
2A	3500 A^o of oxide was grown on it (no implantation)					
3A	3500 A^o of oxide was grown on it (no implantation)					
4A	67	1.9	2	$1.43X10^{15}$	$1.5X10^{15}$-$2X10^{15}$	700
5A	4500 A^o of oxide was grown on it (no implantation)					
6A	71	3.4	2.5	$3.18X10^{15}$	$1.5X10^{15}$-$2X10^{15}$	700
7A	70	2.4	6.75	$6.08X10^{15}$	$1.5X10^{15}$-$2X10^{15}$	600
8A	70	3	10	$1.13X10^{15}$	$1.5X10^{15}$-$2X10^{15}$	700
9A	no implantation					
10A	no implantation					

*n-type silicon wafers of 2.8-3.5 OHM-cm resistivity, thickness of .033 cm and with <111> orientation.

All implantation was done in room temperature.

Annealing the silicon wafers was performed using a furnace for 10 minutes.

TABLE III. Summary of sample parameters. Nitrogen implanted on p-type silicon.

*Sample # (p-type)	Energy (KV)	Beam Current (μA)	Implanted Time (Minutes)	Ion Dose (ions/cm^2)	Impurity Concentration (atoms/cm^3)	Maximum Anneal Temp. (^{o}C)
1B	80	11	4	$1.65X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	700
2B	80	12	5	$2.25X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	750
3B	80	10.5	10	$3.94X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	700
4B	70	15	10	$5.63X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	800
5B	80	19	10	$7.13X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	800
6B	80	18	10	$6.75X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	800
7B	85	17	10	$6.38X10^{16}$	$2.5X10^{14}$-$3.5X10^{14}$	850

*p-type silicon wafers of 40-70 OHM-cm resistivity, thickness of .025 cm and with <111> orientation.

All implantation was done in room temperature.

Annealing the silicon wafers was performed using a furnace in a nitrogen atmosphere for 10 minutes.

evaporated on the samples under investigation, the surface damages were more visible and easier to identify. Although in some samples, it was still difficult to identify the damaged area under high magnification. The magnification varied from 500 to 50,000 and in some samples at the highest magnification, there was not any kind of surface damages that could be observed.

Some of these surface damages were due to a high dosage of ions which were in ranges of $1X10^{15}$-$7X10^{16}$ ions/cm^2. In Figures 4.3.1 and 4.3.2, some of these surface damages are shown which are due to high dosages of ions.

For this work there was no attempt to study the damaged area inside the crystal with the exception of one sample which was broken in half at the implantation area. The purpose of this was to be able to look at the edges of the substrate where they were implanted and be able to observe any modification from the edges where they were implanted. In Figure 4.3.3 and Figure 4.3.4, the scanning electron microscope picture of these edges are shown at two different magnifications. In Figure 4.3.3 and 4.3.4, it should be noted that at the edge of the substrate the implanted layer is visible which is identified by a darker color. Of course a small crack is also visible on the edge of the substrate, which could have been caused by the breaking of the substrate.

The precise mechanism for creation of these damages is not understood yet; but it is obvious that the more dose of ion that is used, the more damages that are created. One thing that is also clear is the temperature of the substrate during

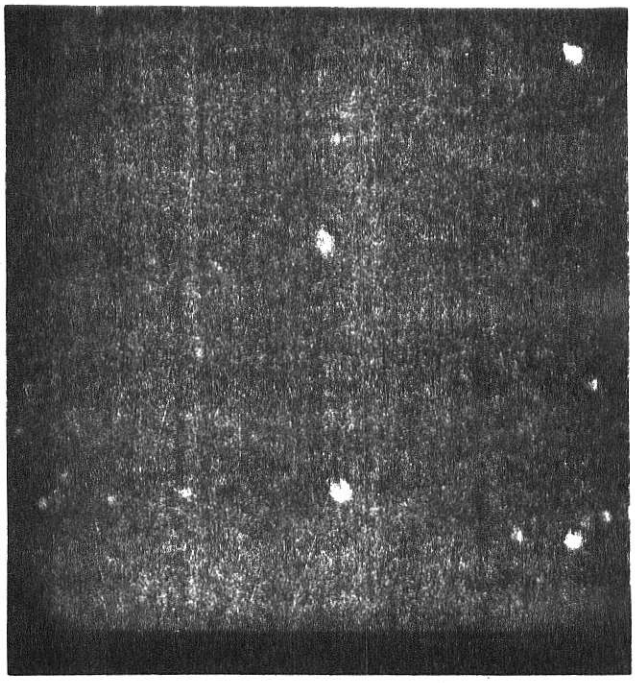


FIGURE 4.3.1. Scanning electron microscope picture for Sample #5B of the implanted region.

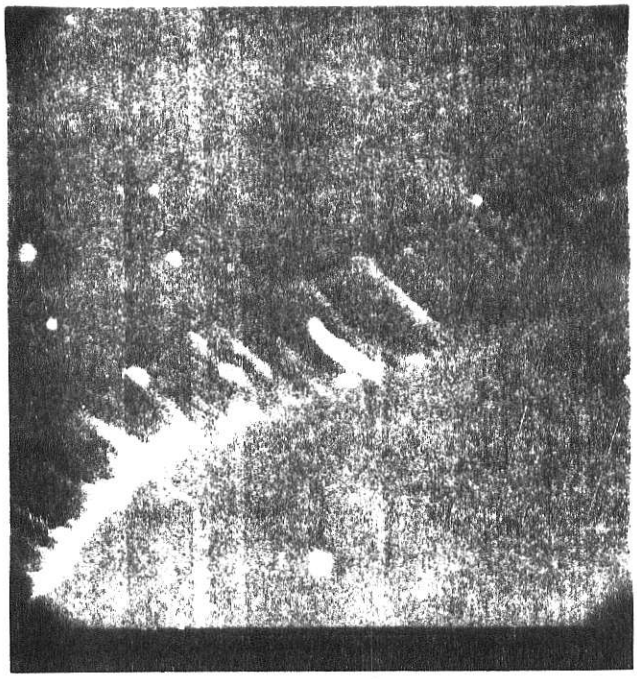


FIGURE 4.3.2. Scanning electron microscope picture of implanted regions with some kind of surface irregularity (Sample #7B).

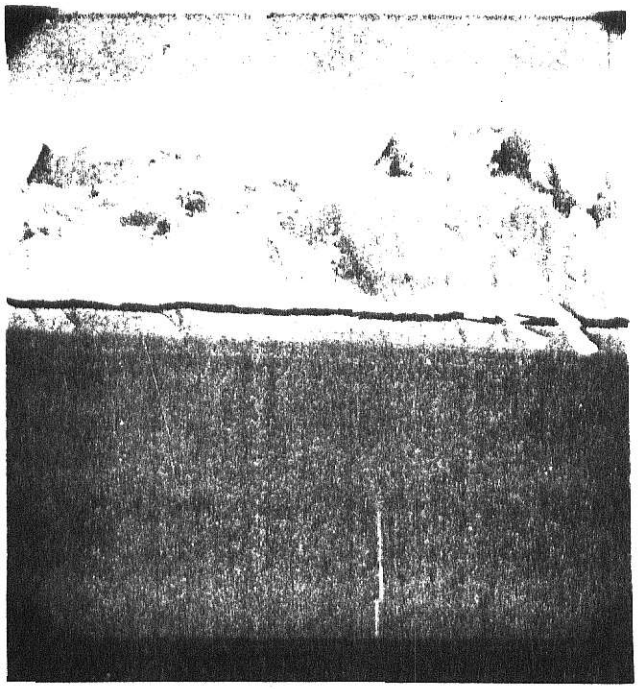


FIGURE 4.3.3. Scanning electron microscope picture of implanted region looking at the edge of the substrate at lower magnification (Sample #7B).

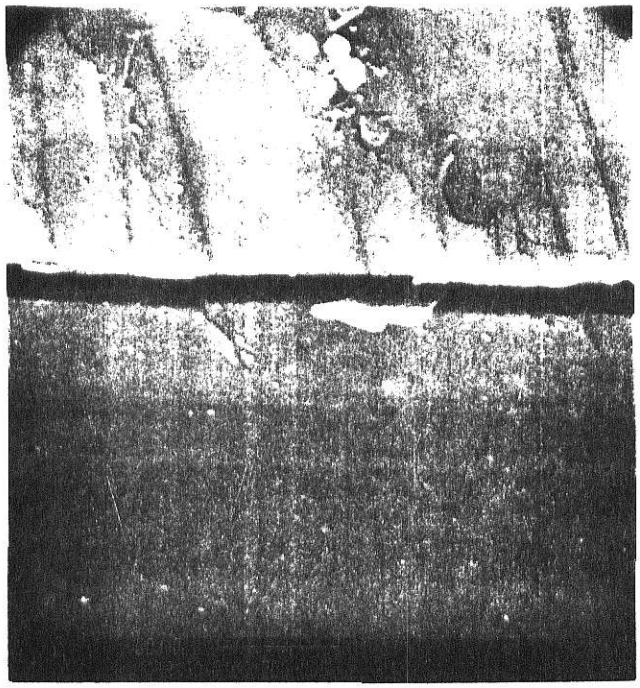


FIGURE 4.3.4. Scanning electron microscope picture of implanted region looking at the edge of the substrate at high magnification (Sample #7B).

implantation. Depending upon the type of crystal and its orientation, the temperature will influence the amount of damages that are created. An important point also should be kept in mind as to the mass and the size of the atoms that are implanted into the crystals. If the size of the implanted ions is large, there will be a highly disordered zone. And in the case of light ions, the damage is more spread out.

4.4 Fabrication of the Insulated Gate Field Effect Transistor

Since the gate structures for most Insulated Gate Field Effect Transistors (IGFET) are of the MOS type, this device has also been called Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The principle of this device was first demonstrated in the early 1930's by Lilienfeld (18) and Heil (19). In the late 1940's, it was again closely studied by Shockley and Pearson (20); and in the early 1960's, the first IGFET was fabricated using a thermally oxide silicon structure.

The basic structure of an IGFET is shown in Figure 4.4.1 (a). This device consists of a p-type semiconductor into which two n-type regions, the source and the drain, are formed. The metal contacts are formed on the source, drain and on the top of the oxide gate. When no voltage is applied to the gate, two p-n junctions are formed back-to-back from the drain to the source. When a large positive bias is applied to the gate, such that a surface inversion layer (or channel) is formed between the two

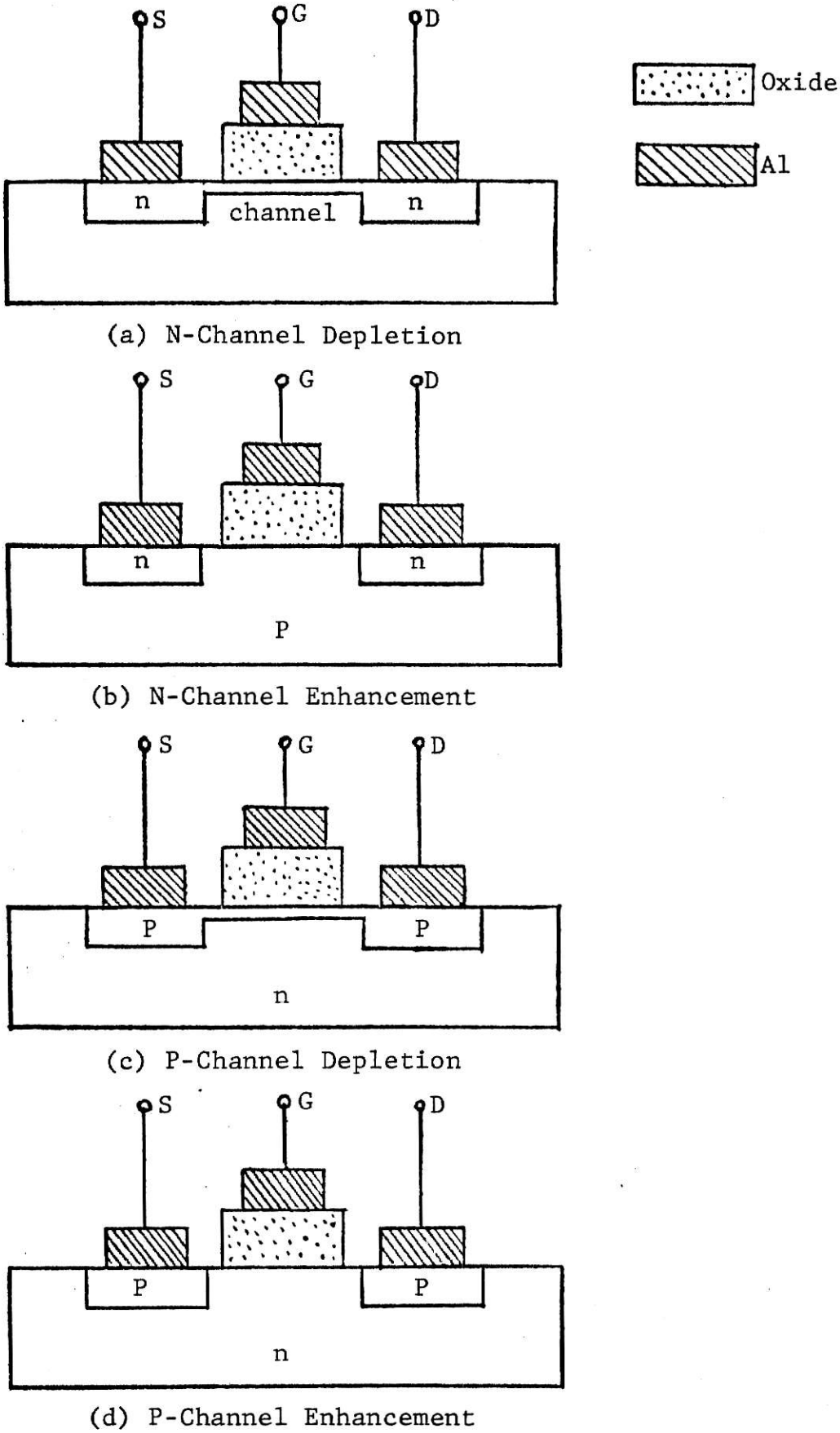
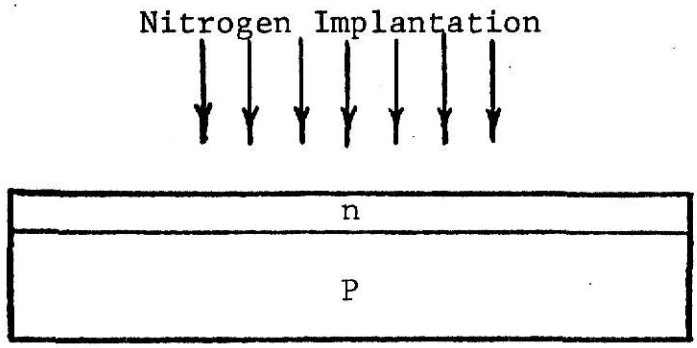
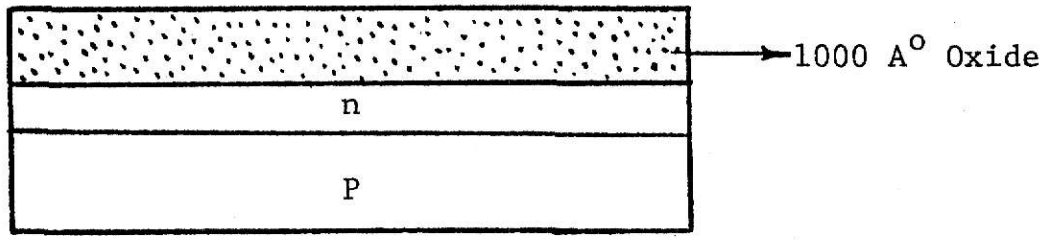


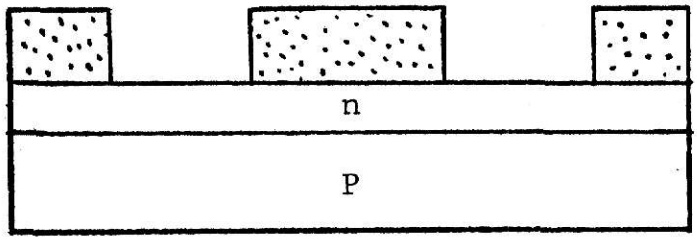
FIGURE 4.4.1 Basic types of insulated gate field effect transistor (IGFET).



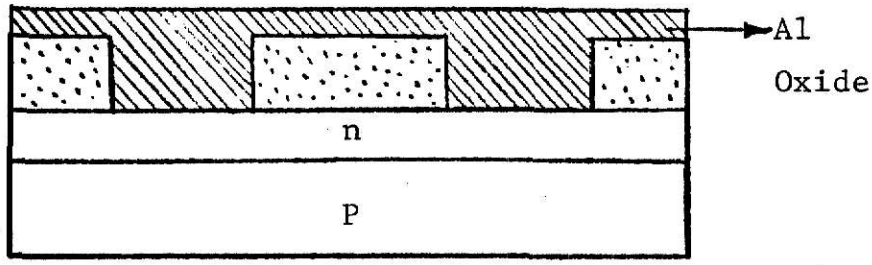
(a) Implant Nitrogen in Silicon



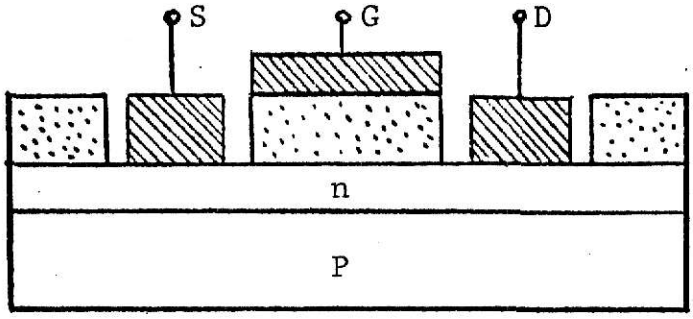
(b) Oxide Was Grown



(c) Windows Were Etched in Oxide



(d) Evaporate Al on Surface



(e) Al Was Etched

FIGURE 4.4.2. Fabrication of IGFET

n-regions, the source and the drain are thus connected by a conducting surface n-channel through which a large current can flow.

There are basically four different types of IGFET depending on the types of inversion layers. These four types are shown in Figure 4.4.1. If an n-channel exists at a zero gate bias, Figure 4.4.1 (a), one should apply a negative bias on the gate to deplete the carriers in the channel and thus reduce the channel conductance. On the other hand, if the channel conductance is very low at a zero bias, Figure 4.4.1 (b), one should apply a positive voltage on the gate in order to enhance the channel conductance. This second type is called the n-channel enhancement IGFET. Similarly, there are the p-channel depletion and the enhancement IGFET as shown in Figures 4.4.1 (c) and (d).

In the fabrication of IGFET, the most important variable parameter is the gate oxide, which influences the characteristics of the device. For fabrication of IGFET, it was decided to follow the earlier work completed for a master's thesis by William Dawes (21) on the fabrication of the IGFET. In his thesis, he fabricated IGFET using a conventional diffusion method. All of the necessary masks were furnished by Mr. Dawes for the fabrication of the IGFET using ion implantation. The following steps were followed for fabrication of the samples:

1. After the implantation of the samples at room temperature with nitrogen, they were annealed in a nitrogen atmosphere. A nitrogen atmosphere was used to prevent any kind of surface oxidation while the samples were annealing.

2. A thin layer of oxide (about 1000 A^{o}) was grown on the substrate using steam oxidation. See Appendix B.

3. Photoresist was applied to the surface; and using mask #02, windows were opened on the oxide. See Appendix C.

4. The substrate was kept clean, and aluminum was evaporated on the surface in the vacuum of 10^{-5} TORR. If good Al deposition is made, the surface looks shiny.

5. Photoresist was applied to the surface again. Using mask #03, the aluminum was etched.

6. The substrate was heated to 550 ^{o}C for 5 minutes to insure a good ohmic contact between the silicon and the aluminum.

In the fabrication of the IGFET, a photolense camera was used to take a photograph of the different parts of the fabrication. Figure 4.4.3 shows the substrate with oxide grown on it. Photoresist on that picture is shown where the windows are to be opened in the oxide; and in Figure 4.4.4, the oxide is etched in hydrofloric acid. After the oxide is etched, the photoresist is removed and a thin layer of aluminum is evaporated on the surface in a vacuum atmosphere. Then the photoresist is applied again, and the metalization mask is used to etch parts of the aluminum. In Figure 4.4.5 the photograph shows photoresist in places that are to be metalized, and in Figure 4.4.6 the completed fabricated IGFET is shown.

After the fabrication of the IGFET, the device was ready to be analyzed. For making contact with the three terminal devices, three small needles were furnished, and under a microscope the contact was made. The transistors were analyzed using

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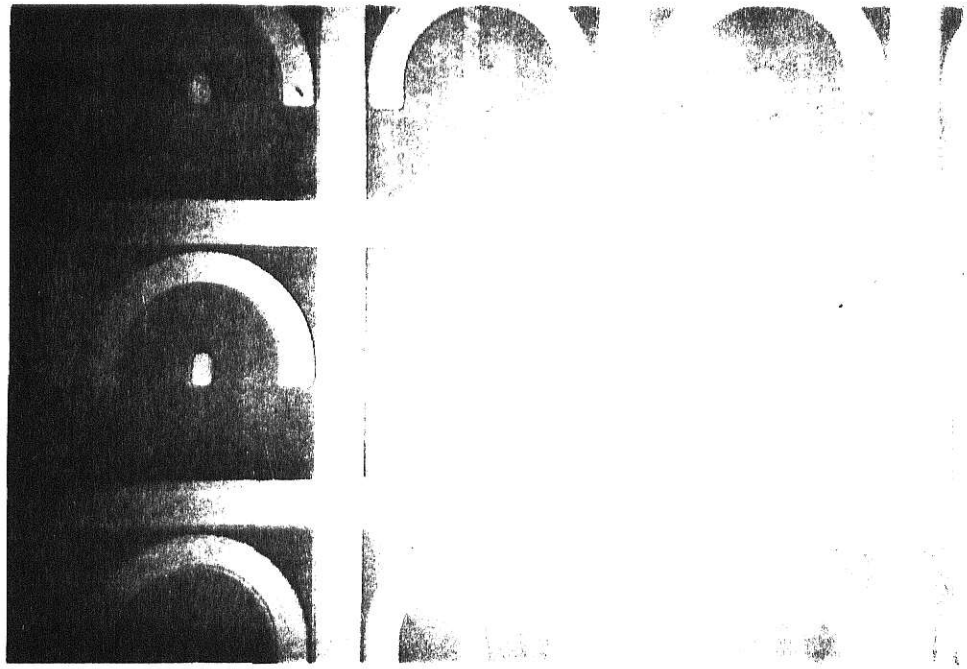


FIGURE 4.4.3. Photoresist is used to etch windows in the oxide.

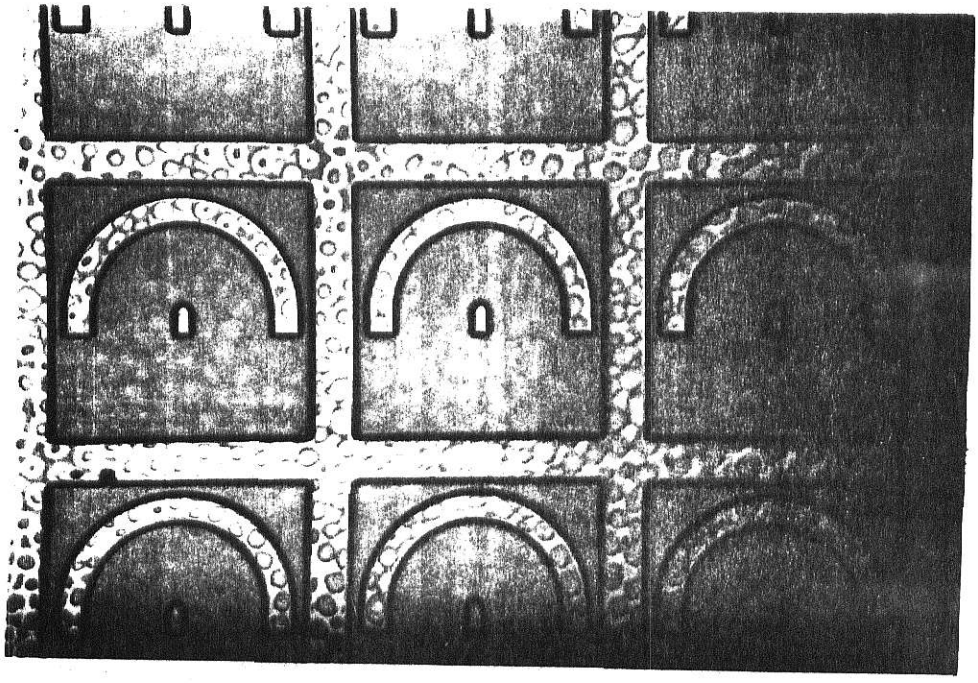


FIGURE 4.4.4. Etched windows are shown here.

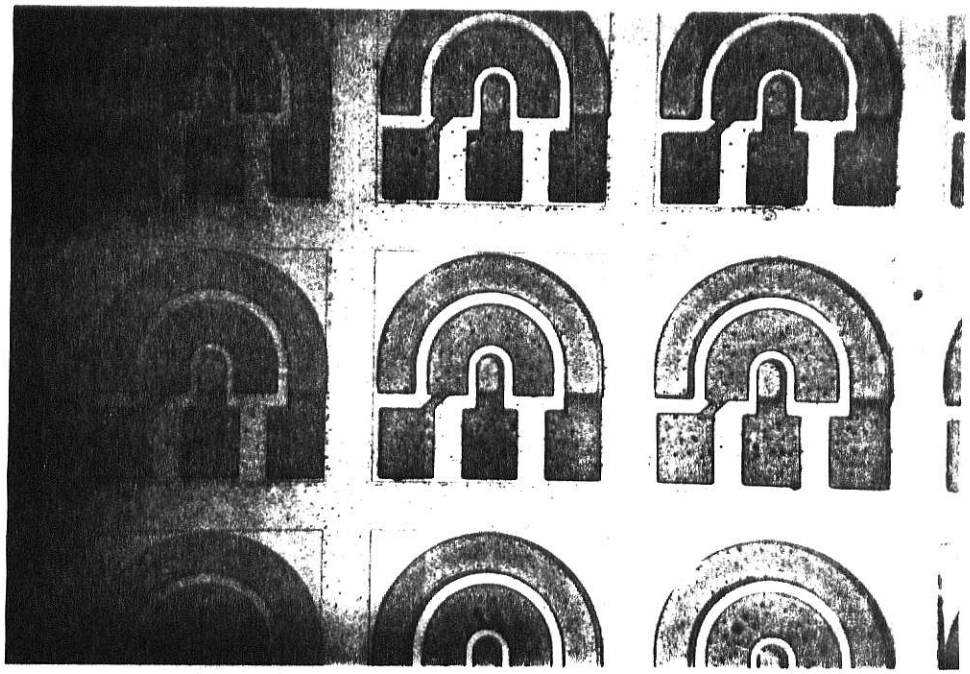


FIGURE 4.4.5. Photoresist covers the parts that are to be metalized.

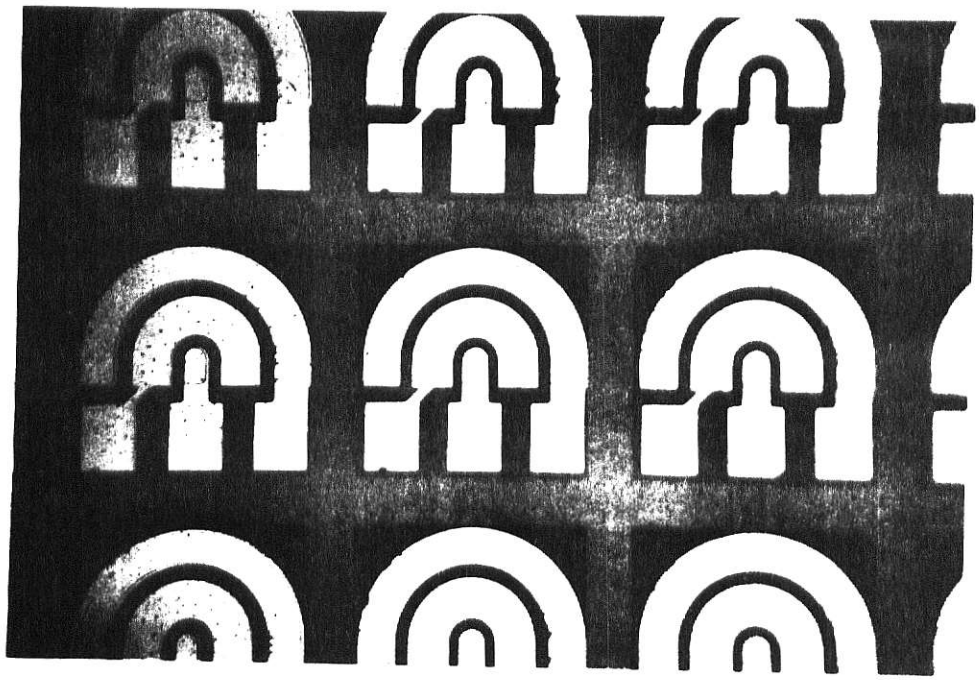


FIGURE 4.4.6. Aluminum covers three terminals of the transistors.

a curve tracer; however, this was not successful on any of the transistors. The measurement did not show any sign of a working transistor. A few things were suspected for the reason of not having working transistors. One reason was that contamination was probable, and the other reason that could have caused the failure of the transistors is that heavy implantation was used all over the silicon substrate.

One of the fabricated transistor parts was carefully examined at a high magnification under a scanning electron microscope (SEM). Figure 4.4.7 shows the SEM photograph of this transistor in which contamination again was likely to have caused the failure.

Analyzing the substrates did not end here; the gate and the gate oxide structure were used to perform the capacitance-voltage measurement. The capacitor was formed with two plates in which one plate was the gate metal and the other plate was the back of the substrate. The capacitance-voltage measurement was discussed briefly in Chapter II. Therefore, it should be noted here in a little more detail.

As was mentioned before, the capacitance-voltage measurement is easy to determine, and it can be performed in between the fabrication of a device. The basic capacitance-voltage measurement set-up is shown in Figure 4.4.8, where a small AC voltage is superimposed upon a DC bias. A small probe with a coaxial cable is used to make contact with the top plate and another connection with the bottom of the substrate which is

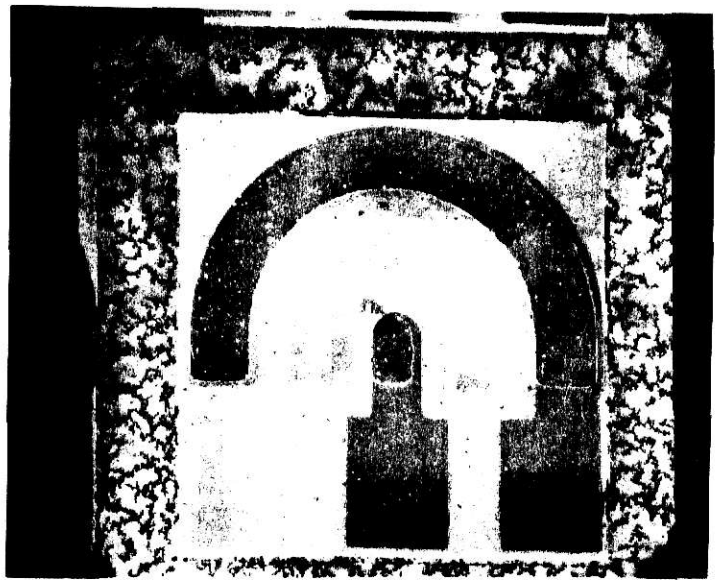


FIGURE 4.4.7. Photograph of one transistor enlarged X150 using the scanning electron microscope.

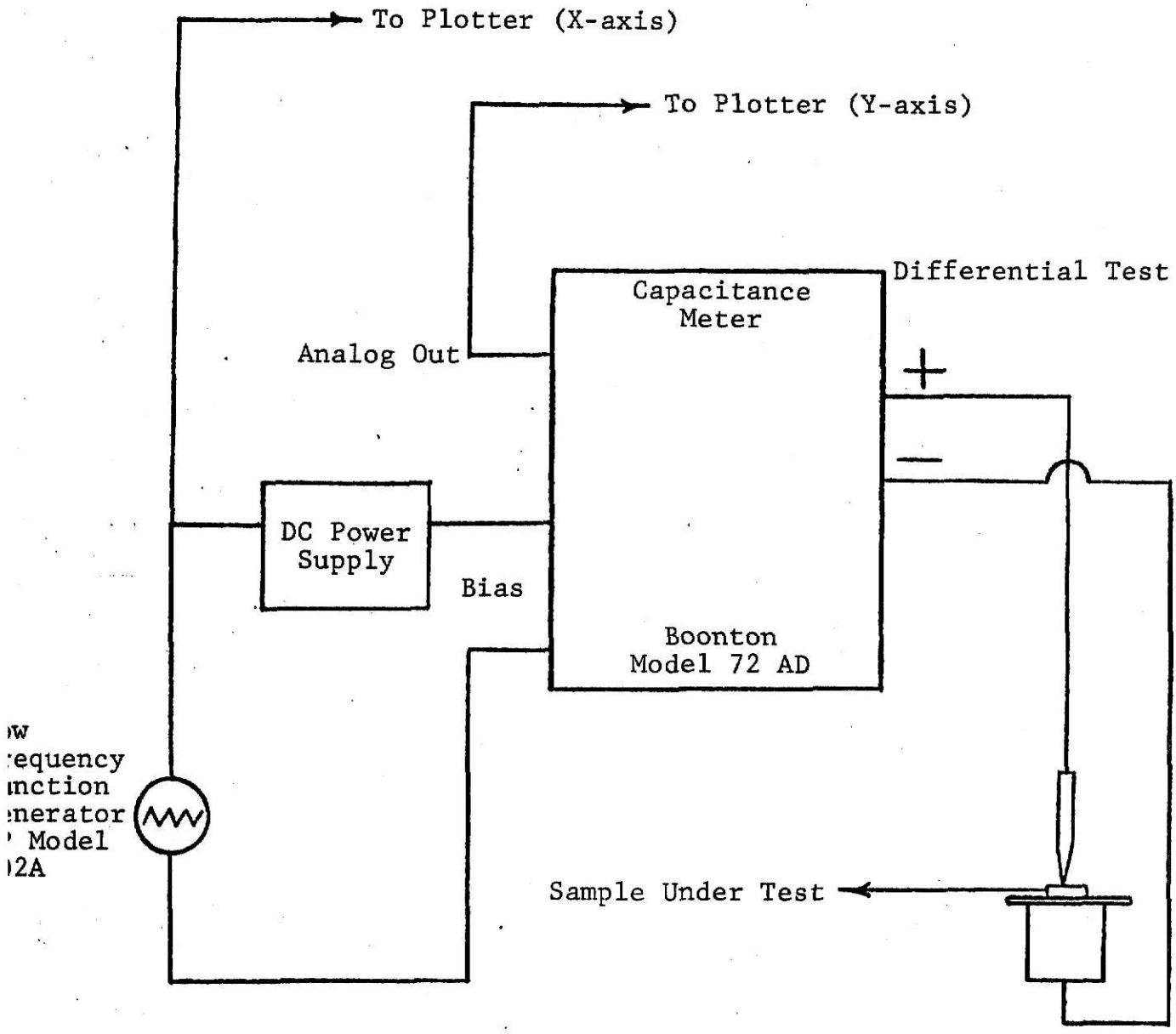


FIGURE 4.4.8. Diagram of the apparatus used to obtain the C-V measurement.

metalized with aluminum. A capacitance meter is used for measuring the capacitance; and for recording the data, an X-Y plotter is used.

The results of these capacitance-voltage measurements and the C-V curves will be given in the next section. It should be stated here that the small applied AC voltage had a triangular waveform of a low frequency (f = .1 HZ) which was produced by a low frequency function generator (HP Model 202A). Also faster frequency waveforms were applied for C-V measurement, but there was no results obtained from them.

4.5 Experimental Results

Resistivity Measurements

Resistivity measurements were performed on different samples using a four point probe. This method was described in Chapter II. The measurement device has four probes in which all are set in one line. A current is applied to the two outer probes, and the voltage is measured across from the two inner probes. The resistivity is calculated using the formula,

$$\rho = \frac{\pi}{\ln 2} \frac{V}{I} \cdot t$$

where

ρ is the resistivity

V is the measured voltage

I is the applied current

t is the wafer thickness

This formula holds for the case where the spacing between the probes are much larger than the thickness of the substrate.

The measurement that was performed here on the different samples was not too accurate because of poor contact with the substrate surface. One of the requirements for making a good ohmic contact was to have a good clean surface. The substrate surface should be free of any kind of oxide, and the 10-30 A^{o} of oxide which forms on the surface in room temperature must be removed. The measurements were performed on the ion implanted regions before and after annealing. Again, it was not clear that the measurements were accurate.

A summary of the resistivity measurement is given in Table IV, and it should be noted that measurements were made on the samples after annealing of the samples at different temperatures. The annealing was performed in a nitrogen atmosphere to prevent surface oxidation.

Capacitance-Voltage Measurement

For each of the samples, both n-type and p-type silicon, capacitors were formed on the surface using the oxide as a dielectric of the capacitor and the two plates. One plate was formed by evaporating aluminum on the surface, and the other was the bottom of the substrate. Using the gate and the gate oxide as capacitors, the capacitance-voltage measurement was performed on the completed Insulated Gate Field Effect Transistors.

TABLE IV. Summary of resistivity measurements on implanted regions as a function of anneal temperature.

	Sample #	Measured Voltage (V)	Applied Current (A)	Resistivity (Ω-cm)
Before Anneal	4B	.08	0	∞
	5B	.15	0	∞
	6B	.08	0	∞
500 °C Anneal	4B	5m	28μμ	$22.3X10^6$
	5B	13m	.16n	$10.2X10^6$
	6B	.4m	5μμ	$10.1X10^6$
600 °C Anneal	4B	.8m	4.6μμ	$21.8X10^6$
	5B	2.5m	80μμ	$3.9X10^6$
	6B	4m	6μμ	$81X10^6$
700 °C Anneal	4B	4.2m	42μμ	$12.6X10^6$
	6B	10m	.19n	$6.6X10^6$
	7B	6m	64μμ	$11.7X10^6$
750 °C Anneal	4B	2.9m	.11m	333.4
	5B	18m	.01m	227.8
	6B	3m	.2m	189.8
800 °C Anneal	4B	22m	.02m	1.22
	5B	18m	.01m	3.33
	6B	4m	.02m	2.53

TABLE V. Impurity concentration for a few selected samples obtained from the C-V curves.

	Sample #	Minimum Capacitance (PF)	Maximum Capacitance (PF)	$\frac{C_{min}}{C_{max}}$	Impurity Concentration (atoms/cm^3)
Non-Implanted Regions	1B	2.7	6.9	.42	$5X10^{15}$
	4B	4.7	8.7	.54	$2X10^{16}$
	6A	5.3	11.6	.45	$7.5X10^{15}$
	8A	14.3	34.0	.42	$5X10^{15}$
Implanted Regions	1B	9.1	9.3	.98	$2X10^{18}$
	4B	12.5	12.7	.98	$2X10^{18}$
	6A	11.5	12.7	.90	$1X10^{18}$
	8A	34.5	37.5	.92	$1.2X10^{18}$

Details of the capacitance-voltage measurement were described in the last section. The C-V curves were obtained using an X-Y plotter, and they were plotted on graph paper. The capacitors were fabricated on both the implanted and the non-implanted regions; therefore, capacitance-voltage measurements were also performed on both the implanted and the non-implanted regions. Having data on both the implanted and the non-implanted regions made it possible to compare the data.

As expected, the C-V measurement showed heavy impurity concentration in the implanted region. These impurities were as high as $2X10^{18}$ atoms/cm^3 which is a very heavy implantation. Of course, as was stated in the first chapter, there was a limitation. In this experiment, the mass analyzing magnet was not used and could have prevented the unwanted species to enter the surface of the substrate. In Table V impurity concentrations are given for a few selected samples that were obtained from the C-V curves. The data which is given in Table V compares the impurity concentrations of both the implanted and the non-implanted regions. The impurity concentrations were calculated using maximum and minimum capacitance from the C-V curves. Then these capacitance values were normalized; and using the prepared graph from Goetzberger (23) which gives the impurity concentration versus oxide thickness, the results were obtained. It should be stated here that this method was the fastest procedure to find the impurity concentration from the C-V plots. A few selected C-V plots are also given for the non-implanted and the implanted regions. In the non-implanted C-V curves which are

identified by sample numbers, there appears a large valley, i.e. the maximum and the minimum capacitance differ by a large margin. And in the implanted C-V curves, also identified by sample numbers, one can see that the curves have flattened out; and the difference between the minimum and the maximum capacitance is small. Also in the given C-V curves, it is shown if the samples were p-type or n-type which makes it easier for the readers to interpret the C-V curves.

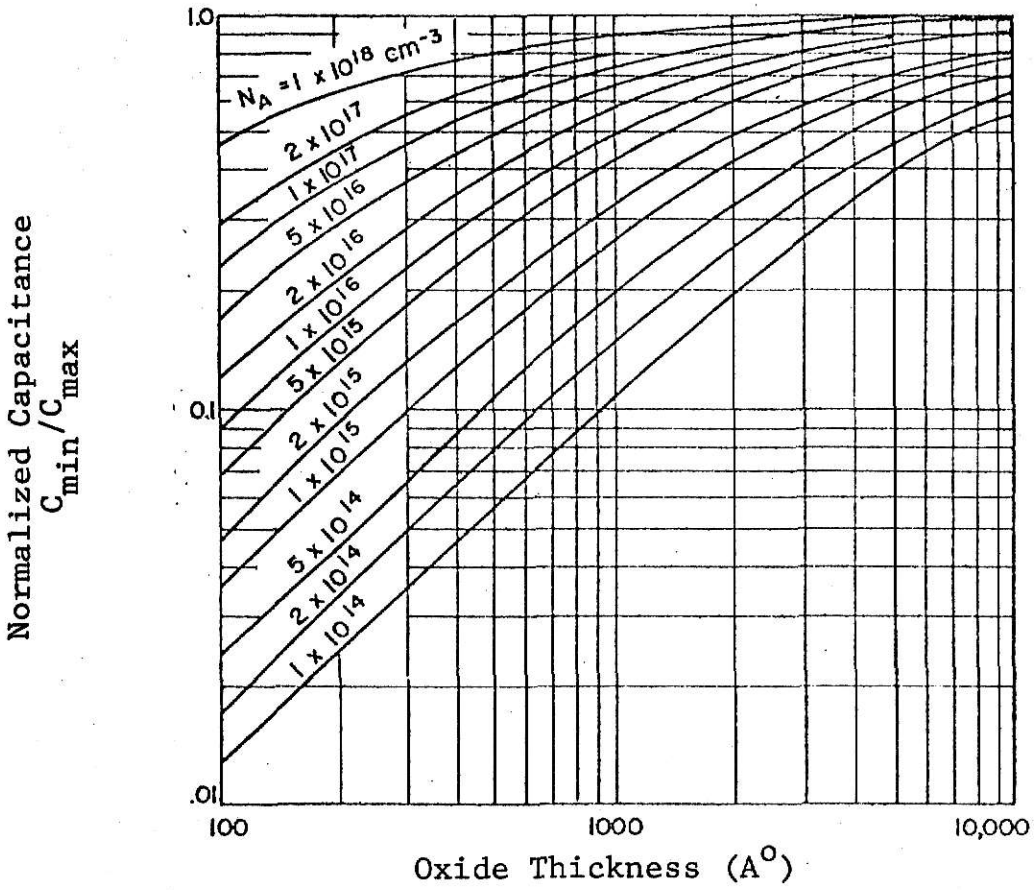


FIGURE 4.5.1. Normalized capacitance versus oxide thickness for MOS capacitors from [Goetzberger (23)].

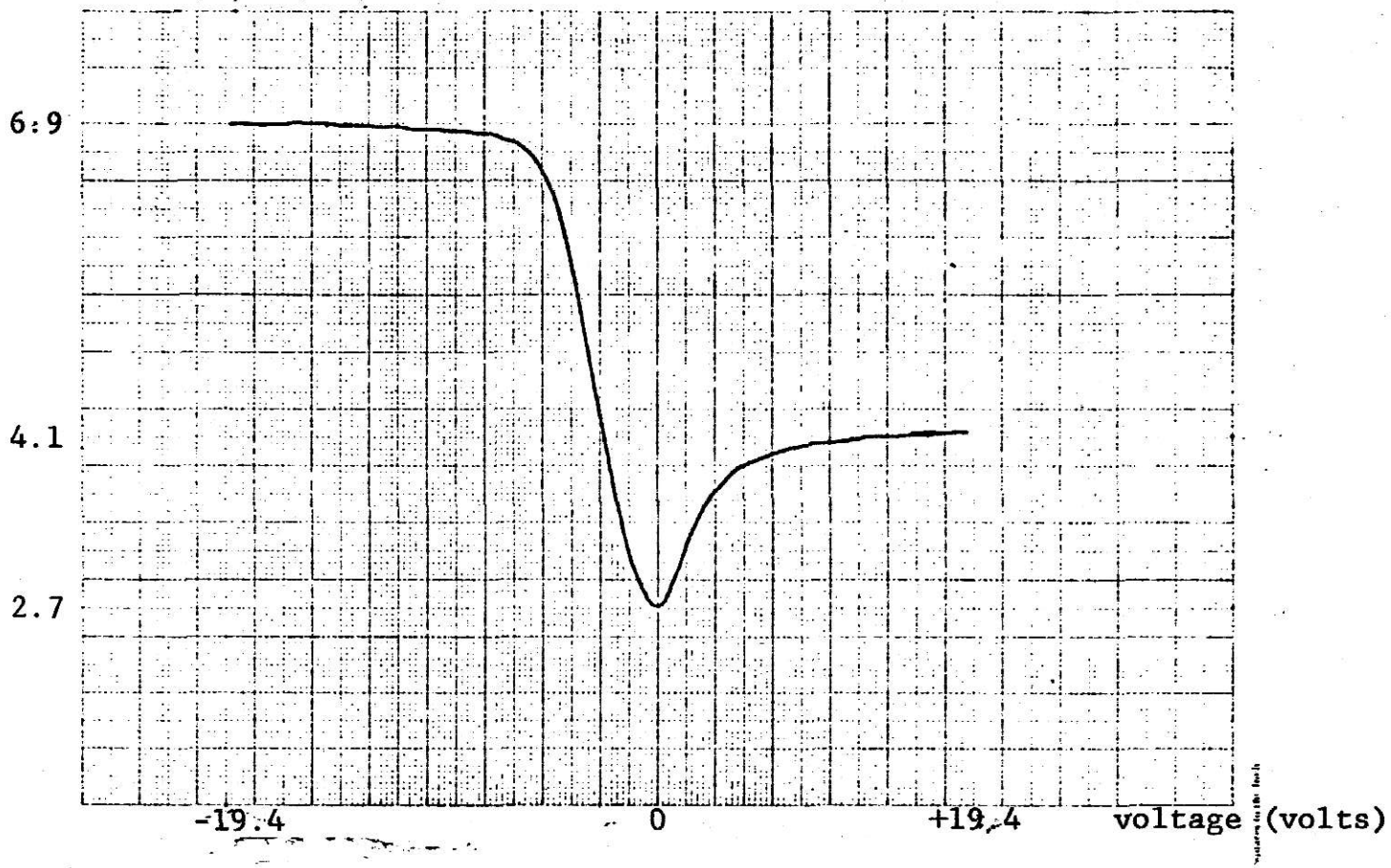
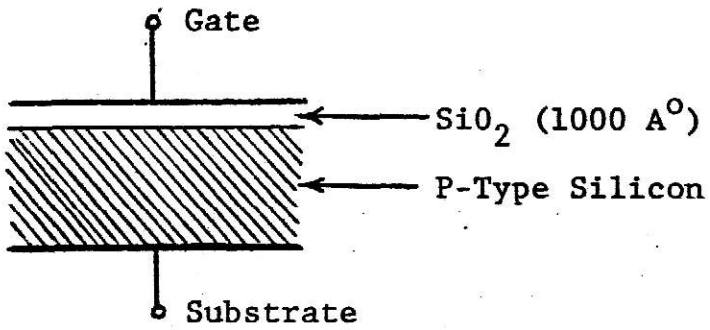


Figure 4.5.2

SAMPLE #1B

Non-Implanted Region



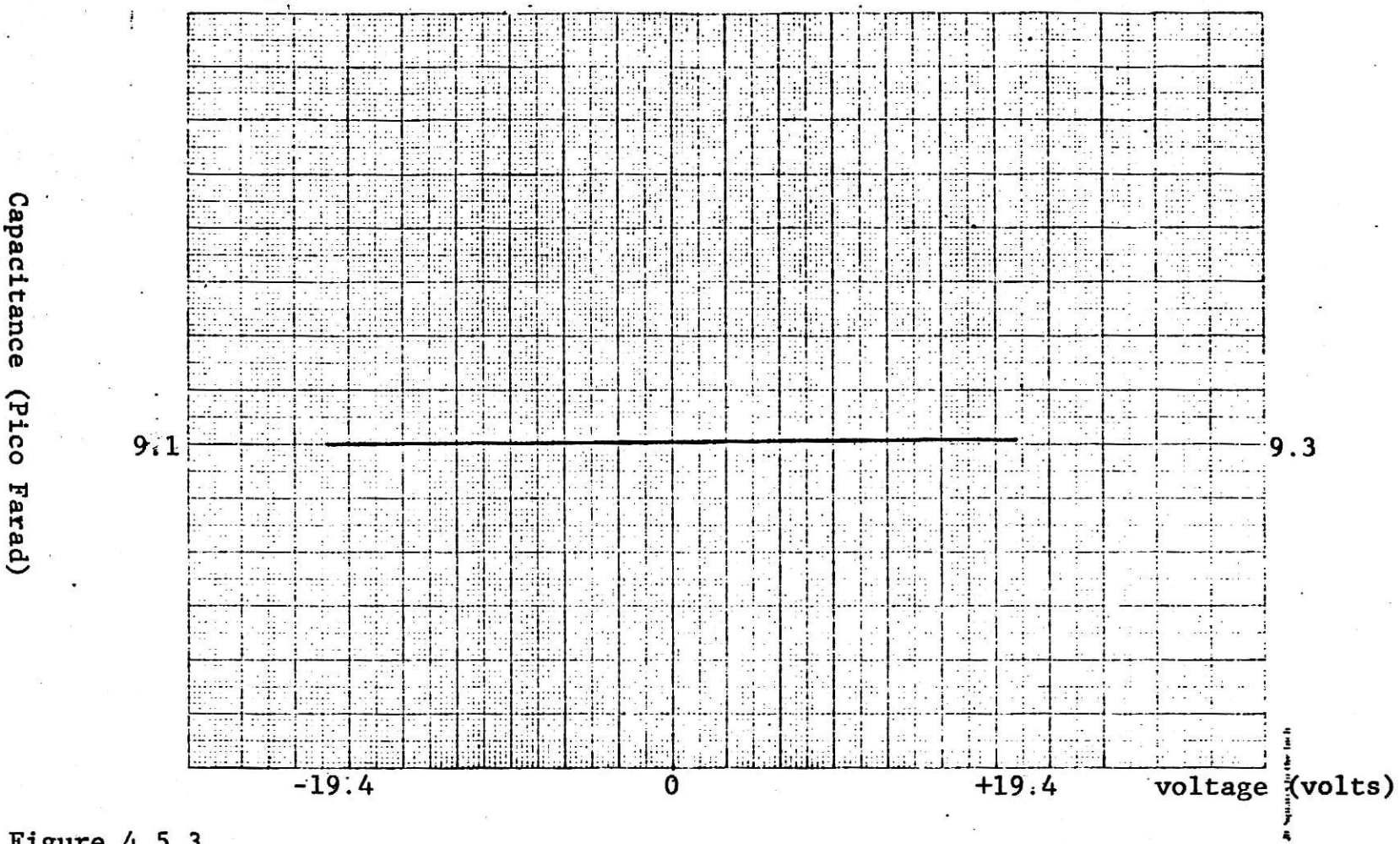
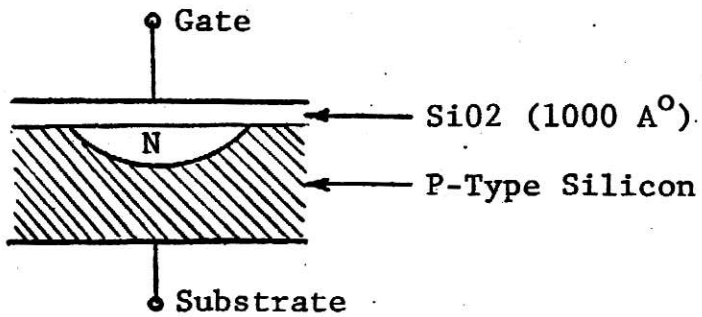


Figure 4.5.3

SAMPLE #1B

Nitrogen Implanted Region



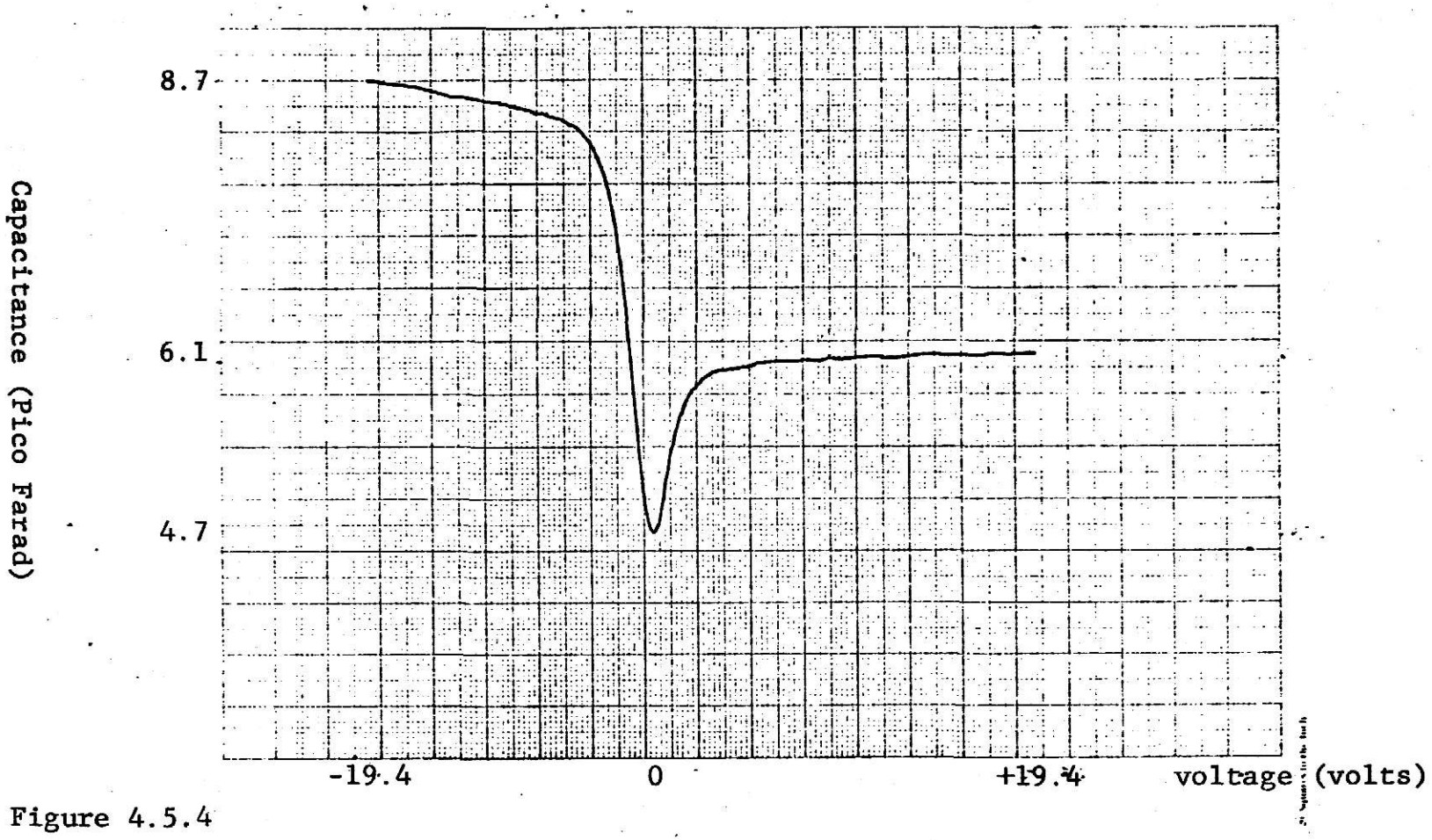
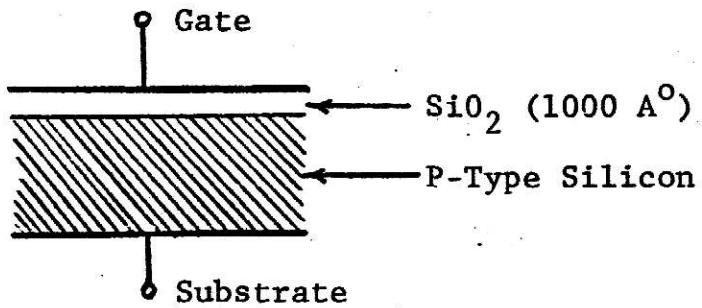


Figure 4.5.4

SAMPLE #4B

Non-Implanted Region



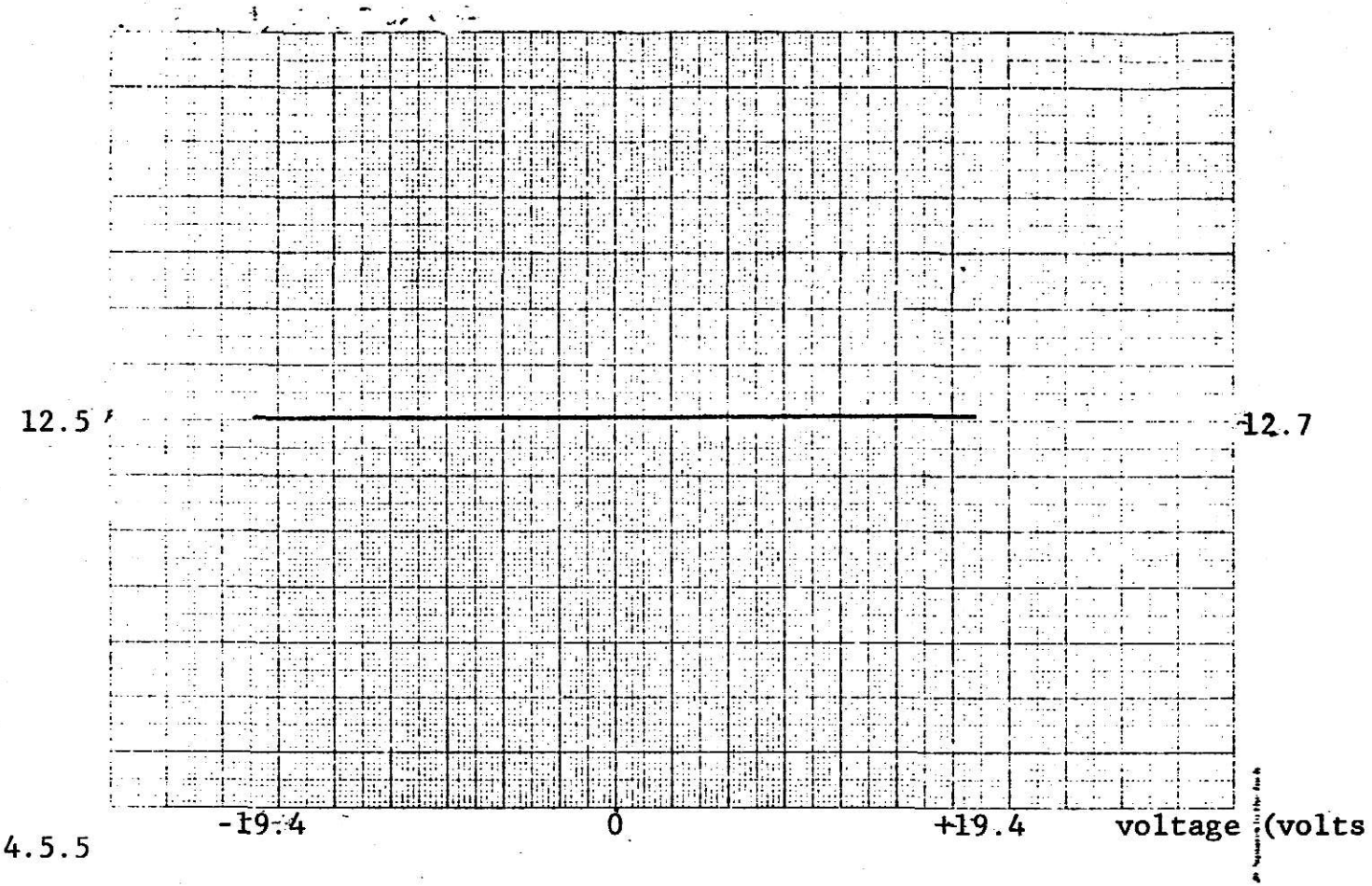
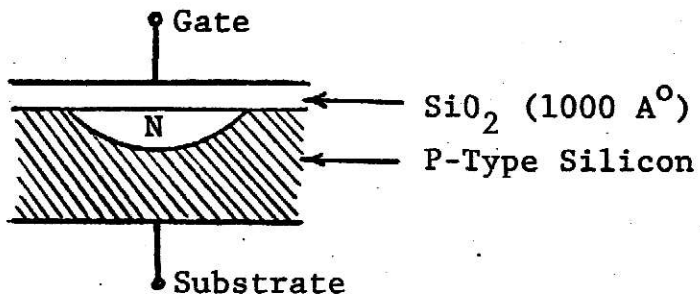


Figure 4.5.5

SAMPLE #4B

Nitrogen Implanted Region



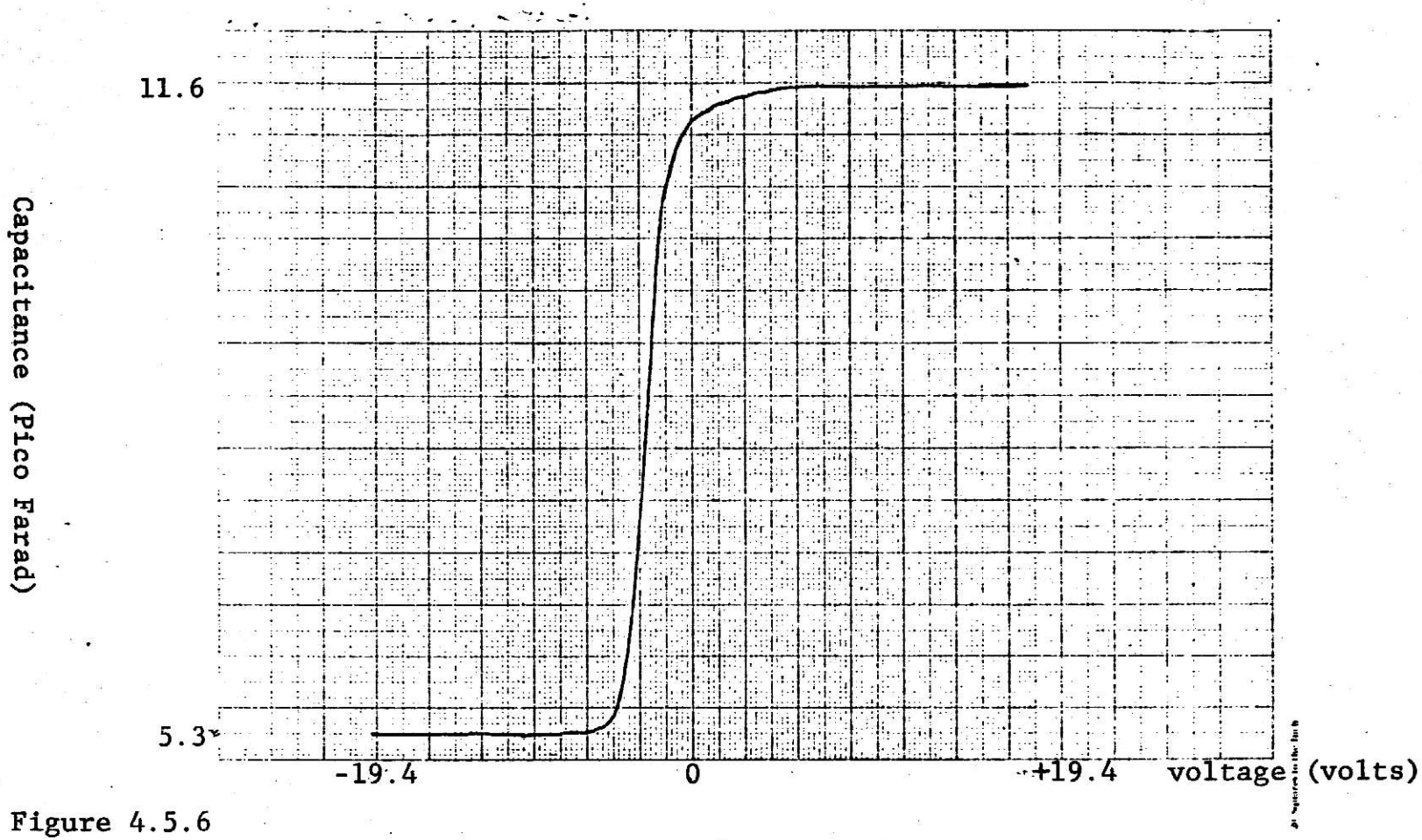
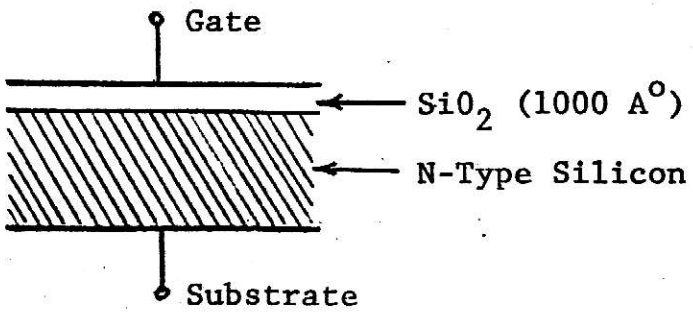


Figure 4.5.6

SAMPLE #6A

Non-Implanted Region



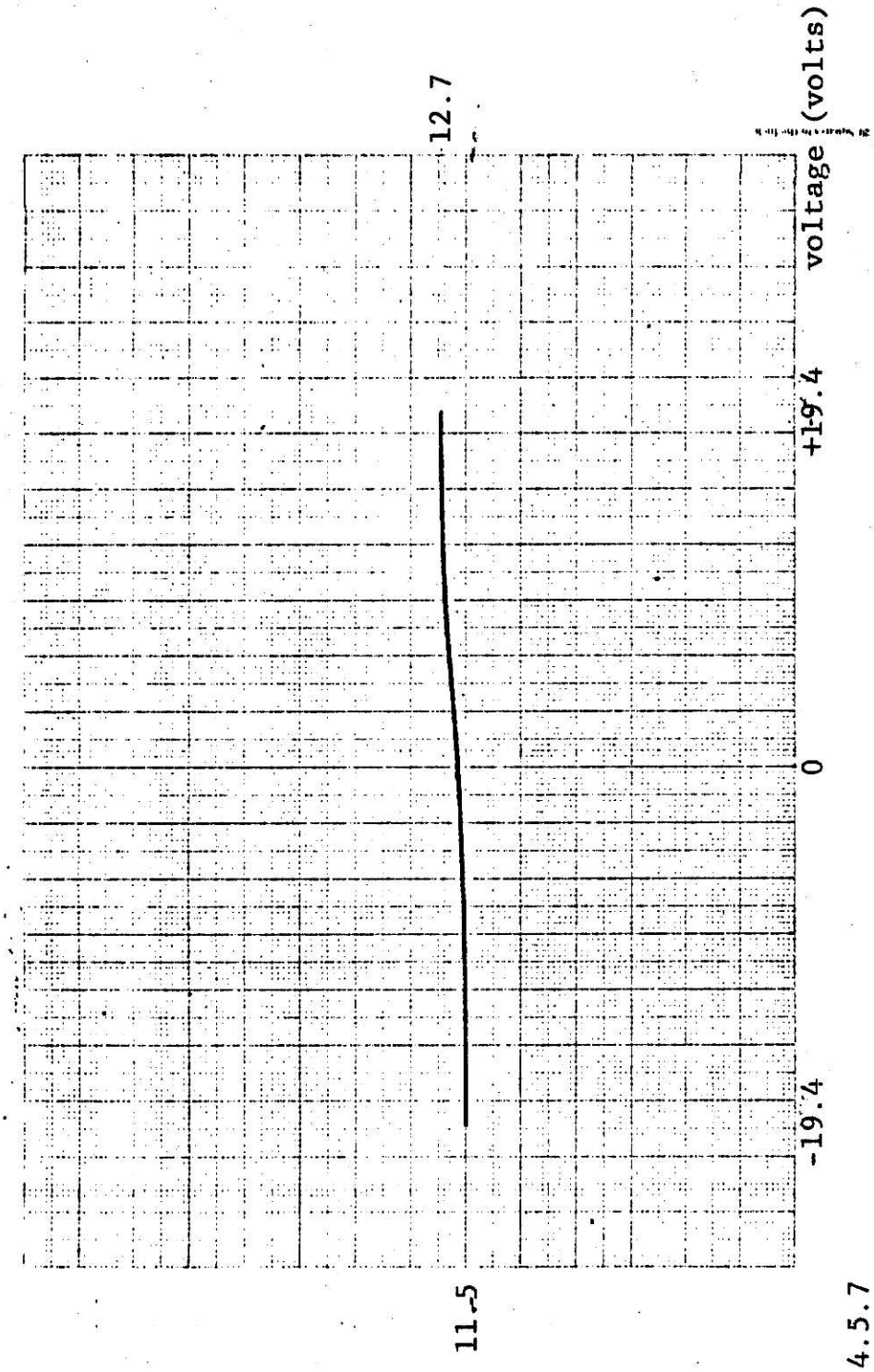
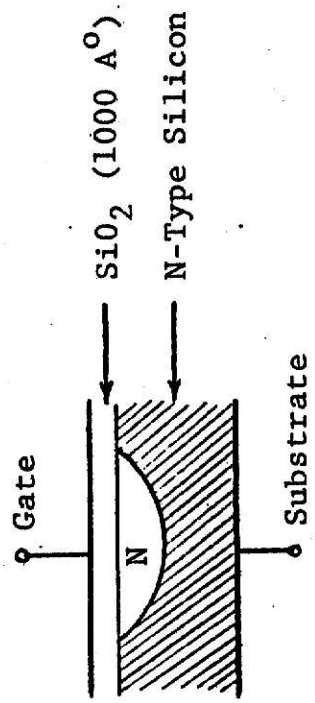


Figure 4.5.7

SAMPLE #6A

Nitrogen Implanted Region



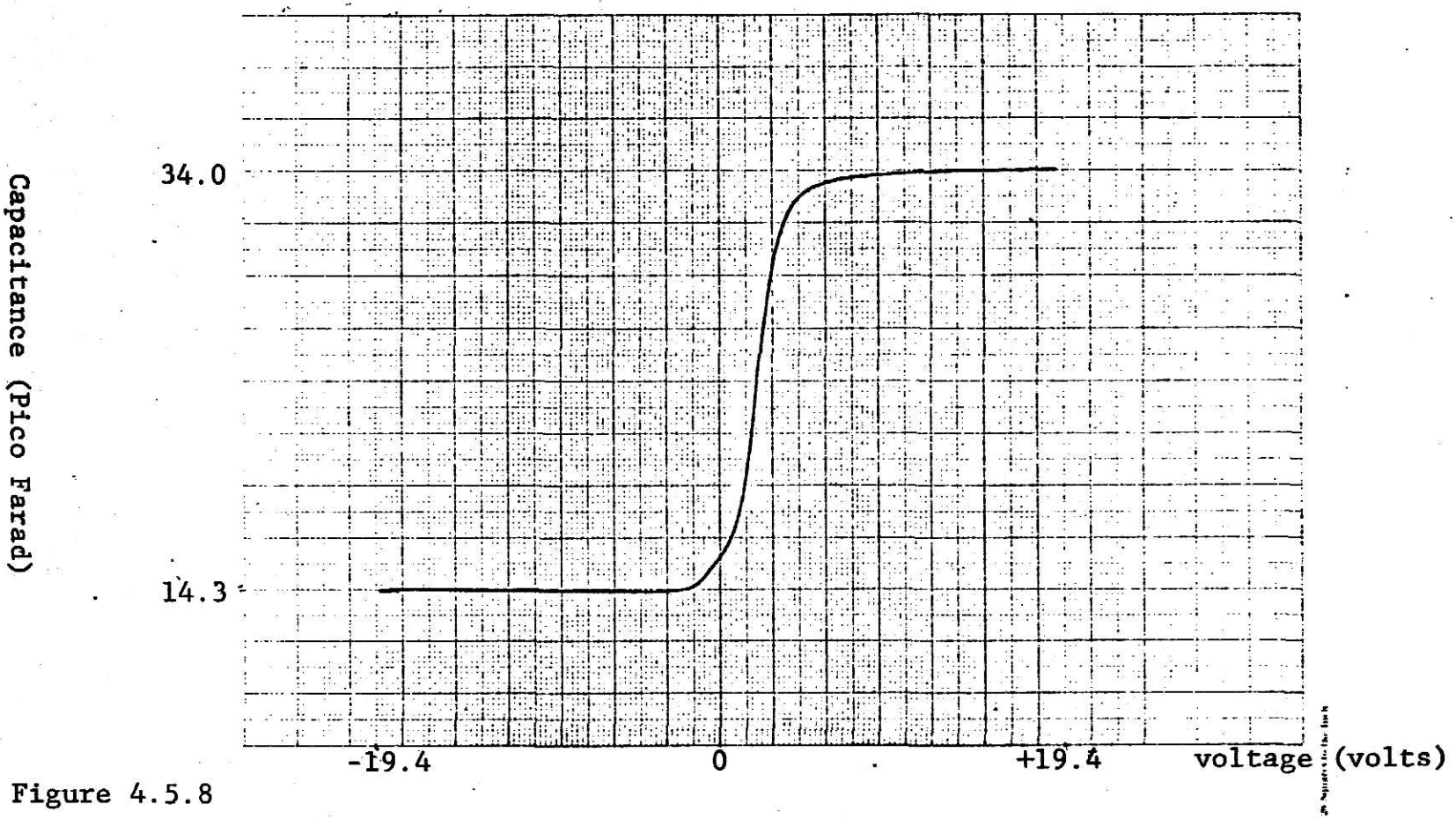
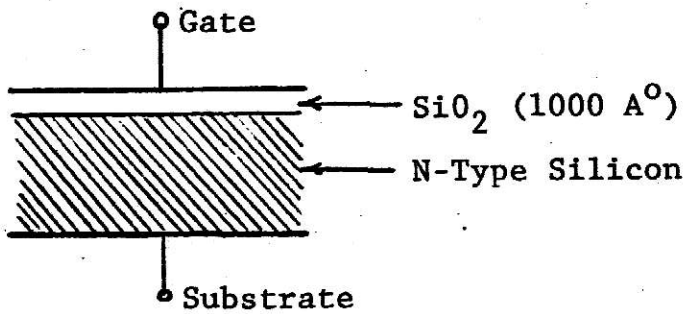


Figure 4.5.8

SAMPLE #8A

Non-Implanted Region



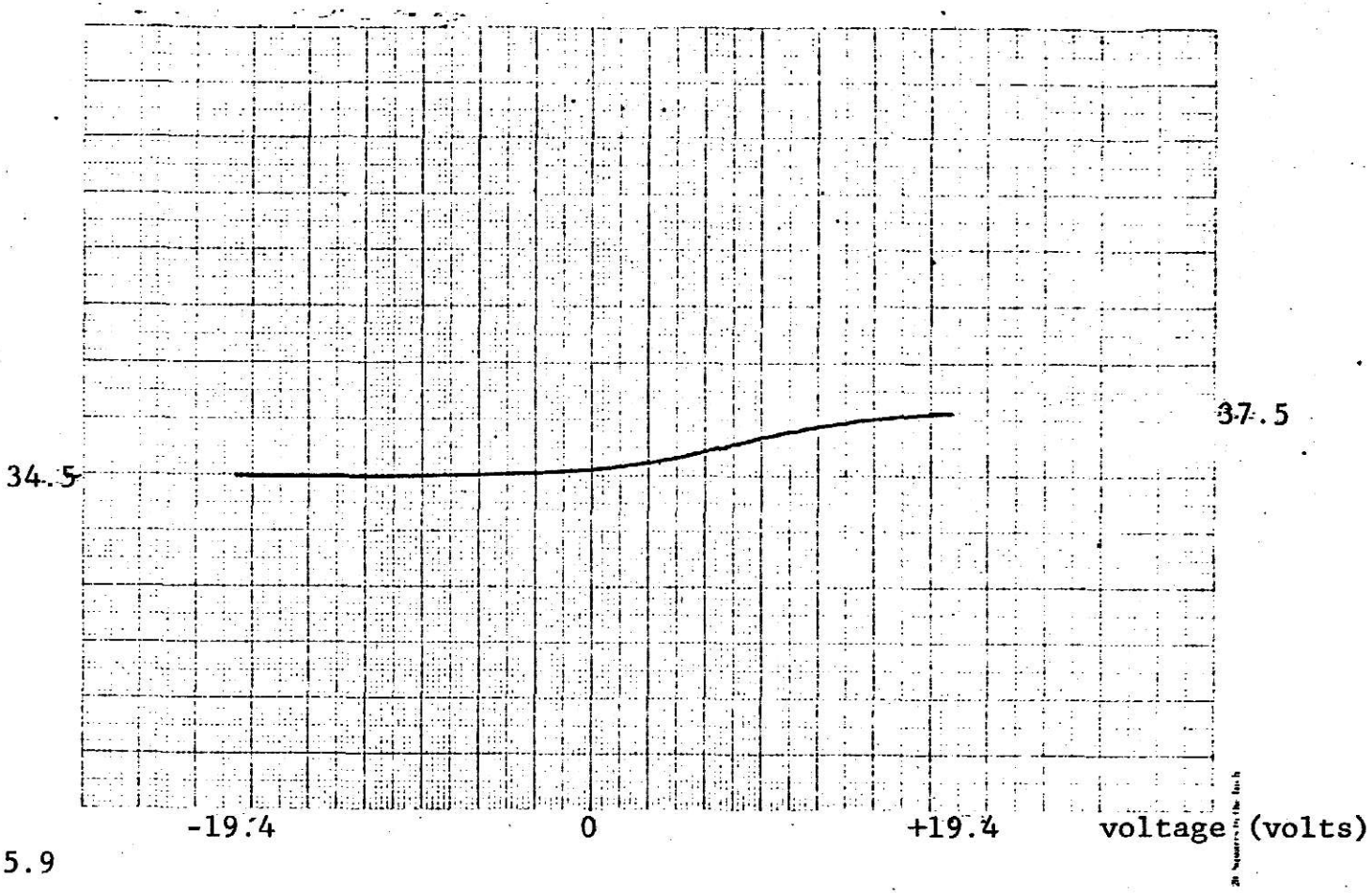
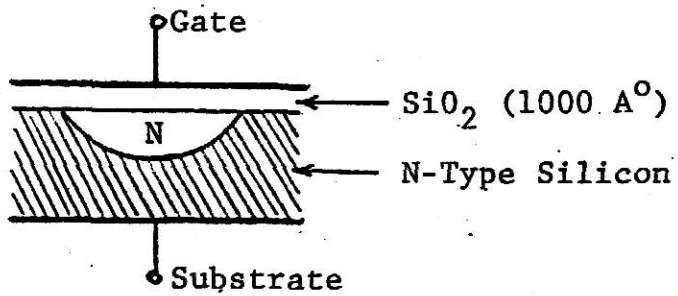


Figure 4.5.9

SAMPLE #8A

Nitrogen Implanted Region



CHAPTER V

5.1 Conclusions

The purpose of this study was to implant nitrogen in both n-type and p-type silicon using the Cockcroft Walton accelerator available in the Electrical Engineering Department and to analyze the samples by fabricating some kind of device on them. The samples were cleaned (using the cleaning procedure), then implantations were performed on them at room temperature. The beam currents were monitored and were recorded for the different energies. The damages that were created during implantation were observed using a scanning electron microscope in the Entomology Department. Some of these damages were repaired by annealing the samples.

The samples were bombarded with ion doses between $1.43X10^{15}$-$7.13X10^{16}$ ions/cm^2 which is a heavy doping. Therefore, it was necessary to anneal the samples at a higher temperature (between 600-800 ^{o}C). The color of the samples after implantation varied from dark blue to white gray, and the color change started disappearing after the samples were annealed at a higher temperature. This suggested some kind of crystal recovery after heavy bombardment. The disappearing of the color from the implanted regions does not always mean crystal recovery. At times it is possible that at a high temperature some type of surface oxidation would occur and change the color of the surface.

For the preliminary measurements, the four point probe was used to perform the resistivity measurement on both the implanted and the non-implanted regions. The data that was obtained showed that the resistivity of the implanted regions decreased with the increasing of the anneal temperature. The measurements were not very accurate because of the difficulties that were involved with making contact to the implanted regions. It was difficult at times to repeat the measurements.

A thin layer of oxide was formed on the samples; and to prevent having trapped charges under the oxide which was grown using steam oxidation, the samples were heated in a nitrogen atmosphere. Having a good clean furnace was very important in growing the oxide. During the experiment, it was noticed that if the furnace was not clean and had some dust particles in it, the oxide that was grown in this furnace was not a good oxide and had some pinholes in it.

For the fabrication of the Insulated Gate Field Effect Transistors, a p-type substrate was used, and the fabrication was accomplished using a photomask and alignment. The IGFET that was fabricated did not work properly, and the gate electrodes were used for the capacitance-voltage measurement.

The reason for failure of the fabricated transistors was that they needed to be fabricated in a super clean room, and this was not possible here. Therefore, contamination was suspected. Also heavy implantation may have caused the failure of the transistors. A scanning electron microscope was used to study one of these fabricated transistors. See Figure 4.4.7 which shows

some type of either a contaminated or a damaged surface due to heavy dose implantation.

The capacitance-voltage measurements were made on the fabricated transistors. It was found that the capacitance-voltage measurement is very easy to make and could be performed in between steps of the fabrication of the devices. The data that was obtained from the capacitance-voltage measurements was easy to analyze, and the C-V curves analysis showed that the samples were heavily doped.

Another point which should be discussed here is that when nitrogen is heavily implanted into a silicon, it is possible to form a layer of non-conducting film (Si_3N_4). This possibility was not investigated; and therefore, it was not known actually if this layer existed. And it should be mentioned here that if this was the case which a non-conducting film was formed, this may have also been one reason for the failure of the IGFET.

Another reason for the failure of the IGFET that was not mentioned before is that the geometry of the fabricated devices could have been incorrect. In this experiment the samples were implanted first, and then the oxide layer was grown and etched later. The actual procedure should have been to first grow the oxides on the samples and open the windows in the oxide, and then to implant the nitrogen through the windows to form a drain and a source in the transistors. This possibility again was not clear; and as was mentioned, the geometry could have caused the failure of the transistors.

The results of the resistivity measurement given in Table IV show that at first when the samples are not annealed, the resistivity of the implanted region is infinite. Annealing the samples between 500-700 ^{o}C still resulted in having a high resistivity region. After 750 ^{o}C the resistivity of the implanted regions started to decrease, indicating that the samples needed to be annealed at a higher temperature, between 800-900 ^{o}C for heavy implantation.

APPENDIX A

Silicon Substrate Cleaning Procedure

Apparatus, chemicals, and equipment that are needed:

1. Sulphuric acid reagent (H_2So_4)
2. Nitric acid reagent (HNo_3)
3. 48% hydroflouric acid (HF)
4. Trichloroethylene
5. Distilled water supply
6. Double distilled water supply
7. Hot water bath (90-95 ^{o}C)
8. Plastic beakers
9. Squirt bottles
10. Plastic tweezers
11. Ultra-sonic cleaner
12. Methanol
13. Acid and HF acid hood

After all of the chemicals and equipment are provided, the acid hoods should be turned on. Rubber gloves should always be worn when one is handling acids.

Preparation

1. Mix a solution of 50% H_2So_4 and 50% HNo_3 (at least 300 ml).

2. Place half of the HNo_3 - H_2So_4 solution in each of the two beakers.
3. Place approximately 150 ml of H_2So_4 in a plastic beaker.
4. Place approximately 150 ml of trichloroethylene in a plastic beaker.
5. Fill a squirt bottle with methanol.
6. Fill a squirt bottle with distilled water.
7. Place the four beakers mentioned in steps 2, 3, and 4 in the hot water bath.
8. Place about one inch of water in the ultra-sonic cleaner.
9. Fill a beaker with HF acid. Keep it under the HF acid hood. Use gloves and a nylon apron with this. (USE EXTREME CAUTION.) Know how to handle HF acid.
10. Fill a clean beaker with double distilled water.

After all preparation is made one should procede with the following steps.

Procedure

1. Place a wafer that is going to be cleaned in a hot trichlor for 5 minutes. Use plastic tweezers to handle the wafers at all times. Immerse the wafer with the polished face up.
2. Remove the wafer from the trichlor and squirt methanol over its surface.
3. Immerse the wafer in the distilled water and agitate for 30 seconds.
4. Dip the wafer (polished side up) in the H_2So_4 for 10 minutes.

5. Place the wafer and the H_2So_4 in the ultra-sonic cleaner for 5 minutes.
6. Immerse the wafer in a fresh distilled water bath for 2 minutes
7. Place the wafer in HNo_3 - H_2So_4 solution (polished side up) for 10 minutes.
8. Place the wafer and the acid solution in the ultra-sonic cleaner for 5 minutes.
9. Submerge the wafer in a fresh distilled water bath for 2 minutes.
10. Handling the wafer with the tweezers, dip the wafer in the HF acid for 30 seconds.
11. Squirt the wafer faces carefully with the distilled water.
12. Immerse the wafer in a distilled water bath for 1 minute.

APPENDIX B

Oxidation

Oxidation plays an important role in the fabrication of silicon devices. The oxide (SiO_2) serves three major useful functions. First, it can act as a mask which blocks the chemical impurities, donors and acceptors from entering the silicon crystal. Second, it can work as a protective shield to prevent contamination of the silicon surface. Third, the oxide can serve as an electrical insulator.

There are many ways to grow oxide on silicon. One of the most widely used methods is steam oxidation, in which basically the oxide is thermally grown on the top of the silicon. The apparatus needed for steam oxidation is shown in Figure B1. Highly purified water is boiled in a flask, and the water vapor is allowed to pass the silicon wafers placed in a quartz boat assembly. The thickness of the oxide can be measured in three different ways which are:

1. by optical measurement
2. through color change
3. from experimental curves

The measurement that was used here was from the experimental curves given by Burger (17) (Figure B2), and it was checked by using the optical method.

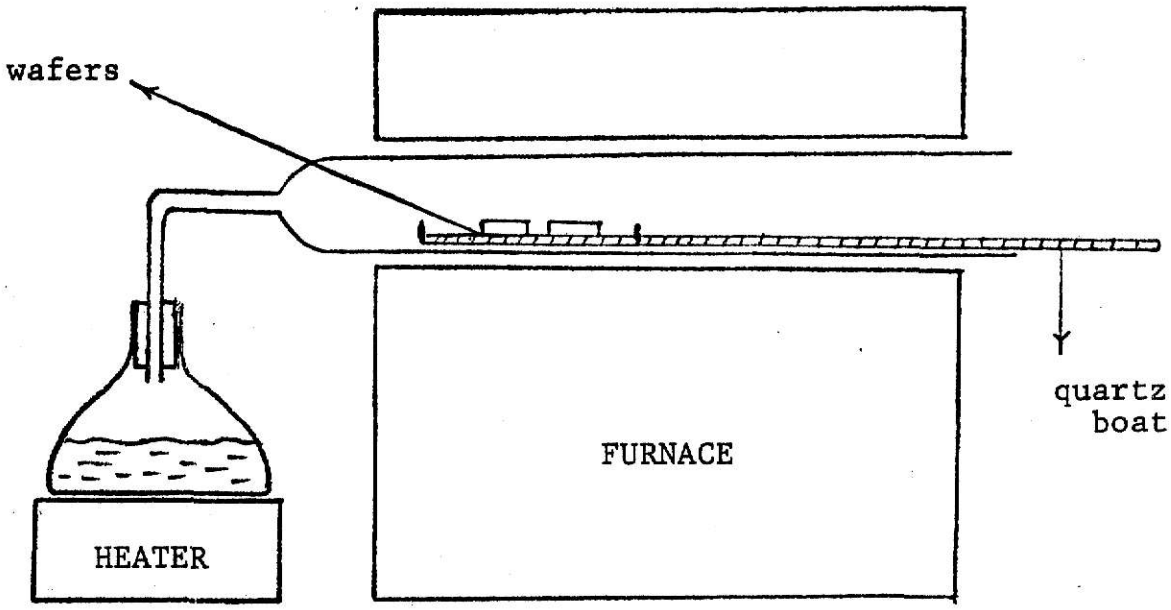


FIGURE B1. Steam Oxidation Set-Up

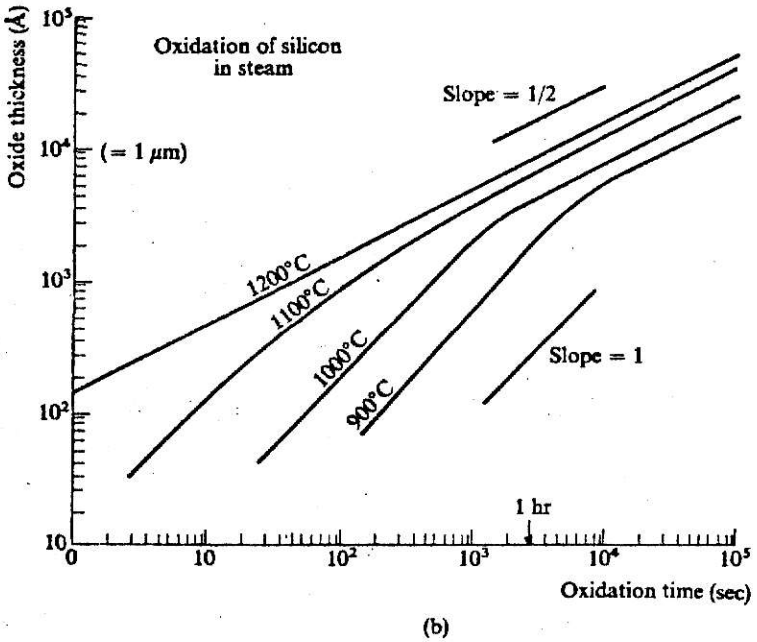


FIGURE B2. Oxide Thickness as a Function of Reaction Time and Temperature

APPENDIX C

Photoresist Processes

Photoresist techniques have been well developed in recent years for use in semiconductor work. There are two types of photoresist. One type is positive photoresist in which, like Shipley photoresist, when exposed to an ultra violet light using some mask and then is developed, the places that have been exposed to the ultra violet light will wash off. The second type of photoresist is negative photoresist, such as Kodak photoresist (KPR). When KPR is exposed to an ultra violet light using some mask and is developed, the places that have been exposed to the ultra violet light will remain. The main use for both of these two photoresist has been to etch some selected area with either oxide or some metals. The photoresist also has been used in ion implantation processes as a mask, i.e. it will cover the areas where implantation are not needed. Both the Shipley photoresist and the KPR were available here, but for this experiment only the Shipley photoresist was used.

The following procedure was followed when the Shipley photoresist was used:

1. After the oxide has been grown on the silicon substrate, it should be kept under a clean hood bench. (See Appendix B.)

2. The photoresist is applied to the surface of the silicon substrate using a syringe which is fitted with a microscope filter.

3. Place 3 drops of photoresist on the silicon wafter and spin for 30 seconds at 3000 rpm.

4. Repeat step #3 for one more time and inspect the silicon wafer visually to make sure that the photoresist has been distributed evenly over the surface of the silicon wafer.

5. Keeping the silicon wafer under the clean hood bench, bake it under a heat lamp for 15 minutes. Care must be exercised not to overheat the photoresist.

6. After baking, use the mask that is needed for the pattern and expose it to an ultra violet light for 2 minutes.

7. Mix a solution of 50% Shipley developer and 50% distilled water.

8. Develop the photoresist-coated wafer for 15 seconds in the developer solution that was prepared.

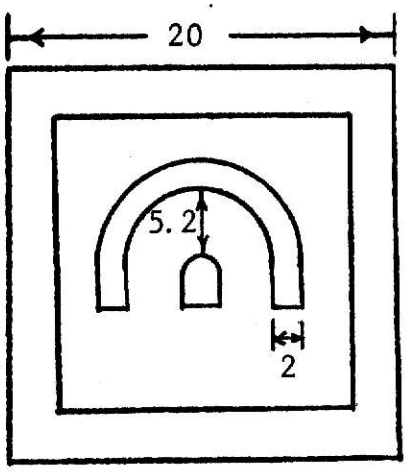
9. Rinse the silicon wafer with the distilled water, and then the patterns should be inspected under the microscope for defects.

10. Harden the photoresist by baking the wafer under the heat lamp for 15 minutes.

11. After the photoresist patterns have hardened, the wafer is ready to be etched off.

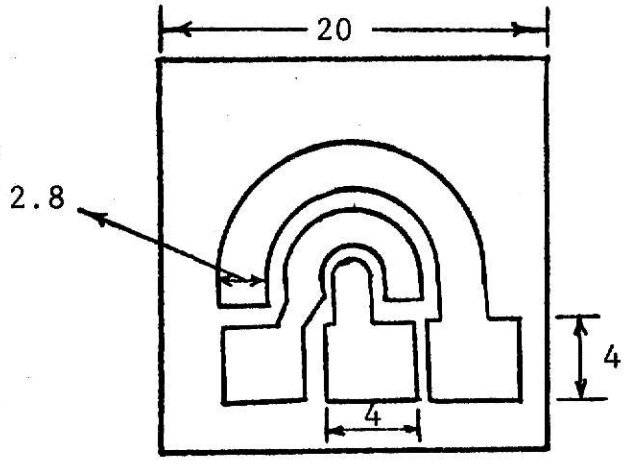
APPENDIX D

Dimensions of the Masks for Fabrication of IGFET



Mask #02

This mask was used for opening windows in oxide.
(dimensions are in mils)



Mask #03

This mask was used for metalization.
(dimensions are in mils)

APPENDIX E

Definition of Terms

Annealing: Annealing is the thermal treatment of a damaged solid which eventually results.

Avalanche: At a higher reverse voltage, minority carriers can attain sufficient volicity to dislodge outer-shell electrons, which in turn can gain sufficient volicity to dislodge more outer-shell electrons, etc., with the result that there is significant increases in reverse current.

Barrier Potential: The voltage across a p-n junction. This voltage is produced by the layer of charged atoms on both sides of the junction. Approximately 0.3 volt for germanium and 0.7 volt for silicon.

Breakdown Voltage: The value of the reverse voltage beyond which there is a significant increase in the reverse current.

Channeling: The condition in which ions that do not collide with the target atoms and travel far into the substrate.

Covalent Bonding: Takes place when electrons are shared by a bound nuclei. The hydrogen molicule (H_2) illustrates this type of bond.

Crystal: The internal structure of a solid piece of silicon. In this structure, each atom has four neighboring atoms that share outer-shell electrons.

Crystal Damage: After each implantation, the crystal structure of the atoms will be damaged because of the collision between the implanted ions and the target atoms.

Depletion Region: A region on both sides of a p-n junction. It is relatively empty or depleted of free charges and primarily contains immobile ionized atoms.

Doping: Adding impurity atoms to pure germanium or silicon in order to increase the number of free electrons or holes.

Electronic Collisions: Results when the energy transfer occurs between the electrons of the incident ion and the target atoms.

Electronic Stopping: The effect of the electronic collision phenomena is called electronic stopping.

Extrinsic Semiconductor: Doped semiconductors.

Forward Bias: Applying external voltage across a diode with a polarity such that the conventional current is trying to flow in the direction of diode triangle, that is from a p-type to an n-type material.

Hole: A vacancy in an outer-shell of an atom. It can be produced either by thermal energy or by doping.

Intrinsic Semiconductor: Pure silicon. The only charge carriers are the free electrons and the holes produced by thermal energy.

Ion: If one or more electrons are removed from an atom, the remaining positively charged structure is called a positive ion. A negative ion is an atom which has gained one or more extra electrons.

Ion Implantation: Atoms of the desired doping element are ionized and accelerated to a high velocity and then caused to enter a substrate lattice.

Ionic Bonding: Occurs when there is an exchange of electrons. The donor becomes positively charged, and the acceptor is negatively charged.

Ionization: The process of losing or gaining electrons is called ionization.

Lifetime: The average amount of time that a free electron or a hole exists after being generated but before recombining.

Metalic Bonding: Leaves the valence electrons relatively free to wander through the lattice structure, acting much like a gas.

N-Type Semiconductor: A semiconductor that has been doped to produce an excess of free electrons.

Nuclear Collision: Involve the stronger electrostatic force interactions between the nuclei of the incident and the target atoms.

Nuclear Stopping: The effect of nuclear collision phenomenon is called nuclear stopping.

P-Type Semiconductor: A semiconductor that has been doped to produce an excess of holes.

Recombination: The merging of a free electron and a hole.

Reverse Bias: Applying external voltage across a diode with a polarity such that conventional current is trying to flow against the diode triangle, that is, from an n-type to the p-type material.

Semiconductor: Material such as germanium or silicon whose electrical properties lie between those of an insulator and a conductor.

Van der Waal Bonds: Are relatively weak bonds due to the nonsymmetrical distribution of electrons in atoms or molecules.

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NITROGEN IMPLANTATION IN N-TYPE AND P-TYPE SILICON

by

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ABSTRACT

In this study, some important aspects of an ion implantation system are discussed. Also some principles that are involved in the evaluation of ion implanted regions is presented.

Nitrogen has been implanted into the p-type silicon (2.8-3.5 Ω-cm resistivity and <111> orientation) and the n-type silicon (40-70 Ω-cm resistivity and <111> orientation). The samples were implanted with a dose of $1.13X10^{15}$-$7.13X10^{16}$ ions/cm^2 and were annealed in a nitrogen atmosphere furnace to recover the damaged crystal. Also some of the surface damages were studied using a scanning electron microscope.

Resistivity measurements were performed on the samples using four point probes at different steps of the temperature annealings.

Silicon oxide was grown on the samples; and on the p-type substrates, Insulated Gate Field Effect Transistors were fabricated using the photoresist techniques. The transistors were analyzed using a curve tracer; no sign of working transistors was found. Contamination was suspected for the failure.

Capacitors were formed on the samples by growing a thin layer of oxide on them, and metalization was performed by evaporating aluminum on the samples. Capacitance-voltage measurements were performed on these samples; and using an X-Y plotter, C-V curves were obtained for the different samples. Also the gate structure of the Insulated Gate Field Effect Transistors was used to perform the capacitance-voltage measurement.

From the obtained C-V curves and the resistivity measurement, it was found that the samples were heavily doped up to $2X10^{18}$ atoms/cm^3.