A DATA ACQUISITION SYSTEM WITH SWITCHED CAPACITOR SAMPLE-AND-HOLD

by

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

DATA ACQUISITION SYSTEM
WITH SWITCHED-CAPACITOR SAMPLE-AND-HOLD

INTRODUCTION

To increase the number of potential applications for an electronic device, designers usually attempt to limit the values of such parameters as size, weight, cost, and power consumption. One well known example is the development of computers. They have evolved from large, expensive, power hungry, laboratory curiosities to small, lightweight, portable, everyday machines. A second example, important to the progress of computers, is the development of analog-to-digital converters, which link digital computers to an analog world. Many of the improvements made in these devices are every bit as dramatic as the improvements made in computers.

Still, there are some applications of analog-to-digital converters that have received insufficient attention. This is the reason the data acquistion system (DAS) described in this thesis has been designed. Its target host system is a low frequency signal processing system that requires a digitizer with high resolution and very low power consumption. Highlights of the DAS' specifications include

- input voltage range: [-5,+5] V

- resolution: 15 bits
- maximum conversion rate: 500 Hz
- maximum integral linearity error: ±1 LSB
- total system power consumption: 60 mW

The circuit requires no custom components; yet it should be very nearly possible to construct it on a single 3"x5" printed circuit board.

The design evolved from an earlier design for a DAS that was intended for a similar host system. The unique feature of the new DAS is the switched-capacitor sample-and-hold (S/H); this S/H operates in the normal manner except that it has the additional capability of making a low-resolution estimate of the sampled input. Because the DAS' analog-to-digital converter (ADC) is only used to determine the error in this estimate, the ADC does not need to have as large an input range as required when using an ordinary S/H. The error measurement is combined with the switched-capacitor S/H's estimate to produce a high resolution quantization of the analog input.

Three other important features of the DAS are power-switched components, microcomputer control, and self-calibration. The average power consumption of the system is minimized by turning components off when not in use. Thus, the system's average power consumption can be varied by adjusting the sampling rate. A powerful single chip microcomputer (MC68HC11) is included in the circuit to

provide most of the necessary control logic, and thereby eliminate several digital logic chips. Self-calibration--another major function of the microcomputer--eliminates the need for external adjustments (such as potentiometers) and errors due to component drift with temperature variations.

Unfortunately, the DAS is not fully implemented and additional testing and development work will be necessary to bring it to completion. The designers have constructed a wire-wrapped test system that should provide the information necessary to modify the system such that its performance expectations are met.

Background material for the DAS design may be found in the references.[1-4 8 11]

CHAPTER 1. THE EVOLUTION OF A LOW-POWER DAS

A Critical Review of Earlier Data Aquisition System

Development of the DAS is primarily based upon work by Ragsdale,[2] Doerfler,[4] Bradley,[1] Reed,[3] and Lucas. The DAS toward which their work was directed can be used in applications very similar to those for which the new DAS is intended. The subject of this chapter is the role the earlier DAS played in the evolution of the new DAS. To distinguish between the two systems, the earlier DAS will be called the RDB DAS, after its designers, and new DAS will be called the switched-capacitor DAS, for its sample-and-hold.

The initial design requirements for the RDB DAS were

- input voltage range: [-5,+5] V
- number of analog input channels: 2
- conversion technique: successive approximation
- resolution: 15-bits
- maximum differential linearity error: $\pm 1/2$ LSB
- maximum integral linearity error: ± 1 LSB
- maximum no. of missing codes: 0
- input bandwidth: 45 Hz
- maximum conversion rate per channel: 128 Hz
- form of digital output: two's complement
- control: microprocessor based

- supply voltages: ±7.5 VDC
- maximum power consumption (analog section): 80 mW
- fabrication requirement: easily reproducible with commercially available components

Two of these requirements were not met. The integral linearity of the system was greater than one LSB and there were some missing codes.[1]

Method of Conversion

The block diagram for the RDB DAS is shown in Figure 1.1. A single sign-magnitude successive approximation ADC serially converts two inputs held by a dual track-and-hold amplifier. Because it was not possible to purchase a suitable low-power 15-bit digital-to-analog converter (DAC), 15-bit resolution was obtained by having the system determine the polarity of the input, and then using a 14-bit DAC to successively approximate the magnitude. The DAC output voltage is inverted as necessary to be the same polarity as the input voltage.

Successful Features of the RDB DAS

Despite the RDB DAS' nonlinearity, it did demonstrate features that deserve attention. These features include power-switched components, track-and-hold amplifiers, an onboard microprocessor, shrewdly selected components, and DAC/ADC test procedures and software.

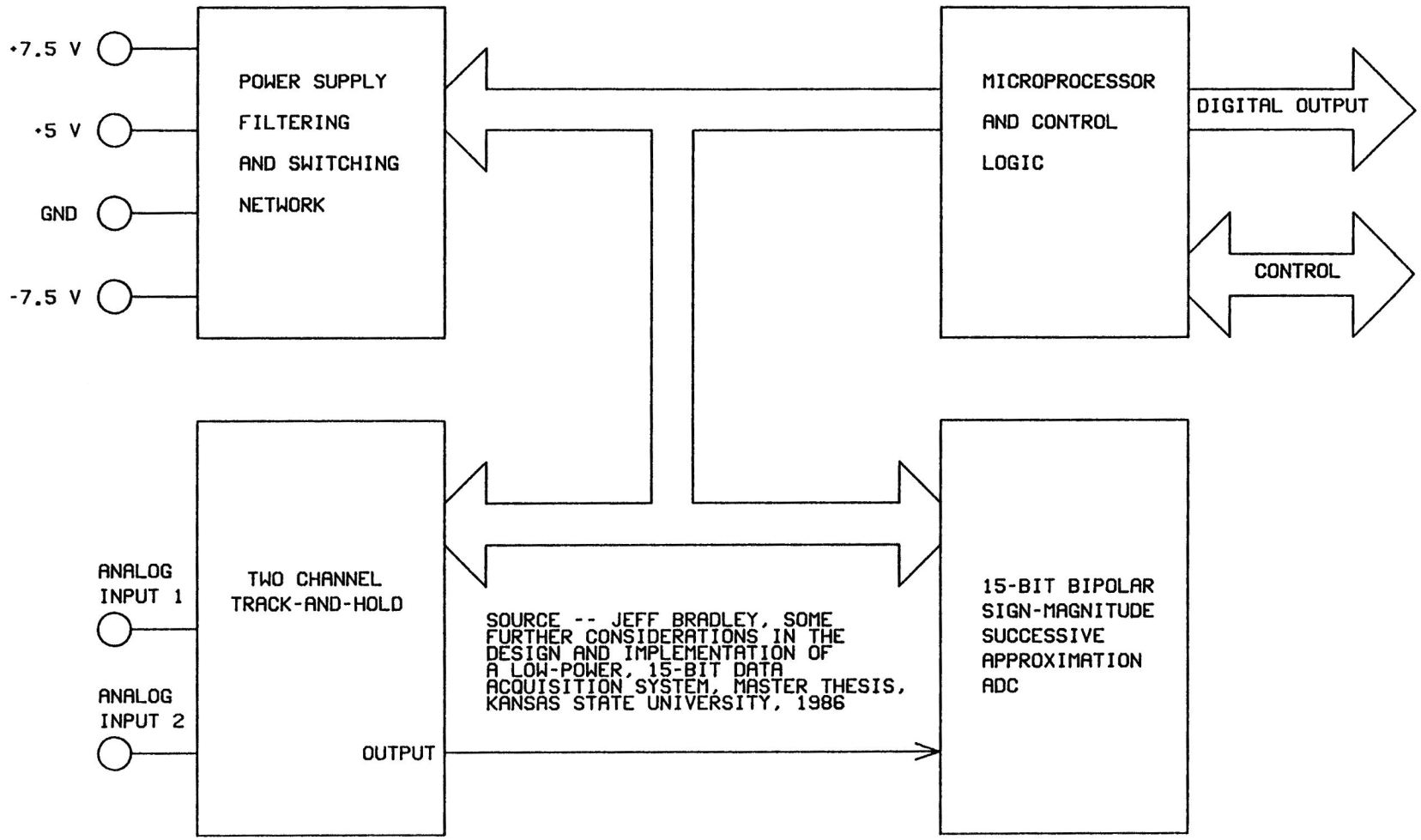


Figure 1.1 Block Diagram of the RDB DAS

Power-switched components -- The power consumption of the RDB DAS was minimized by power-switching components. The concept of power switching is to minimize average system power consumption by turning components off when not in use. The average power consumed by a power-switched component is equal to its continuous power consumption multiplied by its fractional duty cycle of operation.[2] By using this technique, the RDB DAS consumes only 36.5 mW.[1]

Track-and-hold amplifiers -- In contrast to sample-and-hold amplifiers, which ideally acquire the input signal instantly, track-and-hold amplifiers use an extended input acquisition period. Because a high slew rate is not required, a track-and-hold typically does not need an operational amplifier that consumes as much power as the operational amplifier used in a sample-and-hold. The RDB DAS made this tradeoff fairly successfully by using a dual track-and-hold amplifier that consumes only three milliwatts, and it is not power switched.[3]

Onboard microprocessor -- Developments of higher levels of integration in digital processors, which fuel the demand for a better DAS, also make it possible to add additional processing power to the DAS board itself. An onboard microprocessor can reduce chip count by providing numerous control functions. A second advantage is that a microprocessor can execute output code correction

algorithms to maximize linearity. For instance, the integral linearity error of the RDB DAS was almost six LSBs until software correction algorithms reduced it to slightly more than one LSB.

Shrewdly selected components -- To meet stringent design requirements, components must perform near their performance limits. Therefore, shrewdly selected components are necessary. Testing procedures, used by the designers of the RDB DAS, ensure that components perform within their manufacturers' specifications. These and other procedures, yet to be developed, can also be used to contrast the performance of different product families for potential use in the switched capacitor DAS. The procedures are especially valuable for selecting power-switched components because manufacturers do not always provide sufficient specifications of transient behavior to choose the best component possible.

DAC/ADC test procedures -- Finally, analog-digital converter test procedures were developed by Doerfler to quantitatively measure the performance of the RDB DAS itself and to verify the quality of the DAC used within the DAS. This type of data is essential to any design process. These procedures test both static and dynamic performance of DACs and ADCs. Doerfler documented these procedures and wrote most of the relevant software.[4]

Major Error Sources of the RDB DAS

There are a few problems with RDB DAS that contributed to its linearity error. The system's major error sources include polarity range mismatch, track-and-hold droop, and system noise.[1]

Polarity range mismatch -- Polarity range mismatch is largely a result of the ADC's sign-magnitude configuration. As explained below, this configuration is especially troublesome for high resolution DASs.

> The biggest problem with this configuration is that the ADC inherently posesses two ranges which must be closely matched. Making the ranges match is a complicated task for two reasons. The first reason is that the two ranges are generated by different circuitry. The second reason involves the ADC's internal DAC. The transition region between the DAC input codes 00...00 and 00..01 is a likely place for a healthy differential linearity error because the output impedance of the DAC changes from an ideally infinite value to a finite value. Since this transition region is used in both ranges, it occurs on both sides of (and adjacent to) the desired matching point of the two ranges. Also, since any error that is created in the ADC's transfer characteristic by the DAC's differential linearity error at the 00...00 input code occurs in the middle of the bipolar input range, it will more frequently affect the determination of a digital representation of the analog input.1

Track-and-hold droop -- Track-and-hold droop, caused the input bias current of the track-and-hold output buffer, contributed to the RDB DAS' offset and linearity errors. Linearity error, which is more critical than offset error, is caused by droop during the successive

approximation routine.[1]

System noise -- Because it is difficult to collect quantitative noise data that can be used to diagnose a system's specific problem area, reducing system noise is largely constrained to trial-and-error methods. But, it is known that system noise is largely a function of component layout and power supply filtering. One cost associated with power switching components is increased noise at the supply terminals of those components. Power supply switches induce noise by increasing the source resistance seen by a device's supply terminals (due to the on-resistance of the switch), but impede attempts to filter that noise because supply filters cannot be located directly on that device's supply terminals. Reducing noise on the comparator's supply lines is especially important because of the comparator's effect on the overall performance of the ADC. In the RDB DAS the power-switched comparator was suspected to have problems rejecting power supply noise.

Introduction to a Second Generation Low-Power DAS

Design Requirements

The design goals for the switched-capacitor DAS are to generate an enhanced version of the RDB DAS.

Specifically, these are

- bipolar input voltage range: [-5,+5] V
- number of analog input channels: 2
- resolution: 15-bit
- maximum differential linearity error: ±1/2 LSB
- maximum integral linearity error: ±1 LSB
- input bandwidth: 200 Hz
- maximum conversion rate per channel: 500 Hz
- control: microprocessor based
- maximum power consumption (total system): 50-mW
- maximum printed circuit board area: one 3"x5" board
- fabrication requirements: easily reproducible with commercially available components

The enhancements over the requirements of the RDB DAS include (1) a reduction of board space, (2) a greater sampling rate, (3) higher input bandwidth, and (4) reduced average power consumption.

Method of Conversion

A simplified block diagram of a one-channel version of the switched-capacitor DAS appears in Figure 1.2. The input voltage is acquired and held in the normal manner by the switched-capacitor S/H. The S/H's estimate is equivalent to determining the first few bits of the successive approximation conversion. For the switched-capacitor DAS,

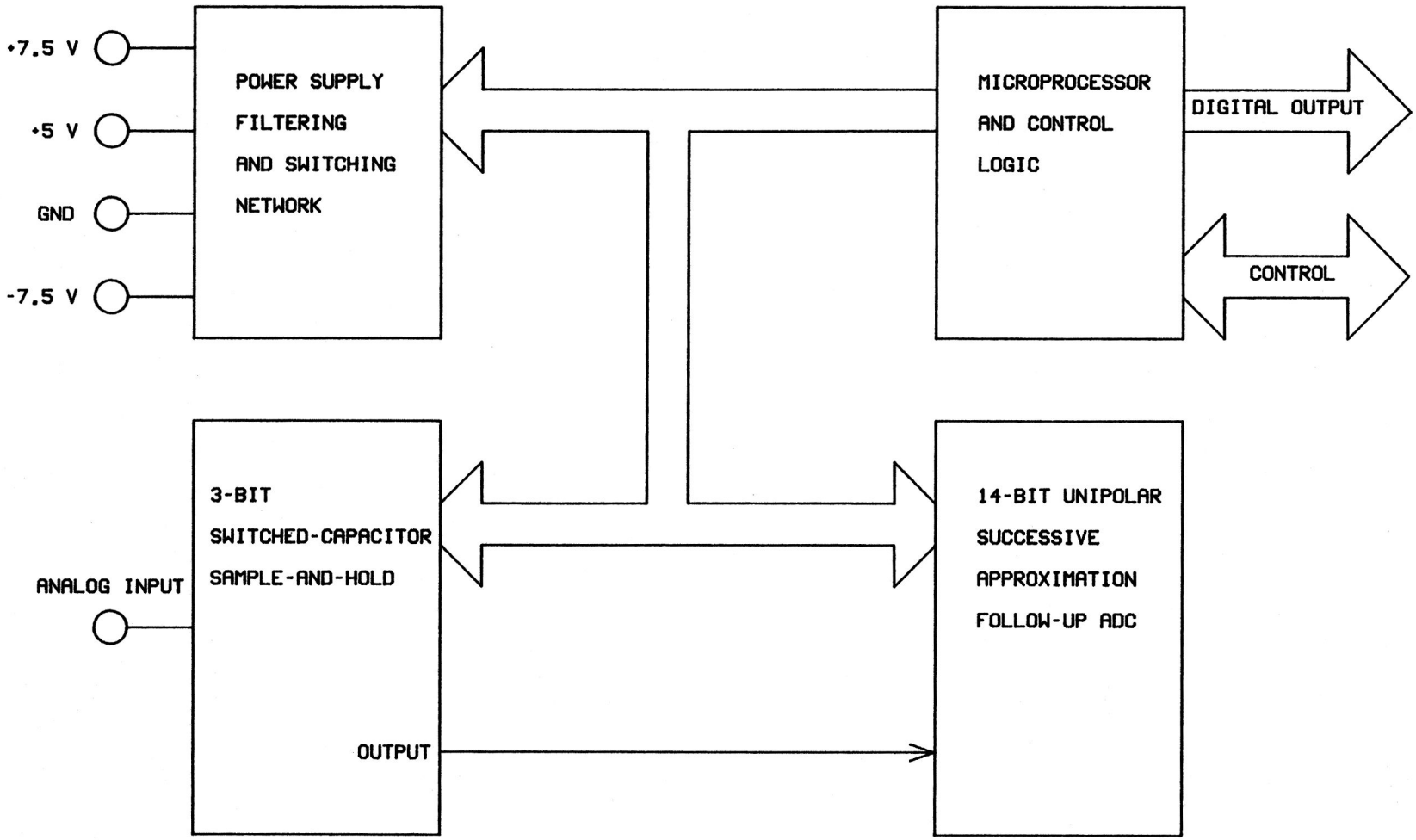


Figure 1.2 Block Diagram of the Switched-Capacitor DAS

the resolution of the estimate is nearly three bits. At the end of this preliminary conversion, the residual output voltage of the switched-capacitor S/H is unipolar (negative) and equal to the difference between the original input and the preliminary estimate of that input. The residual voltage is digitized by the follow-up ADC, sent to the microcomputer, and combined with the S/H's preliminary estimate. The result is processed by the microcomputer and passed to the DAS host.

One advantage afforded to the follow-up ADC by the switched-capacitor S/H is a reduced range of input voltages. Because its range of output voltages can be smaller, the follow-up DAC needs fewer bits of resolution than the overall DAS. For example, the LSB size of a 14-bit DAC with a 10-V output range is 610 μV. If the output range is reduced to 2.5 V, only 12 bits of resolution is needed to obtain the same size LSB. A second important advantage is the elimination of the causes of polarity range mismatch--the DAC does not need to be bipolar.

Similarities of the Two Data Acquisition Systems

The switched-capacitor DAS is really a second generation version of the RDB DAS. Because the design requirements and application for the two systems are similar, and because the RDB DAS was largely successful,

the two designs are also (purposely) similar. The major similarities are enumerated below:

- The switched-capacitor DAS also uses power-switching to reduce its average power consumption.
- The switched-capacitor DAS uses an onboard microprocessor to execute correction algorithms which are absolutely necessary to achieve 15-bit linearity. The switched-capacitor design does use a different microprocessor though--the Motorola MC68HC11A8; this is a low-power single-chip microcomputer which has on-chip memory (1/4 K RAM, 8 K ROM, and 1/2 K EEPROM) and extensive I/O capabilities.
- The ADC circuit for the switched-capacitor DAS is exactly the same as for the RDB DAS with the exception that the DAC is not configured for bipolar operation. The same 14-bit, monolithic, CMOS, current-output DAC (Datel-Intersil DAC-HA14BR) is used because of well known characteristics.[4]
- The PMI CMP-04 Low-Power Quad Voltage Comparator is used in both DASs because of its low power consumption, high gain, and high common mode rejection ratio. In the switched-

capacitor system, a discrete JFET front-end has been added to increase input impedance, and thereby save power by eliminating the need for a S/H output buffer.

Additional Considerations Resulting From Enhanced Design Requirements

The enhanced specifications of the switched-capacitor DAS impose constraints on the design which require considerations beyond those required to design the RDB DAS. The considerations needed to overcome these constraints are summarized below:

Reduction of board space -- The RDB DAS has separate analog and digital boards (each approximately 3"x5" in size). To reduce this area by a factor of two, the switched-capacitor design must either reduce the number of components required, pack the circuit layout more tightly, or do both. Because packing the layout aggravates noise problems by placing analog and digital components in close proximity, it is preferable to reduce the number of components.

Higher sampling rate -- The sampling rate for the switched-capacitor DAS is to be almost four times that of the RDB DAS. Therefore, components of the switched-capacitor DAS will consume power for a longer period

during a conversion. To reduce power consumption further, it is necessary to either reduce the number of components required or find components consuming less power with the same or better performance levels.

Higher input bandwidth -- The bandwidth of either DAS is limited by the input buffer's ability to acquire the input signal within a limited amount of time. The RDB DAS uses a non-power-switched, low slew-rate, low-power operational amplifier to perform this function adequately for an input bandwidth of 45 Hz. However, this type of amplifier may not be adequate for a 200 Hz bandwidth; so the tradeoff between a track-and-hold amplifier and a S/H amplifier must be examined closely.

Reduced average power consumption -- This requirement simply compounds the problem already presented by increases in sampling rate and input bandwidth.

CHAPTER 2. A SWITCHED-CAPACITOR SAMPLE-AND-HOLD

An Ideal Switched-Capacitor Sample-and-Hold

The switched-capacitor S/H is, in part, a discrete component version of a monolithic, 10-bit ADC reported by McCreary and Gray.[5] The switched-capacitor circuit used in this converter was later reported to have been used successfully to construct a 15-bit, monolithic, CMOS ADC with a 10-kHz conversion rate and slightly more than 20-mW power consumption.[9 10] This converter meets all the desired specifications for the switched-capacitor DAS, but unfortunately, it is not known to be commercially available. In effect, the switched-capacitor S/H is a low-resolution ADC with an intrinsic S/H. It is easiest to begin by describing its ideal operation and then proceed by tackling the practical problems of implementing it for use in the DAS.

Circuit Description

A simplified schematic of a 3-bit switched-capacitor S/H appears in Figure 2.1. The circuit consists of an array of capacitors and switches, and a high input impedance comparator. Each capacitor is one-half the size of the capacitor to its left, except for the last capacitor, C_0, which is equal to C_0. The total

capacitance is C_T. The lower plate of each capacitor, except C_0', can be connected either to the reference voltage V_{REF}, to the input voltage V_{IN}, or to ground.

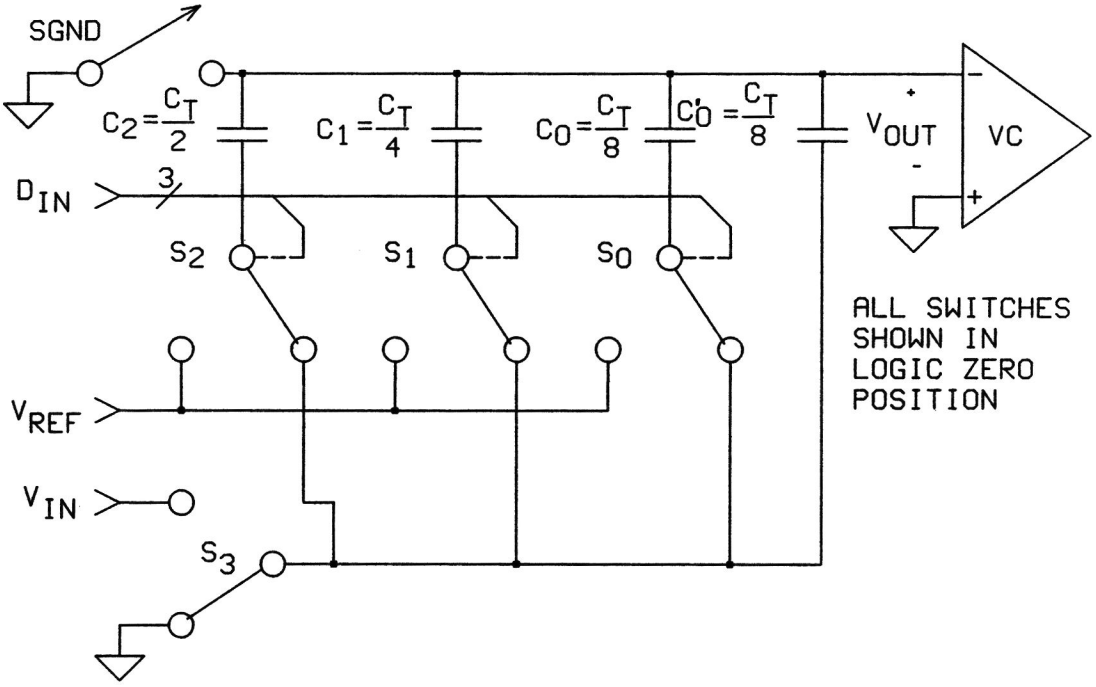


Figure 2.1 Ideal Three-Bit Switched-Capacitor Sample-and-Hold

The input voltage is sampled by acquiring a charge on the top plate of the array that is linearly related to the input voltage. This is done by grounding the top plate and connecting all the lower plates to V_{IN}. After the array is fully charged, switch SGND is opened and the

lower plate of each capacitor is returned to ground. This action conserves the net charge acquired on the top plate.

The analog output of the S/H is taken from the top plate and fed into the inverting input of the voltage comparator. The output voltage is a function of the net charge Q_X residing on the top plate of the array and the positions of switches S_0 through S_2, which are set according to the three bits of the digital control input $D_{IN} = b_2b_1b_0$ (bit b_i controls switch S_i where i=0,1, or 2). The output is

$$V_{OUT} = \sum_{i=0}^{2} \frac{b_i C_i}{C_T} + \frac{Q_X}{C_T} \qquad (2.1)$$

To derive this formula, it is helpful to notice that the parallel combination of the capacitors with lower plate connected to V_{REF} form the upper leg of a capacitive voltage divider; the remaining capacitors form the lower leg.

In the ideal case, where

$$\frac{C_i}{C_T} = 2^{(i-3)}; \quad i = 0, 1, 2 \qquad (2.2)$$

Equation 2.1 reduces to

$$V_{OUT} = V_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} + Q_X/C_T \qquad (2.3)$$

Equation 2.1 is illustrated by Figure 2.2. The ideal switched-capacitor S/H's transfer characteristic is

perfectly linear with uniform steps. A net charge on the top plate of the capacitor array shifts the characteristic as shown by the broken line in Figure 2.2. This shift is

$$V_S = Q_X/C_T \tag{2.4}$$

Unipolar Operation

The S/H shown in Figure 2.1 can be used as a three-bit unipolar ADC. After the input is sampled according to the procedure just described, the net charge on the top plate is

$$Q_X = -V_{IN}C_T \tag{2.5}$$

which causes the transfer characteristic to shift by

$$V_S = -V_{IN} \tag{2.6}$$

A successive approximation search for the digital control input (D_{IN}) that returns the analog output to the threshold potential of the comparator (ground) can be performed to obtain a digital representation of the input.

The successive approximation routine begins by testing for the value of the most significant bit (MSB), b_2. To do this, the control sets $D_{IN} = 100$ causing the output to be

$$V_{OUT} = -V_{IN} + V_{REF}/2 \tag{2.7}$$

Bit b_2 is a logic '1' if $V_{OUT} < 0$ or $V_{IN} > V_{REF}/2$. The comparator makes this decision. Switch S_2 is returned to ground, if the bit is a logic '0'.

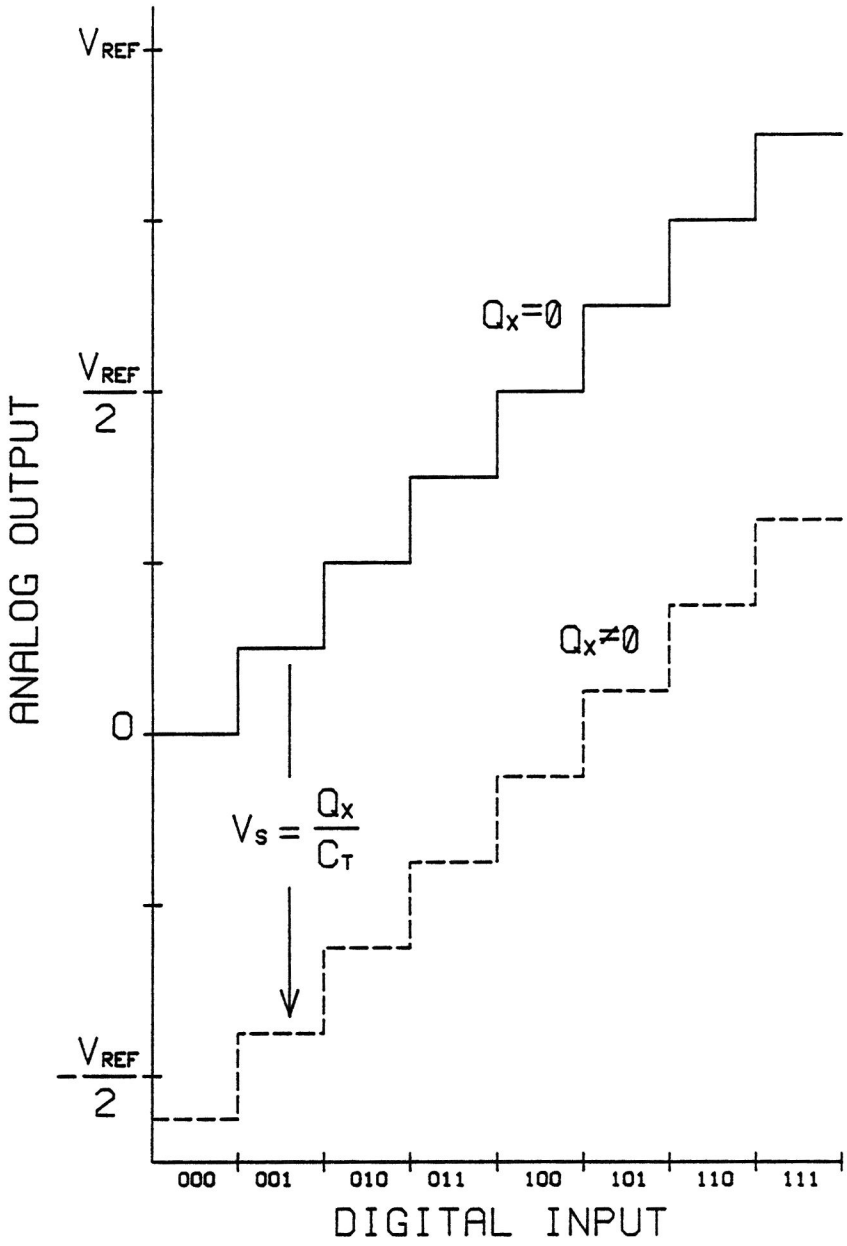


Figure 2.2 Ideal Transfer Characteristic

Successive bits are tested in a similar fashion. As the routine proceeds, the output converges toward ground from below in successively smaller steps, going positive only momentarily during the test of a bit which results in a logic '0'. The residual output voltage (V_{RES}) is

$$V_{RES} = V_{OUT} = -V_{IN} + V_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \qquad (2.8)$$

The procedure ensures that the residual output voltage is negative but within one step of ground. The input can be estimated by assuming $V_{RES} = 0$ and solving Equation 2.8 for V_{IN}:

$$\hat{V}_{IN} = V_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \qquad (2.9)$$

The error in the estimate is equal to the residual output voltage; that is,

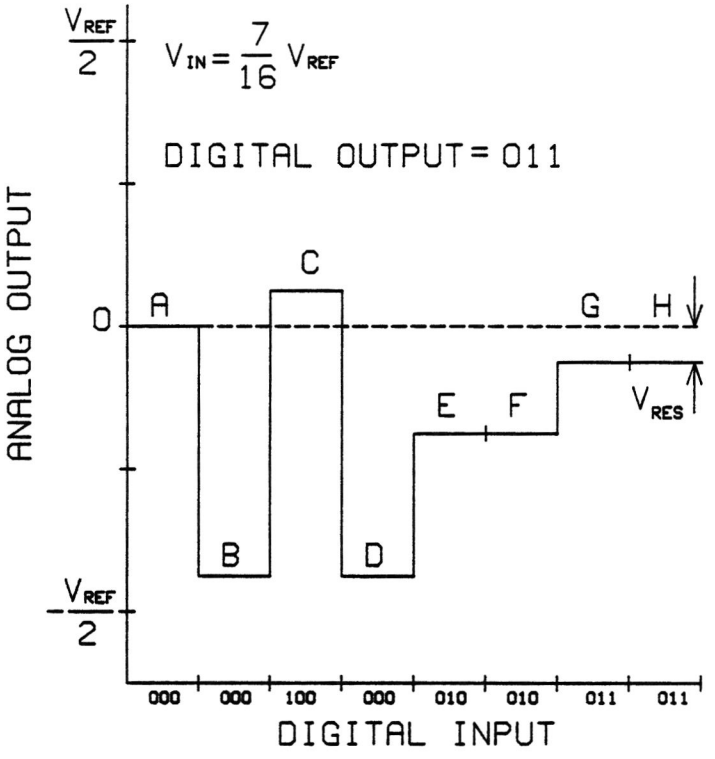
$$V_{RES} = \hat{V}_{IN} - V_{IN} \qquad (2.10)$$

The S/H's digital output ($\hat{D}_{IN}$), equal to the digital control input (D_{IN}) at the end of the successive approximation routine, is the digital representation of the binary fraction $\hat{V}_{IN}/V_{REF}$ (see Ref. 11, p. 171).

A plot of V_{OUT} for a hypothetical input $V_{IN} = (7/16)V_{REF}$ appears in Figure 2.3. The result of the conversion is $\hat{D}_{IN} = 011$ or $\hat{V}_{IN} = (3/8)V_{REF}$.

Bipolar Operation

There are several methods available to make the S/H bipolar. Most of them change the shift in the S/H's transfer characteristic. Two of these are the single-reference method and the dual-reference method.



A. Acquire charge Qx by closing switch SGND and connecting all lower plates to VIN.

B. Conserve charge Qx on the array top plate by opening SGND and grounding all lower plates. VOUT = -VIN.

C. Begin successive approximation search. Test MSB by connecting lower plate of C_2 to VREF.

D. MSB test fails. Return lower plate of C_2 to GND.

E. Test bit b_1 by connecting capacitor C_1 to VREF. VOUT = -VIN + VREF/4.

F. Bit-test b_1 passes. Leave capacitor C_1 connected to VREF.

G. Test bit b_0 by connecting capacitor C_0 to VREF.

H. Bit-test b_0 passes. Leave capacitor C_0 connected to VREF. VRES = VREF/16.

Figure 2.3 Plot of S/H Output During a Conversion

Single-reference method -- A method devised by McCreary and Gray[5] uses the same circuit as the unipolar switched-capacitor S/H to convert bipolar inputs in the range $[-V_{REF},+V_{REF}]$. Only a slight modification in control logic is required.

The modification is to set the MSB of D_{IN} to a logic '1' rather than a logic '0' to acquire the charge

$$Q_X = -C_T(V_{REF}/2 + V_{IN}/2) \tag{2.11}$$

The shift in the transfer characteristic can be calculated by substituting Equation 2.11 into Equation 2.4.

$$V_S = -(V_{REF}/2 + V_{IN}/2) \tag{2.12}$$

Once the charge is acquired, all capacitors are connected to ground as before, and the control proceeds as for unipolar conversions. The residual output voltage at the end of the successive approximation routine is

$$V_{RES} = -V_{IN}/2 - V_{REF}/2 + V_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \tag{2.13}$$

Again, the input estimate ($\hat{V}_{IN}$) is made by assuming V_{RES} = 0 and solving Equation 2.13 for the input.

$$\hat{V}_{IN} = -V_{REF} + 2V_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \tag{2.14}$$

As before, the error in the estimate is equal to the residual output voltage.

The digital output ($\hat{D}_{IN}$) is coded in offset binary.

Comparing Equations 2.12 and 2.6 clarifies the effect

of the control modification: the input is shifted $V_{REF}/2$ and scaled by 1/2.

Dual-reference method -- Practical considerations motivate the dual-reference method of making the switched-capacitor S/H bipolar. The noise levels for the DAS may be too large to tolerate this reduction. (For the switched-capacitor DAS, the size of an LSB is 305 μV.) The slightly more complex dual reference switched-capacitor S/H does not suffer from this problem (see Figure 2.4).

This method requires a second reference. The individual reference voltages are unimportant, but the difference between them is significant. The voltage difference must equal the magnitude of the desired input range. For example, the bipolar input range $[-dV_{REF}/2, +dV_{REF}/2]$ requires two references, $V_{REF}^{(1)}$ and $V_{REF}^{(2)}$, of any values such that

$$dV_{REF} = V_{REF}^{(1)} - V_{REF}^{(2)} \tag{2.15}$$

A few differences exist between this circuit and the unipolar S/H shown in Figure 2.1. First, the switch, SGND, formerly connecting the top plate to ground is renamed S_2, is now used to connect the top plate to the input. Second, switches S_0-S_2 connect to one of the two references; they cannot be connected to ground. Finally, the last capacitor C_0' connects to $V_{REF}^{(2)}$.

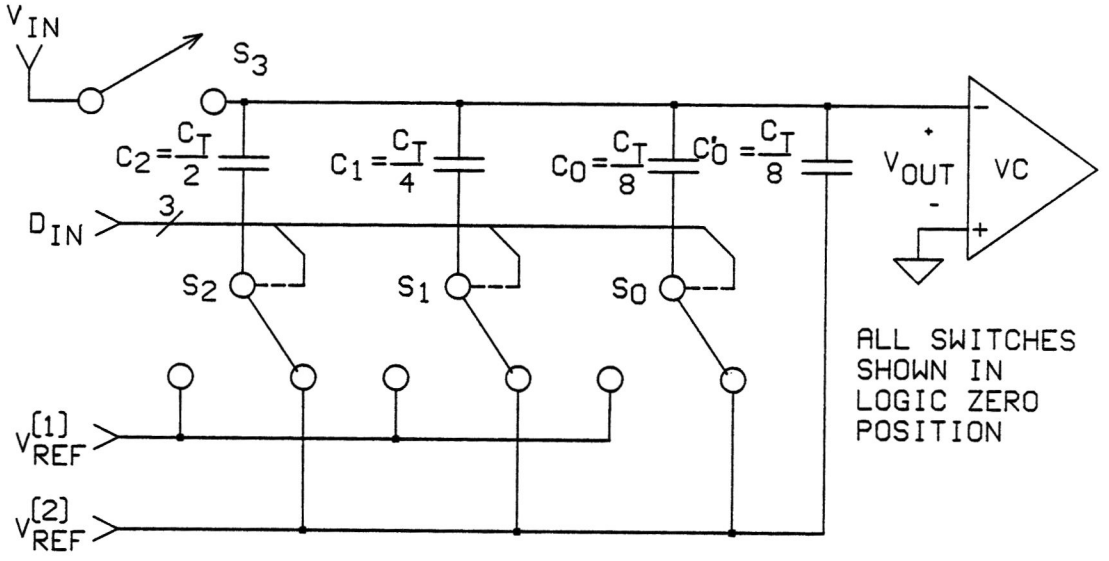


Figure 2.4 Dual-Reference Switched-Capacitor S/H

The control sequence is unchanged from McCreary and Gray's single reference method.[5] The net charge acquired by the top plate is

$$Q_X = C_T\left(\frac{V_{IN} - V_{REF}^{(1)}}{2} + \frac{V_{IN} - V_{REF}^{(2)}}{2}\right) \tag{2.16}$$

$$= C_T\left(V_{IN} - \frac{V_{REF}^{(1)} + V_{REF}^{(2)}}{2}\right) \tag{2.17}$$

Because the lower plates are not connected to ground, the characteristic shift depends on $V_{REF}^{(2)}$ as well as the charge Q_X:

$$V_S = V_{REF}^{(2)} + Q_X/C_T$$

$$= V_{REF}^{(2)} + V_{IN} - (V_{REF}^{(1)} + V_{REF}^{(2)})/2 \qquad (2.18)$$

$$= V_{IN} - \frac{dV_{REF}}{2}$$

The residual output voltage left after the successive approximation routine is

$$V_{RES} = V_{IN} - dV_{REF}/2 + dV_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \qquad (2.19)$$

Again, the input is estimated by assuming V_{RES} is zero and solving Equation 2.19 for the input.

$$\hat{V}_{IN} = dV_{REF}/2 - dV_{REF} \sum_{i=0}^{2} b_i 2^{(i-3)} \qquad (2.20)$$

Equations 2.18 to 2.12 and 2.6 reveal that the dual-reference circuit shifts the input voltage $-dV_{REF}/2$, but unlike the single-reference method, no scaling takes place. Herein, lies a possible advantage of the dual-reference switched-capacitor S/H gained at the cost of a slightly more complex circuit.

The switched-capacitor DAS uses this method for making the S/H bipolar. The single-reference method can be used only if testing indicates that the DAS' signal-to-noise ratio is high.

The Effects of Improper Capacitor Ratios

To this point, the author has indulged himself by assuming that it is possible to obtain capacitor ratios exactly equal to their nominal values (see Equation 2.2). Clearly, this is not possible, and the effects of capacitor ratio errors must be understood.

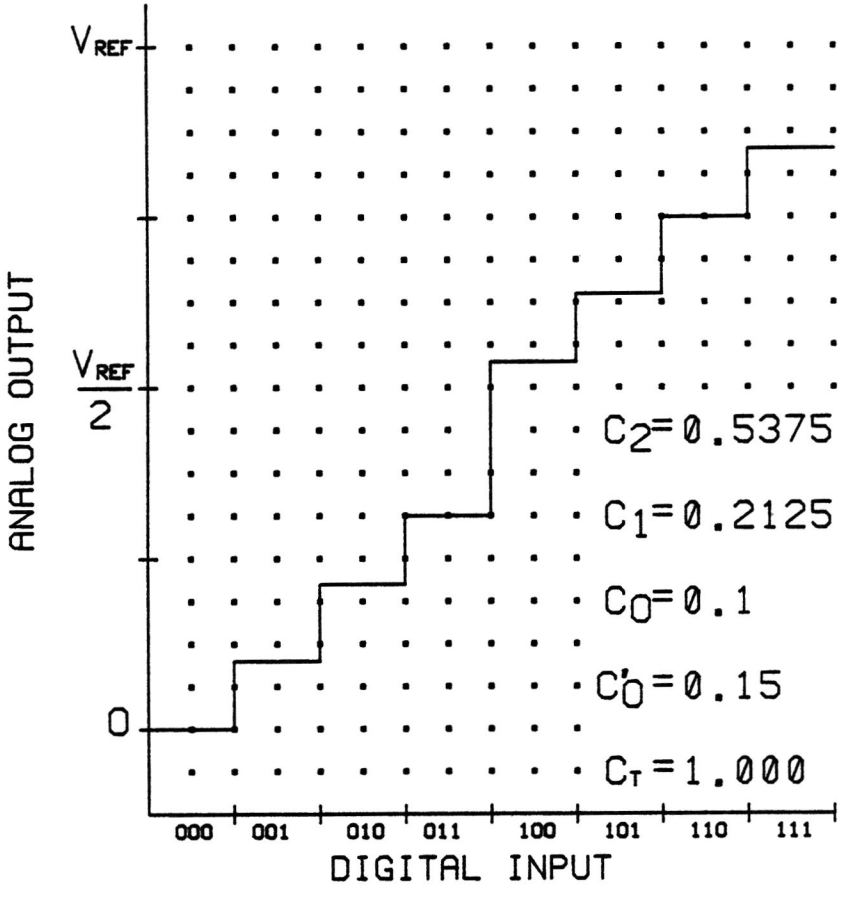


Figure 2.5 Characteristic of S/H With Improper Capacitor Ratios

When the ratio of each capacitor to the total capacitance is not a binary fraction--that is, an integer power of 1/2 (see Ref. 11, p. 171)--the steps of the transfer characteristic are not uniform as was shown in Figure 2.2. Rather, the transfer characteristic is distorted as indicated by the example shown in Figure 2.5. The resolution of a practical switched-capacitor S/H is not as fine as an ideal switched-capacitor S/H, because the practical transfer characteristic is nonlinear.

However, if the capacitor ratios are known by some means--either by direct measurement or by an indirect method--the transfer characteristic can be determined using Equation 2.1, repeated here.

$$V_{OUT} = \sum_{i=0}^{2} \frac{b_i C_i}{C_T} + \frac{Q_X}{C_T} \qquad (2.1)$$

The equations used to calculate the estimate of the input for the three types of S/H circuits can be derived from Equation 2.1 by not substituting the ideal capacitor ratios as was done to obtain Equation 2.3. The equations are

- unipolar switched-capacitor S/H

$$\hat{V}_{IN} = V_{REF} \sum_{i=0}^{2} b_i C_i / C_T \qquad (2.21)$$

- bipolar single-reference switched-capacitor S/H

$$\hat{V}_{IN} = - \frac{C_2}{(C_T - C_2)} V_{REF} + \frac{V_{ref}}{(C_T - C_2)} \sum_{i=0}^{2} b_i C_i \quad (2.22)$$

- bipolar dual-reference switched-capacitor S/H

$$\hat{V}_{IN} = dV_{REF}C_2/C_T - dV_{REF}/C_T \sum_{i=0}^{2} b_i C_i \quad (2.23)$$

The three unique terms of the appropriate equation must be stored in memory with the same resolution as the DAS itself (15 bits). (In practice, the terms must be stored with 16-bit resolution to overcome roundoff error.) The estimate of the input voltage is obtained by using the microcomputer to sum the terms according to Equation 2.22. Or, all possible sums could be precalculated. If this is done, the digital output of the S/H is more properly thought of as an address, rather than a digital estimate, that points to the appropriate sum. It is not unreasonable to consider forming a table of these sums for a low-resolution switched-capacitor S/H; for only few memory locations are needed.

The table could be generated and stored in memory at production, but drifts in the capacitor ratios after production would not be accounted for. The switched-capacitor DAS' self-calibration cycle, presented in Chapter 4, is used to build this table. Self-calibration

performed at regular intervals, eliminates errors due to drift in the capacitor ratios and the S/H's reference voltages.

A Switched-Capacitor S/H Implementation

The circuit diagram for a one-channel dual-reference switched-capacitor S/H minus control logic, power supply filters, and power supply switches appears in Figure 2.6. (The parts list is in Appendix B.) This section describes this implementation. The control logic, power supply filters, and power supply switches will be discussed in the next chapter.

Power Supplies

The analog power supply voltages for the circuit are $\pm$7.5 V. These voltages may be increased for improved performance at the cost of greater power consumption, but they may not be reduced because of the requirements of the dual reference circuit.

Dual-Reference Circuit

The two reference voltages are

$$V_{REF}^{(1)} = +5.0 \text{ V}$$
$$V_{REF}^{(2)} = -5.0 \text{ V}$$

Any other values will not work given the power supply voltages and the input voltage range. The circuit used to produce the two reference voltages must minimize the variation in their difference to minimize the frequency of calibration cycles. Therefore, it is not wise to use a 5.0-V reference with a unity-gain inverting operation amplifier, because of two problems. First, the inverter requires a matched pair of resistors that track well with temperature variations. Second, the temperature coefficient of the difference voltage (dV_{REF}) is double that of the reference, because any change in the reference output voltage produces an opposing, equal change in the output voltage of the inverter.

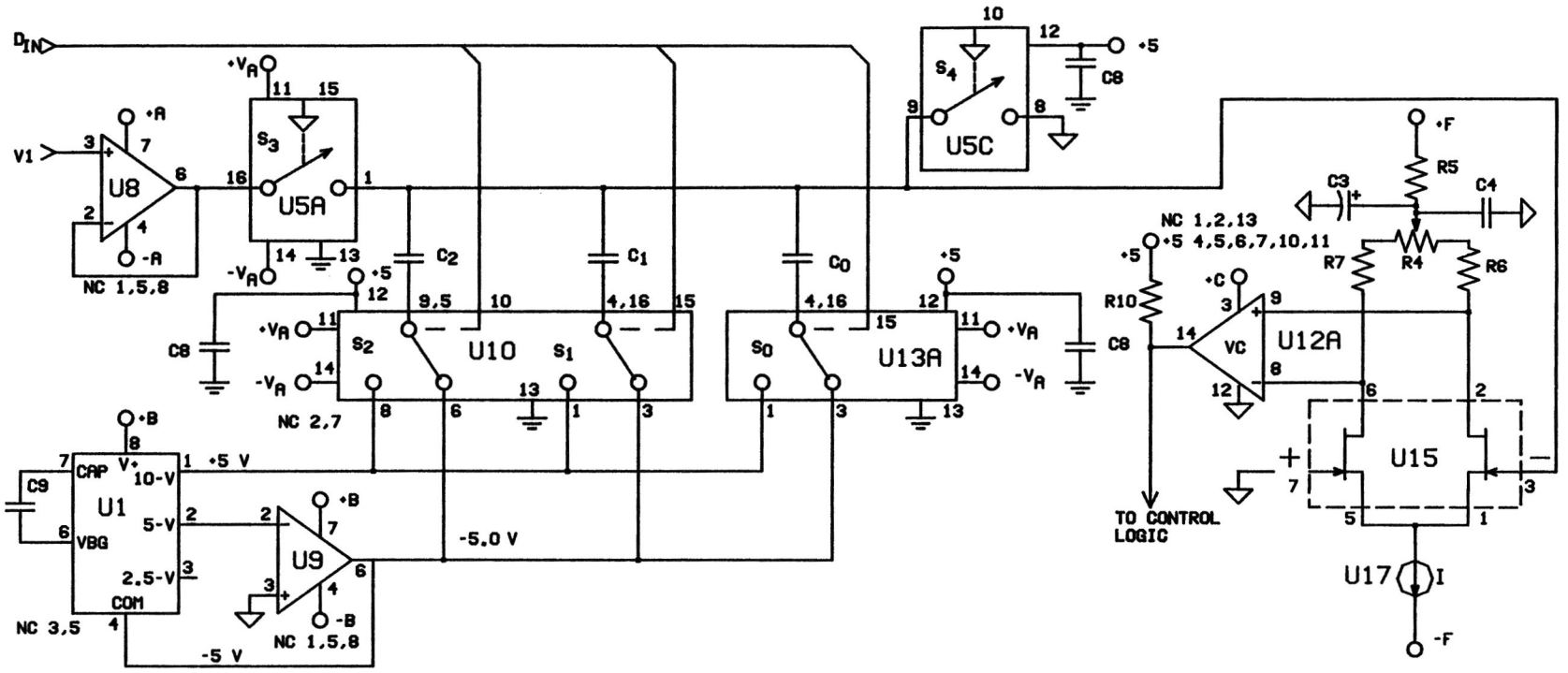
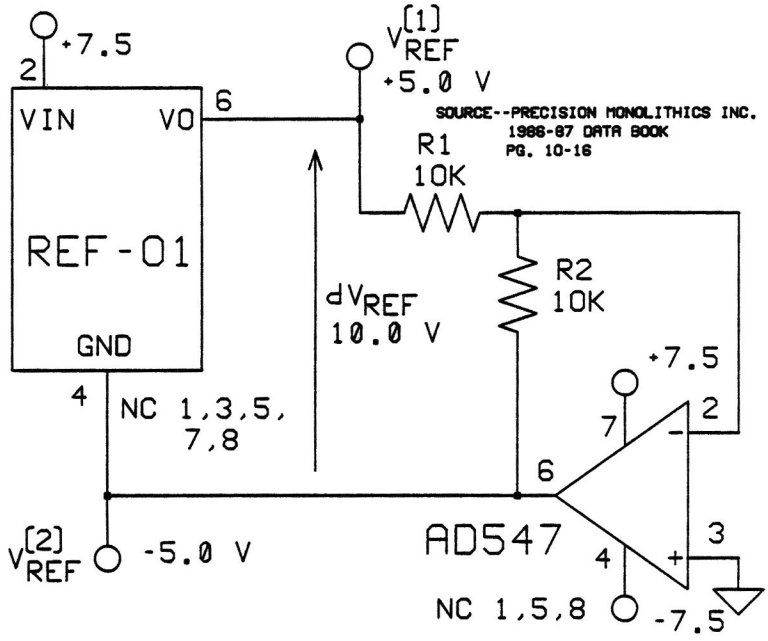


Figure 2.6 Circuit Diagram of a Switched-Capacitor Sample-and-Hold

Two similar circuits are available that avoid both of these problems. The first one is shown in Figure 2.7. The Precision Monolithics Inc. (PMI) REF-01 is a low power 10-V reference. The operational amplifier and resistors R1 and R2 force the GND pin of the reference to -5.0 V. In this circuit, the resistors R1 and R2 do not need to be closely matched, nor do they need to track closely over the operating temperature range. Reasonable operational amplifier offsets and offset drifts are also inconsequential because the difference dV_{REF} is solely dependent on the characteristics of the REF-01.



$$V_{REF}^{(1)} = \frac{R1}{R1 + R2}(dV_{REF}) \qquad V_{REF}^{(2)} = \frac{R2}{R1 + R2}(dV_{REF})$$

Figure 2.7 Dual-Reference Circuit Using Resistors

The second circuit (Figure 2.8) is the one used in the switched capacitor DAS. It uses the Analog Devices Pin-Programmable Voltage Reference and does not require any external resistors.[11] The circuit has essentially the same advantages as the first circuit, but it requires fewer components.

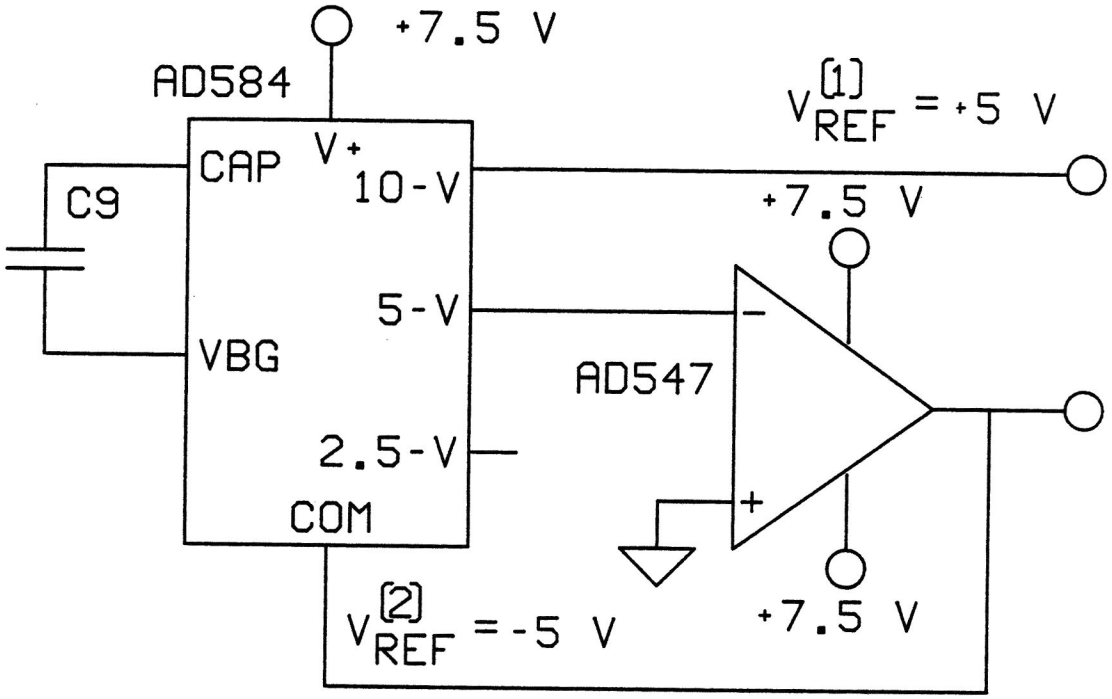


Figure 2.8 Dual-Reference Circuit Using AD584 Pin-Programmable Voltage Reference

Switches

CMOS analog switches are chosen mainly for their extremely low power consumption (less than 1.0 μW). The time constants for the switched capacitor array are proportional to the on-resistance of the switches, so this parameter should be minimized to achieve minimum input acquisition time and settling times so that the successive approximation search can proceed as quickly as possible.

Switch S_3 (see Figure 2.6) is selected in the same manner as any S/H amplifier switch.[3] Charge transferred by switch S_3 produces a sample-to-hold step, producing an offset error easily corrected by a microprocessor calibration cycle.

In contrast to switch S_3, switches S_0-S_2 do not transfer charge to the capacitor array, because the interelectrode capacitance of these switches is always charged by one of the references.

Capacitor Array

The last capacitor C_0' (see Figure 2.4) is deleted to save a small amount of board space. This omission is justified because it is done without cost--the only effect of omitting the last capacitor is to change the total array capacitance, and hence change the ratio of each of the other capacitor values to the total array capacitance. In any case, it is impossible (or at least impractical) to

build a capacitor array of discrete components with ideal ratios. Therefore, a method of correcting for improper capacitor ratios must be used whether the last capacitor is deleted or not.

If the other capacitors were equal to their ideal nominal values, where each capacitor is half the size of the capacitor to its left, the transfer characteristic would still be perfectly linear with uniform steps. But, because the capacitor ratios would now be

$$\frac{C_2}{C_T} = \frac{4}{7} \qquad \frac{C_1}{C_T} = \frac{2}{7} \qquad \frac{C_0}{C_T} = \frac{1}{7} \tag{2.24}$$

each step is one-seventh full scale rather than one-eight full scale.

To select a value for the total array capacitance and to select the type of capacitance dielectric material, the designer must proceed exactly as when choosing a S/H capacitor.[3] In this case, teflon capacitors are used, mainly because they exhibit low dielectric absorption.

The settling times of the S/H are partially set by the RC-time constants associated with the capacitors and the switch on-resistances. Other factors include the input buffer slew rate and settling time, and the maximum reference output currents. A rough calculation of the input acquisition time and settling time necessary for each bit is performed in Appendix A. The results of these calcu-

lations indicate a 30-μs acquisition time and a 20-μs settling time for each bit.

Comparator

The comparator must be able to resolve the polarity of a differential input voltage less than 1/2 LSB in magnitude (1/2 LSB for the switched capacitor DAS is 152.6 μV). To do this, the minimum required open-loop voltage gain is

$$A_{v(min)} = \frac{V_H - V_{OL}}{152.6\ \mu V} \tag{2.25}$$

where V_H = 3.5 V = CMOS logic '1' input threshold

V_{OL} = comparator negative supply rail

The PMI CMP-04 Quad Low-Power Precision Comparator has a specified $A_{v(min)}$ = 80 V/mV for a +15-V supply. To accept bipolar inputs the comparator must have a ±7.5-V supply. In this case, according to Equation 2.27, the required open-loop gain,

$$A_{v(min)} = 72\ V/mV \tag{2.26}$$

is just within the CMP-04's minimum specification.

A couple of problems occur if the CMP-04 is used alone. First, a level translator (such as the National Semiconductor MM74C904) is required so that the output range, -7.5 V to +5 V, is compatible with the DAS' control logic circuitry. (The control logic and microcomputer must be powered from a +5-V single supply.) Second, the

input bias current will cause excessive droop of the S/H's output voltage.

A high input impedance comparator can be built by adding a JFET differential to the front end of the CMP-04 (Figure 2.9).

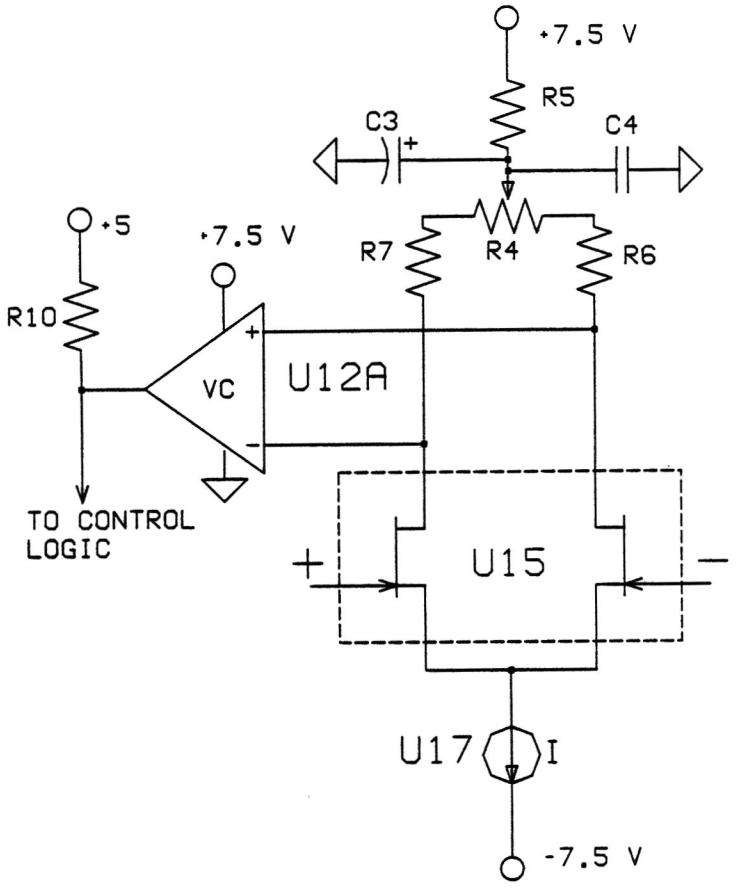


Figure 2.9 Voltage Comparator With JFET Differential Amplifier Front-End

The composite comparator possess the following advantages over the CMP-04 alone:

- The input bias current of the JFET differential amplifier is only several picoamperes.
- The CMP-04 output is directly compatible with the control logic--no level translator is required.
- The required open-loop gain is reduced as a result of the diminished output swing and the additional gain stage:

$$A_{v(min)} = \frac{(+5 - 0)\ V}{152.6\ \mu V} = 33\ V/mV \qquad (2.27)$$

- The power consumption is less than using another operational amplifier to buffer the S/H's output. This amplifier would consume a relatively large amount of power because it would have to have a high slew rate and a fast settling time to respond to the step changes of the S/H's output during the successive approximation search.

The differential amplifier circuit does not have to perform as well as one might think. First, amplification is not required (except as a margin of safety) because the gain of the CMP-04 alone is sufficient to resolve 1/2 LSB. Second, the transfer function of the differential amplifier does not need to be linear. The only requirement is that its output preserve the polarity of the input.

Minor attention does have to be paid to the matching characteristics of the two sides to keep the input offset voltage temperature coefficient small so that corrections will not be needed too frequently. However, the effects of the CMP-04's offsets are only small, because when they are referred to the input of the differential amplifier they are reduced by a factor equal to the gain of the amplifier.

Resistor R_5 is present to keep the CMP-04 common mode input voltage as near ground as possible. Capacitor C10 is used for power supply noise filtering.

The current source is the Siliconix CR022 Current Regulating Diode. This device is used to keep the differential amplifier bias current (approximately 0.210 mA) very nearly constant and to provide a very high impedance current source.

A quick test was run to check the performance of the composite comparator. The differential input was connected to the DC offset of a function generator and varied while monitoring the comparator output voltage on an oscilloscope. The comparator output was at one of the logic supply rails except when the input was in a very narrow band around the trip point. In this band the output was noisy, and its logic level indistinguishable. The width of this band, an indication of the comparator sensitivity, was found to be about 15 μV. The test

verified that the sensitivity of the composite comparator is sufficient to resolve 1/2 LSB (152 μV). Of course, the primary advantage of this circuit is low input bias current. One final note regarding the comparator: if the JFET differential amplifier is not power switched, and the comparator is power-switched, it is not necessary to disconnect the CMP-04 inputs. The CMP-04 can withstand input voltages which exceed the supply voltage by less than 30 V.

Input Buffer

Two major alternatives are (1) to operate the switched capacitor S/H as a S/H amplifier that acquires the input almost instantaneously, or (2) to operate it as a track-and-hold amplifier which acquires the input signal in a much longer period. Laboratory experimentation will be required to determine the optimal choice. As always, there are tradeoffs affecting the decision:

- The track-and-hold buffer. Because the track-and-hold amplifier does not have to be power-switched, it is potentially the simplest circuit.

  There are disadvantages, though. Because the input buffer is connected to the JFET differential amplifier input, it is necessary to continually power the differential

amplifier, offsetting the power consumption savings of the track-and-hold. Moreover, the higher sampling rate of the switched-capacitor DAS (500 Hz) may not allow enough time between conversions for the track-and-hold buffer to reacquire the input, precluding its use. This problem is compounded by the fact that self-calibration must be done between regular conversions to correct for component drifts.

- The sample-and-hold buffer. Operating the switched-capacitor S/H with a S/H type amplifier requires a much higher performance operational amplifier (such as the PMI OP-27). The power consumption of such an operational amplifier is much greater; consequently, it is necessary to operate it for a reduced duty cycle by turning it off during the hold-mode. The circuitry required to do this makes this circuit more complicated than the track-and-hold circuit.

The wire-wrapped test board includes a S/H type buffer. This type of amplifier is included for the simple reason that more board space and control logic is required to power switch it. Later, if a track-and-hold buffer

proves to be a better choice, it will be less difficult to remove a few components than to add them.

Adding a Second Input Channel

Basically, there will be two alternatives for adding a second input channel to the system. The first alternative is to add a slave S/H to the system. The switched-capacitor S/H and the slave S/H would acquire the two inputs simultaneously. Then, after completing the conversion of the input sampled by the switched-capacitor S/H, the output of the slave S/H would be sampled onto the switched-capacitor circuit. A second conversion is then performed. For this method, it is probably necessary to use a S/H type buffer for the switched-capacitor S/H because of the need to acquire the signal from the slave S/H so quickly.

The second method of adding another input channel is to duplicate all or part of the switched-capacitor S/H. Parts that may not need to be duplicated include the dual reference, the lower plate switches and the comparator. The residual voltages from the two S/Hs would need to be converted one after the other unless two follow-up ADCs are used. Duplicating components requires more board space than adding a slave S/H, but it may not consume as much power because an extra sample acquisition cycle is

not needed as for the slave S/H alternative. Another disadvantage is that a second calibration cycle would be needed to correct for the capacitor ratio errors of the second switched-capacitor S/H.

CHAPTER 3. IMPLEMENTATION OF THE SWITCHED-CAPACITOR DAS

The additional circuitry required to create the switched-capacitor DAS basically includes a follow-up DAC, the power supply filters, a power supply switching network, and a MC68HC11 microcomputer. The complete schematic is shown in Figures 3.1 and 3.2. (It is repeated in Appendix B where the parts list is also located.)

The Follow-up DAC

The follow-up DAC is used to perform a successive approximation analog-to-digital conversion of the S/H's residual output voltage. Fourteen bits of resolution are required. These fourteen bits are combined with the three bits determined by the S/H. In total, the microcomputer receives 17 bits of information with which it produces a 15-bit system output. The two extra bits of resolution are necessary to overcome the nonlinearity of the switched-capacitor S/H and roundoff error which manifests itself during microcomputer calculations.

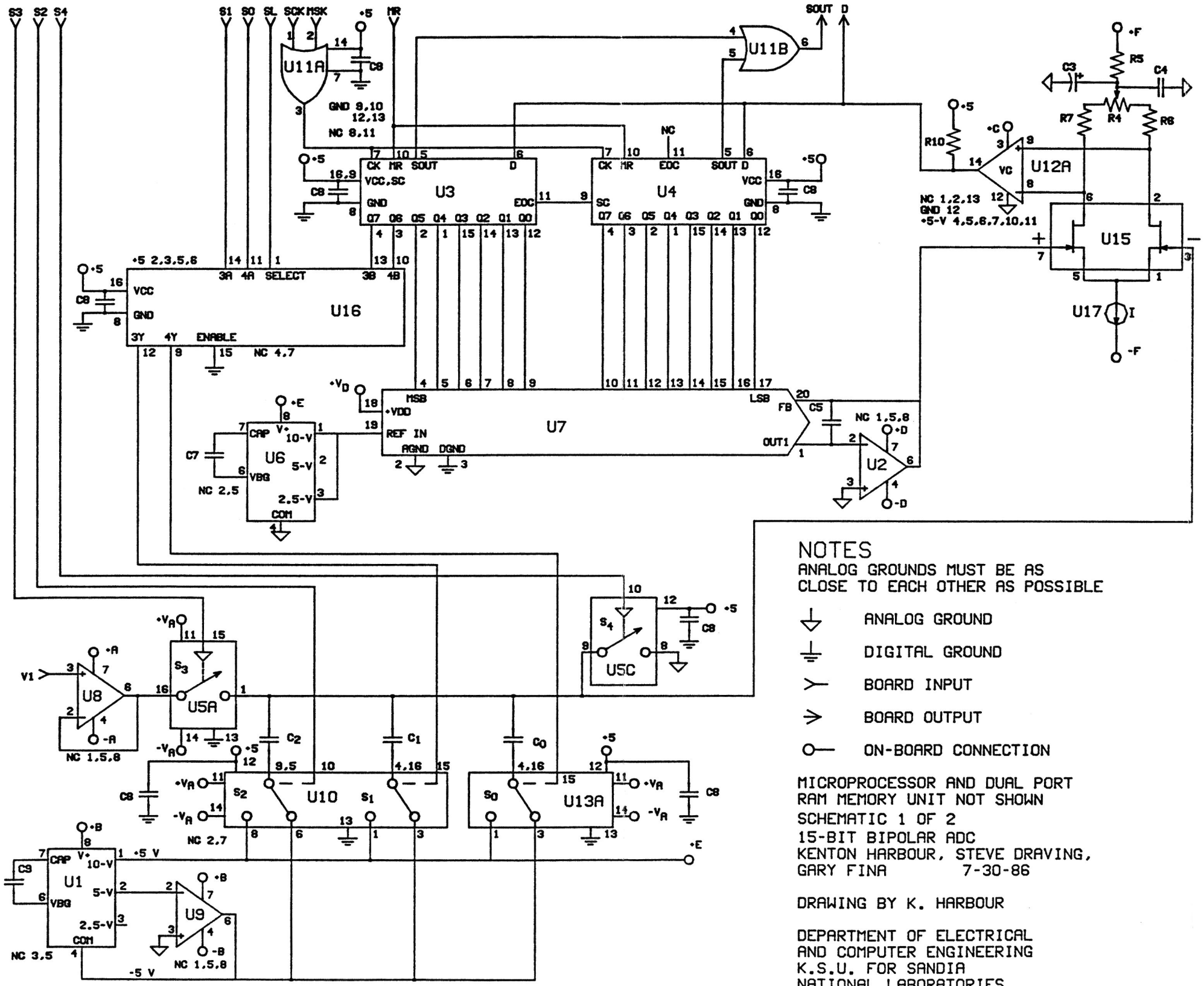


Figure 3.1 Circuit Diagram of Switched-Capacitor DAS (Schematic 1 of 2)

NOTES

ANALOG GROUNDS MUST BE AS CLOSE TO EACH OTHER AS POSSIBLE

- ANALOG GROUND
- DIGITAL GROUND
- BOARD INPUT
- BOARD OUTPUT
- ON-BOARD CONNECTION

MICROPROCESSOR AND DUAL PORT RAM MEMORY UNIT NOT SHOWN

SCHEMATIC 1 OF 2

15-BIT BIPOLAR ADC

KENTON HARBOUR, STEVE DRAVING, GARY FINA 7-30-86

DRAWING BY K. HARBOUR

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
K.S.U. FOR SANDIA NATIONAL LABORATORIES

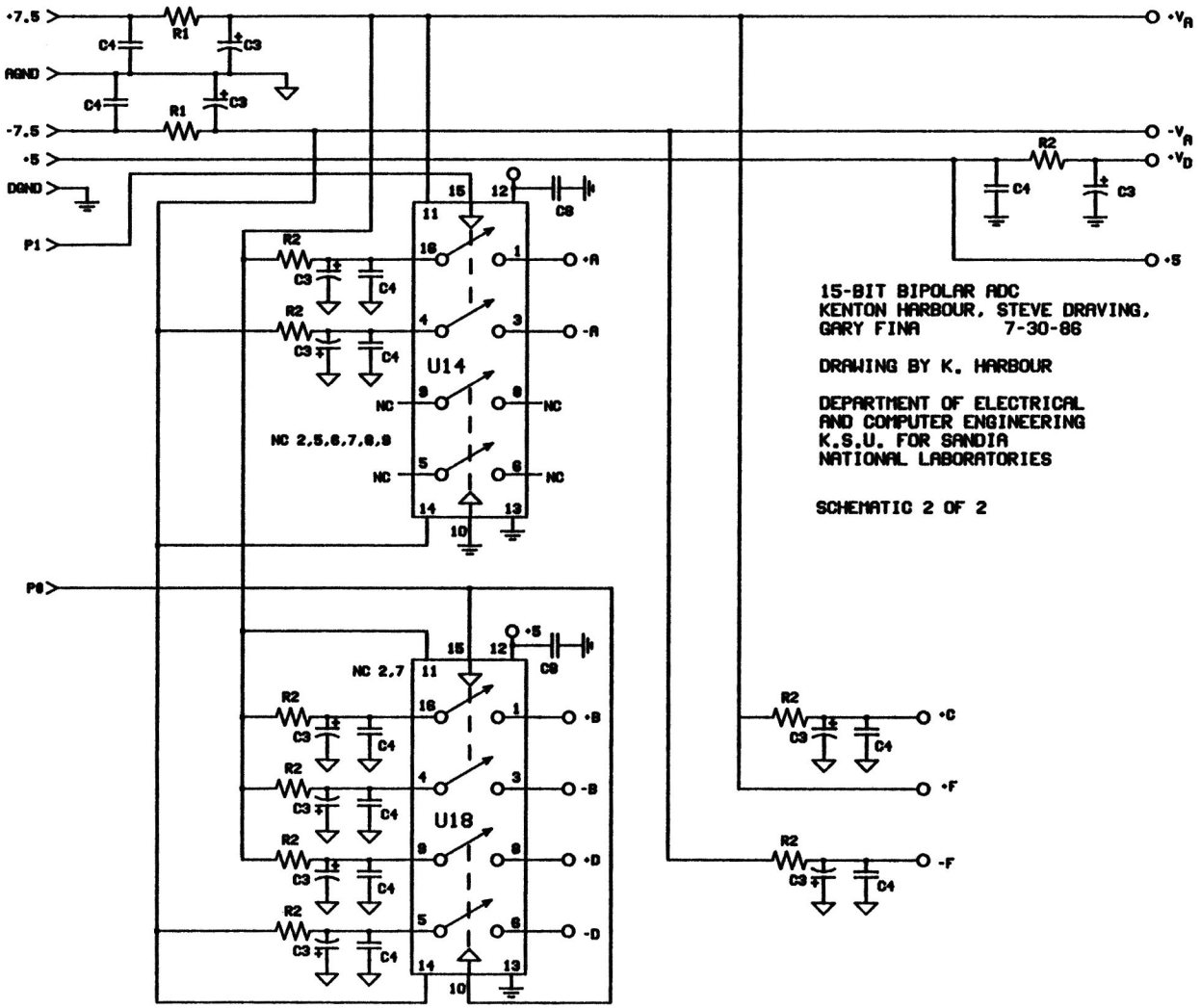


Figure 3.2 Circuit Diagram of Switched Capacitor DAS (Schematic 2 of 2)

The reference voltage for the follow-up DAC [$V_{REF}^{(3)}$] is chosen to be 2.5 V so that the size of the follow-up DAC's MSB is equal to the S/H's LSB is $dV_{REF}/8 = 1.25$ V. With this reference voltage, the DAC output voltage range is large enough to be used to determine any S/H residual voltage.

The specific DAC used is the Datel-Interstil DAC-HAl4B 14-bit, low power, monolithic, CMOS, current output DAC. The current output of the DAC is converted to a voltage using an operational amplifier as shown in the schematic (see device U2). The Precision Monolithics OP-37 is used despite the manufacturer's suggestion to use the OP-27 for closed-loop gains less than five. The OP-37 has a significantly higher slew rate, and a compensation technique to stabilize it for this application has been determined and tested;[2] only capacitor C5 is necessary to implement it.

The output of the DAC follower is connected to the noninverting input of the S/H's composite comparator. So then, the output of the follow-up DAC with input code 00..00 is the threshold voltage to which the S/H's output converges during the conversion.

Power Supply Filters

Power supply filters should be used so that power supply noise does not interfere with the analog signal lines. The filter configuration used is the same as in the RDB DAS (Figure 3.2).[2] The cutoff points of these filters should be adjusted to reject the operating frequency of the microcomputer. A two-pole low-pass filter appears between all analog components and the power supply. The first pole is common to all components, and the remaining pole is repeated for each component supply line.

Unfortunately, the power supply filters must be located on the supply side of the power supply switching network. A quick calculation shows that to do otherwise would result in a need for excessive amounts of power to charge the filter capacitors each time the power supply switch was closed. For example, if the last pole of the filter were placed on the component side of the supply switch, a capacitance of approximately 10 uF would need to be charged at least once per conversion (assuming the capacitor totally discharges each time). At a 500-Hz conversion rate the power consumed by the capacitor for a single supply line is

$$P_{cap} = \frac{1}{2}CV^2f$$
$$= \frac{1}{2}(10 \times 10^{-6})(7.5)^2(500) \qquad (3.2)$$

$$P_{cap} = 141 \text{ mW}$$

This figure nearly triples the power consumption allotted for the entire system.

A separate filter is not provided for the DAC 2.5-V reference (see Figures 3.1 and 3.2). Its supply pin is connected to the +5-V output of the dual reference circuit. This arrangement virtually eliminates the effects of the DAS' power supply noise. Two more advantages are (1) an extra switch is not needed to power switch the DAC reference, and (2) the power consumption of the DAC reference is slightly reduced. The load of the DAC 2.5-V reference on the dual reference circuit should not effect its performance, because it is a constant current load.

The second pole of the differential amplifier's filter is formed by capacitor C10 and resistor R5.

Power-Switching Network and Calculation of System Power Consumption

Before proceeding further it is useful to present a table which lists the calculated quiescent power consumption of the analog components used in the switched-capacitor DAS. The quiescent power consumption is calculated by multiplying the supply voltage by the manufacturers' worst case specifications of supply current.

Table 3.1

Quiescent Power Consumption of Components

Component	V^+(V)	V^-(V)	I^+_{sq}(mA)	I^-_{sq}(mA)	$P_{dq(max)}$(mW)
OP-27	+7.5	-7.5	+1.5	-1.5	45.0
CMP-04	+7.5	0.0	+1.0	---	7.5
AD584	+7.5	0.0	+1.0	---	7.5
DG5045	+7.5	-7.5	0.0	0.0	0.0*
DG5043	+7.5	-7.5	0.0	0.0	0.0*
DAC-HA14B					0.630**
AD547	+7.5	-7.5	+1.5	-1.5	22.5
Diff. Amp.	+7.5	-7.5	+0.2	-0.2	3.0
MC68HC11 (4 MHz; run mode)					35.0
MC68HC11 (wait mode)					14.0

Note: All values calculated using manufacturer's worst case specifications for ±7.5 V power supplies.

*The power consumption is directly related to frequency of operation. For frequencies below 2 kHz power consumption is negligible.

**The power consumption of the DAC alone is 0.005 mW. The additional amount is due to the current from the reference input through the DAC's internal reference.

For the switched-capacitor DAS, only one and one-half 16-pin packages and two microcomputer I/O lines are required to power switch all analog components, except the composite comparator, as shown in the schematic diagram (Figures 3.1 and 3.2). The composite comparator is not

power switched so that its power supply line noise can be minimized by avoiding some of the problems the RDB DAS encountered.

The CMOS switches (DG5043 and DG5045) consume less than one microwatt. A separate switch is used for all component supply lines except the dual reference circuit. In this case the reference and positive supply for the operational amplifier are switched in common.

The input buffer does not need an additional switch to disconnect the input. When power is turned off (during the hold mode), the output is also disconnected from the circuit. Consequently, there is no loop to allow input current to flow. The switch used to disconnect the supply lines is a double-pole single-throw (DPST) switch on the same CMOS substrate so that there is little chance that one supply line will be disconnected before the other supply line. A resistor could be placed in series with the analog input to limit any damaging transient currents.

All components, except the input buffer, are turned on for the duration of the conversion and then turned off until the next conversion needs to begin. The input buffer is turned on only long enough to acquire the input. The expected conversion time t_c is 350 μs, and the required conversion time T_c is 2000 μs (for a 500 Hz conversion rate). Consequently, the duty cycle of

operation is

$$t_c/T_c = 0.175 = 17.5\% \quad (3.1)$$

The input buffer is only turned on to sample the input. Its expected acquisition time is 30 us, therefore its duty cycle of operation is

$$t_c/T_c = 0.015 = 1.5\% \quad (3.2)$$

The continuous power consumption of each component is multiplied by its fractional duty cycle of operation to obtain its average power consumption. The total power consumption for the total one-channel system using power switching is shown in Table 3.2.

To extrapolate for the total average power consumption of a two channel system, it will be necessary to double the average power consumption of every component except the comparator and the microcomputer. It is expected that it will be necessary to either duplicate components or leave them on twice as long (to perform the two conversions serially). The microcomputer's power consumption will increase because it will be in the run mode twice as long. Extrapolating in this manner, the total average power consumption for a two channel system is expected to be 64 mW.

Table 3.2

Calculation of Average System Power Consumption (One Channel)

Component	Function	Continuous Pwr (mW)	"ON" Duty Cycle(%)	Avg. Pwr. (mW)
OP-27	Input Buffer	45.0	1.5	0.68
AD584	SCSH + Ref.	7.5	17.5	1.31
AD547	SCSH - Ref.	22.5	17.5	3.94
CMP-04	Comparator	7.5	100.0	7.50
	Diff. Amp.	3.0	100.0	3.00
AD584	DAC Ref.	7.5	17.5	1.31
DAC-HA14B	Follow-up DAC	0.63	17.5	0.11*
OP-27	DAC Follower	45.0	17.5	7.88
MC68HC11	Microprocessor (4 MHz; run mode)	35.0	22.5	7.88**
MC68HC11	Microprocessor (wait mode)	14.0	77.5	10.85
TOTALS		206.0 mW		44.4 mW

*Only 0.625 mW due to current through the DAC's internal resistance are power switched. This current is turned off as a result of power switching the DAC reference.

**The microprocessor has a low power wait mode which can be software activated. The microprocessor should be able to perform all calculations and control in 22.5 percent of the 2 ms conversion time.

Control Logic

Circuit Description

The MC68HC11 microcomputer dramatically reduces the number of chips required to control the switched-capacitor DAS. This is because it does not require external memory and I/O interfaces are provided on-chip.

Nevertheless, some control logic is required to limit the number of microcomputer I/O lines required and to reduce the microcomputer's power consumption by reducing its processing load--its power consumption is roughly proportional to its operating frequency.

The successive approximation searches for the S/H and follow-up DAC are controlled by successive approximation registers (SARs; devices U3 and U4); they proceed without interruption. The SARs connect directly to the DAC but share control of switches S_0 and S_1 with the microcomputer via a multiplexer (U16). Switch S_2 is set exclusively by the microcomputer. The SAR clock input can be controlled either by a serial clock (SCK) from a serial port, or by a manually toggled general purpose I/O line (MSK). The SARs feed their data into the serial port through OR gate U11B. The microcomputer may also observe the output of the comparator directly. The microcomputer is used to control the power switches via control lines P0 and P1, and switches S_3 and S_4. Output data may be passed to a host

system through a dual port RAM memory unit (not shown) chosen for its small package size. All together ten microcomputer output lines and two input lines are required.

Control Logic Operation

Control of the dual reference S/H has already been described in Chapter 2. The information given here is only supplemental.

To keep the output voltage of the S/H from above the negative power supply, the microcomputer controls switch S_2 rather than the SAR. If the this were not done, the S/H output would fall below the negative power supply for inputs near -5 V. The protection diode of switch S_3 would forward bias when the lower plate of capacitor C_2 were returned to -5 V at the beginning of the successive approximation search.

During a normal conversion, the multiplexer is set to give control of switches S_0 and S_1 to the SAR. Power is applied to all components simultaneously, but removed from the input buffer as soon as the input is acquired. After the conversion is finished, all components are turned off and the SARs are reset.

An Estimate of Required Board Space

Even though it is not possible to know at this time the exact amount of board space the circuit requires, it can be estimated by comparing the number of components required for the switched-capacitor DAS with the number of components required for the RDB DAS, which occupies two 3"x5" boards. The results of this comparison are summarized in Table 3.3.

Table 3.3

Number of Components Required To Build Each of Two DASs

Design	No. of IC's*	No. of IC Pins
Switched Cap.	19	312
RDB**	33	524

* excludes all discrete components, that is, resistors and capacitors

** information collected from Reference 1, Appendix A

This table implies the switched-capacitor DAS will require a slightly more than half the board space of the RDB DAS, unless it can be packed a little more tightly.

CHAPTER 4. AN ALGORITHM FOR SELF-CALIBRATION

In this chapter an algorithm to determine the transfer characteristic of the switched-capacitor S/H is outlined. Refer to DAS circuit diagram (Figure 3.1 and 3.2) during the following discussion.

There are several advantages to this algorithm that could not be obtained if the capacitor ratios were measured directly and then used to calculate the transfer characteristic according to Equation 2.1:

- No additional instrumentation is required. The information necessary to determine the transfer characteristic is obtained by the DAS alone.
- The DAS can be recalibrated as often as necessary to compensate for drifts in component values due to temperature variations, because the algorithm can be performed between regular conversions without interruption.
- Only one extra logic chip is required, namely, the multiplexer (U16).
- Special matching between the S/H's references and the DAC's reference is not required, because measurements are made only with respect to the DAC's reference voltage.

In the presence of capacitor ratio errors the S/H's estimate of the input voltage is described by Equation 2.24 (repeated here):

$$\hat{V}_{IN} = dV_{REF}/C_T(C_2 - \sum_{i=0}^{2} b_i C_i) \qquad (2.24)$$

The equation above contains three unique terms,

$$\frac{dV_{REF}\, C_i}{C_T} \qquad i = 0, 1, 2 \qquad (4.1)$$

which can be determined to the required resolution using the follow-up DAC. The method for doing this is an adaptation of an algorithm used to measure capacitor ratios in integrated circuit arrays.[6]

At least three conversions are required to determine the three difference voltages that can be used to calculate the terms in Equation 2.24. To perform these conversions it is simplest to give the microcomputer direct control of the switched capacitor S/H's lower plate switches; hence the need for the multiplexer. The difference voltages are

$$dV_0 = \frac{dV_{REF}\, C_0}{C_T} \qquad (4.2)$$

$$dV_1 = \frac{dV_{REF}}{C_T}(C_1 - C_0) \qquad (4.3)$$

$$dV_2 = \frac{dV_{REF}}{C_T}(C_2 - C_1) \qquad (4.4)$$

The difference voltage dV_n (where n=0,1,or 2) is obtained by connecting the lower plate of capacitor C_n to the positive reference, $V_{REF}^{(1)}$, closing switch S_4 momentarily to charge the array, and then reversing the position of switch S_n and all capacitor array switches to its right (if there are any). The positions of the array switches to the left of switch S_n are unimportant, but they must not change. The charge acquired in this manner shifts the S/H's transfer characteristic so that for D_{IN} = n, V_{OUT} = 0. After the array switches are reversed, the residual output voltage of the SCSH is

$$V_{RES} = - dV_n \tag{4.6}$$

A successive approximation search using the follow-up DAC can be used to digitize this value--just as for a normal conversion. The accuracy of the process could be improved by running several conversions and averaging the results. Using this information, the three terms listed in Equation 4.1 can be calculated by solving Equations 4.2 through 4.4 as follows:

$$dV_{REF} \frac{C_0}{C_T} = dV_0 \tag{4.7}$$

$$dV_{REF} \frac{C_1}{C_T} = dV_0 + dV_1 \tag{4.8}$$

$$dV_{REF} \frac{C_2}{C_T} = dV_0 + dV_1 + dV_2 \tag{4.8}$$

Roundoff error will affect the results of these summations; hence, the need for the extra bit of resolution.

In the preceeding derivation, the offset voltage of the composite comparator, V_{OFFSET}, has been neglected. In practice, this is not possible and switch S_4 must be included so that a null input can be sampled to digitize V_{OFFSET} using follow-up DAC. The offset measurement is used to adjust the measured voltages dV_0, dV_1, and dV_2.

Because the offset voltage of the input buffer is specified by the manufacturer to be less than 10 μV, the offset of the whole DAS should equal the offset of the comparator alone. Therefore, it is not necessary to provided a separate ground test switch at the DAS's input. Another advantage is the input buffer does not consume power during the calibration conversions.

It is useful to conclude this chapter by listing the self-calibration algorithm in an abbreviated form:

Self-Calibration Algorithm

- Set D_{IN} = 001
- Close and open S_4
- Measure V_{OFFSET}
- Set D_{IN} = 000
- Measure $-dV_0$

- Adjust measurement by V_{OFFSET}
- Store $C_0 dV_{ref}/C_T = dV_0$ in memory
- Set D_{IN} = 010
- Close and open S_4
- Set D_{IN} = 001
- Measure $-dV_1$
- Adjust measurement by V_{OFFSET}
- Store $C_1 dV_{REF}/C_T = dV_1 + dV_0$ in memory
- Set D_{IN} = 100
- Close and open S_4
- Set D_{IN} = 011
- Measure $-dV_2$
- Adjust measurement by V_{OFFSET}
- Store $C_2 dV_{REF}/C_T = dV_0 + d_1 + dV_2$ in memory

CONCLUSIONS

The preliminary design for the switched-capacitor DAS is complete. These studies indicate that it is possible to build a DAS with the following specifications:

- input voltage range: [-5,+5] V
- resolution: 15 bits
- maximum conversion rate: 500 Hz
- maximum integral linearity error: +1 LSB
- total system power consumption: 60 mW

The task, now, is to rigorously prove this claim by testing the one-channel circuit and then use the test results to modify the circuit as necessary to add a second channel. After this work is complete the circuit may be carefully laid out to determine the board space it requires.

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[12]Calculation by Steve Draving, Graduate Research Assistant, Kansas State University, July 15, 1986.

APPENDIX A. AN ESTIMATE OF INPUT ACQUISITION TIME AND SETTLING TIMES FOR THE SWITCHED CAPACITOR SAMPLE-AND-HOLD

Circuit Models And Step Responses

A rough approximation of the time required for the switched-capacitor S/H to be fully charged by the input and the time required to test each bit during the successive approximation routine was made by modeling the S/H with linear elements. Each closed switch is modeled as a simple resistor. Then, Hewlett Packard's "Linear Systems Analysis" software plotted the step response of the model using the its transfer function.

Figure A.1 is the circuit used to model the switched-capacitor S/H during the input acquisition phase. The unit step response is shown in Figure A.2.

A similar circuit, Figure A.3, is used to model the switched-capacitor circuit for the test of its MSB. The unit step response for this circuit is shown in Figure A.4.

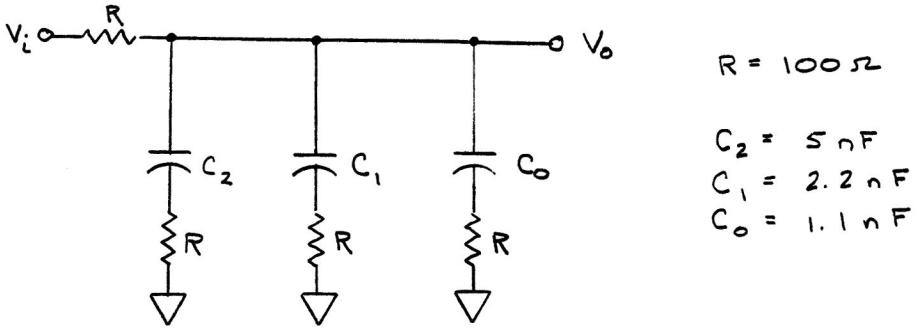


Figure A.1 Circuit Model for the Switched-Capacitor S/H Configured for Input Acquisition

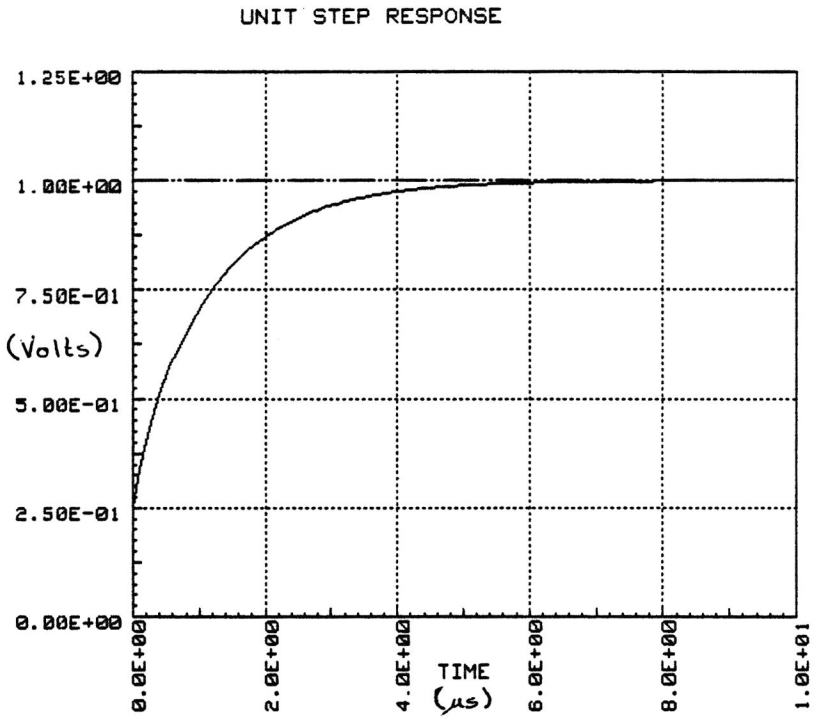


Figure A.2 Step Response For Input Acquisition Configuration

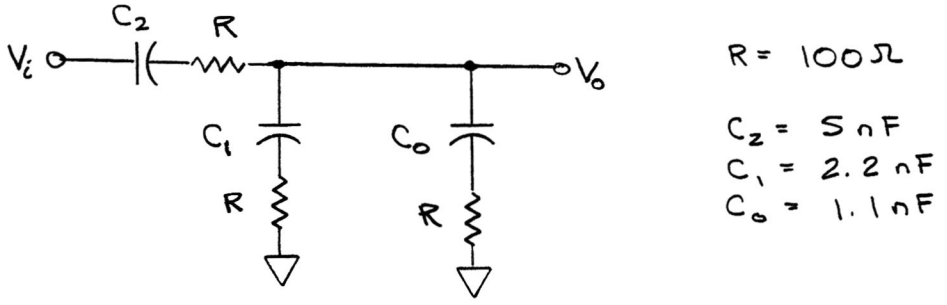


Figure A.3 Circuit Model for the Switched-Capacitor S/H Configured to Test the MSB

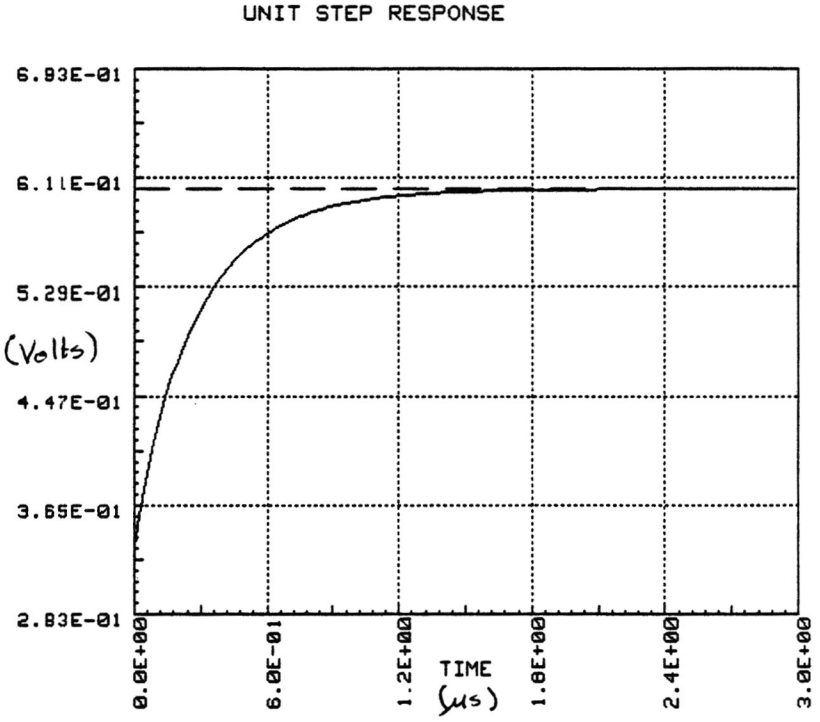


Figure A.4 Step Response for Switched-Capacitor S/H Configured to Test the MSB

The settling times required to test the last two bits of the S/H were not determined. Because the control logic allows the same settling time for all bits, only the required settling time for the MSB, the longest of the three, needs to be known.

Derivation of Transfer Functions

The transfer functions for the two circuits, Figures A.1 and A.3, are derived in this section.

First, consider the circuit in Figure A.1. Let Y_0, Y_1 and Y_2 be the admittance of the three legs.

$$Y_2 = (R + 1/sC_2)^{-1} = \frac{s/R}{s + 1/RC_2} \qquad (A.1)$$

$$Y_1 = (R + 1/sC_1)^{-1} = \frac{s/R}{s + 1/RC_1} \qquad (A.2)$$

$$Y_0 = (R + 1/sC_0)^{-1} = \frac{s/R}{s + 1/RC_0} \qquad (A.3)$$

Let Y_L be the admittance of the parallel combination of these three legs, and let $w_i = 1/RC_i$ (i=0, 1, or 2).

$$Y_L = Y_0 + Y_1 + Y_2 \qquad (A.4)$$

$$Y_L = \frac{s}{R}\left(\frac{1}{s + w_0} + \frac{1}{s + w_1} + \frac{1}{s + w_2}\right) \qquad (A.5)$$

$$Y_L = \frac{s}{R}\left[\frac{(s+w_1)(s+w_2) + (s+w_0)(s+w_2) + (s+w_0)(s+w_1)}{(s+w_0)(s+w_1)(s+w_2)}\right] \qquad (A.6)$$

Substitute this equation into the transfer function,

$$\frac{V_0(s)}{V_i(s)} = \frac{1/Y_L}{R + 1/Y_L} \tag{A.7}$$

First, form the sum in the denominator of Equation A.7.

$$R+\frac{1}{Y_L} = \frac{sR[(s+w_1)(s+w_2)+(s+w_0)(s+w_2)+(s+w_0)(s+w_1)]}{s[(s+w_1)(s+w_2)+(s+w_0)(s+w_2)+(s+w_0)(s+w_1)]} +$$

$$+ \frac{R(s+w_0)(s+w_1)(s+w_2)}{s[(s+w_1)(s+w_2)+(s+w_0)(s+w_2)+(s+w_0)(s+w_1)]} \tag{A.8}$$

The numerator of Equation A.7, after Equation A.8 and A.6 are inserted, is

$$N(s) = (s+w_0)(s+w_1)(s+w_2) \tag{A.9}$$

And the denominator is

$$D(s) = (s+w_0)(s+w_1)(s+w_2) + s(s+w_1)(s+w_2) +$$

$$+ s(s+w_0)(s+w_2) + s(s+w_0)(s+w_1) \tag{A.10}$$

To use the "Linear Systems Analysis" software, these polynomials must be expanded to

$$N(s) = N_3s^3 + N_2s^2 + N_1s + N_0 \tag{A.11}$$

and

$$D(s) = D_3s^3 + D_2s^2 + D_1s + D_0 \tag{A.12}$$

where

$$N_0 = w_0w_1w_2$$

$$N_1 = w_0w_1 + w_1w_2 + w_0w_2$$

$$N_2 = w_0 + w_1 + w_2$$

$$N_3 = 1$$

$$D_0 = w_0w_1w_2$$

$$D_1 = 2(w_0w_1 + w_1w_2 + w_0w_2)$$

$$D_2 = 3(w_0 + w_1 + w_2)$$

$$D_3 = 4$$

For the values of capacitors and resistors used

$$w_0 = 9.091 \times 10^6 \text{ sec}^{-1}$$

$$w_1 = 4.545 \times 10^6 \text{ sec}^{-1}$$

$$w_2 = 2.000 \times 10^6 \text{ sec}^{-1}$$

the coefficients evaluate to

$$N_0 = 8.264 \times 10^{19} \text{ sec}^{-1}$$

$$N_1 = 6.860 \times 10^{13} \text{sec}^{-1}$$

$$N_2 = 1.564 \times 10^7 \text{ sec}^{-1}$$

$$N_3 = 1 \text{ sec}^{-1}$$

$$D_0 = 8.264 \times 10^{19} \text{ sec}^{-1}$$

$$D_1 = 1.372 \times 10^{14} \text{ sec}^{-1}$$

$$D_2 = 4.691 \times 10^7 \text{ sec}^{-1}$$

$$D_3 = 4 \text{ sec}^{-1}$$

These are the coefficients that were entered into the computer to produce Figure A.2.

Now, the transfer function for Figure A.3 is derived. The transfer function for this system is

$$\frac{V_0(s)}{V_i(s)} = \frac{Y_2}{Y_0 + Y_1 + Y_2} \qquad \text{(A.16)}$$

The sum in the denominator has been calculated; it is Y_L (see Equation A.6). So then, the numerator of the transfer function is

$$N(s) = (s+w_0)(s+w_1) \qquad \text{(A.17)}$$

and the denominator is

$$D(s) = (s+w_0)(s+w_1) + (s+w_1)(s+w_2) + (s+w_0)(s+w_2) \quad (A.18)$$

These can be expanded into standard form:

$$N(s) = N_2 s^2 + N_1 s + N_0 \quad (A.19)$$

and

$$D(s) = D_2 s^2 + D_1 s + D_0 \quad (A.20)$$

where

$$N_0 = w_0 w_1$$
$$N_1 = w_0 + w_1$$
$$N_2 = 1$$
$$D_0 = w_0 w_1 + w_1 w_2 + w_0 w_2$$
$$D_1 = 2(w_0 + w_1 + w_2)$$
$$D_2 = 3$$

For the values of capacitors and resistors used

$$N_0 = 4.132 \times 10^{13} \text{ sec}^{-1}$$
$$N_1 = 1.364 \times 10^{7} \text{ sec}^{-1}$$
$$N_2 = 1 \text{ sec}^{-1}$$
$$D_0 = 6.860 \times 10^{13} \text{ sec}^{-1}$$
$$D_1 = 3.127 \times 10^{7} \text{ sec}^{-1}$$
$$D_2 = 3 \text{ sec}^{-1}$$

These are the coefficients that were entered into the computer to produce Figure A.4.

Conclusions

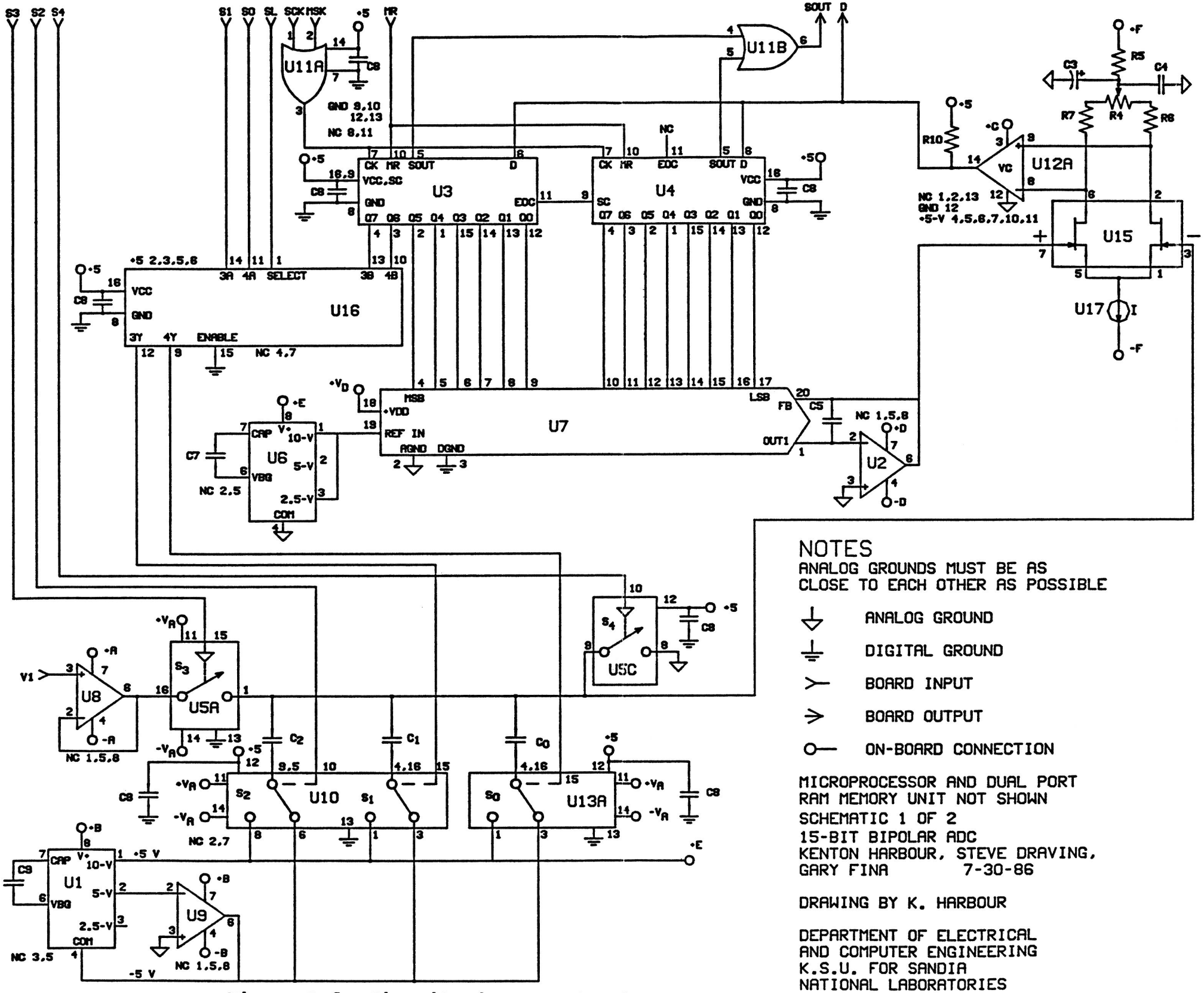
The main purpose for these calculations is to support the calculation of the system average power consumption.

Specifically, it is necessary to know the amount of time the S/H input buffer must be on to acquire the input. And the time required to test each bit must be known so that the total conversion time can be calculated.

The plots shown in Figure A.2 and Figure A.4 are useful for evaluating the type of response the system has in each of the two different configurations, but it is impossible to use the graphs to determine the exact time when the S/H output has settled to within 1/2 LSB, or to within 15 ppm of its final value. A tabular output must be used to obtain this figure.

Unfortunately, the program only presented tabular outputs with four significant digits, a resolution of 100 ppm. According to this output, the S/H will acquire the input and settle to within 100 ppm of its final value in 11.70 us. During the test of the S/H's MSB, it will take 2.525 us for the output to settle to within 100 ppm. In the text much more conservative values were used. They were 30 μs for the input acquisition time, and 20 μs for the test of each bit. Again, the best estimates will be obtained by laboratory evaluation of the circuit itself.

APPENDIX B. CIRCUIT DIAGRAM AND PARTS LIST



NOTES

ANALOG GROUNDS MUST BE AS CLOSE TO EACH OTHER AS POSSIBLE

- ANALOG GROUND
- DIGITAL GROUND
- BOARD INPUT
- BOARD OUTPUT
- ON-BOARD CONNECTION

MICROPROCESSOR AND DUAL PORT RAM MEMORY UNIT NOT SHOWN

SCHEMATIC 1 OF 2

15-BIT BIPOLAR ADC

KENTON HARBOUR, STEVE DRAVING, GARY FINA 7-30-86

DRAWING BY K. HARBOUR

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
K.S.U. FOR SANDIA NATIONAL LABORATORIES

Figure B.1 Circuit Diagram of Switched-Capacitor DAS (Schematic 1 of 2)

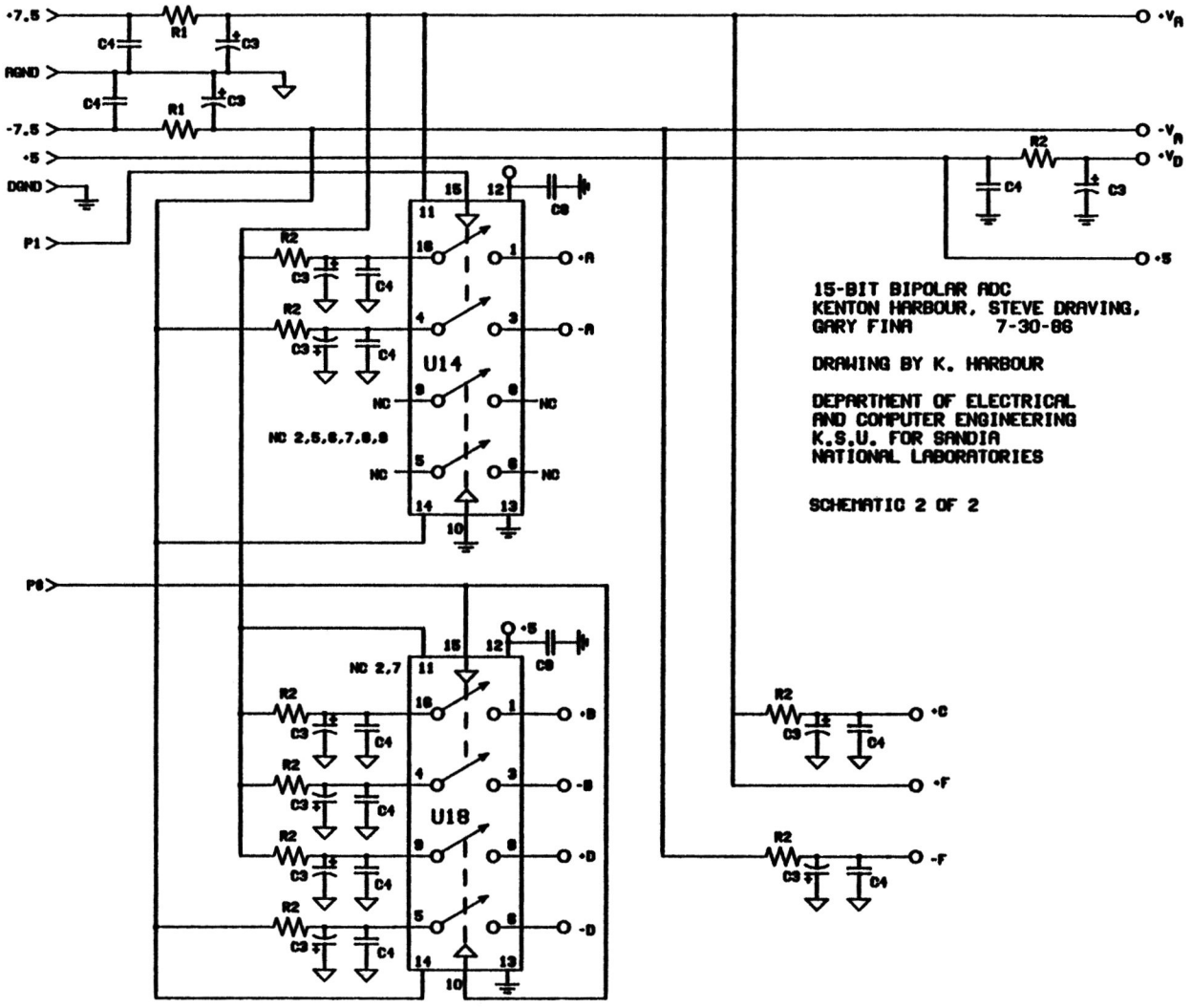


Figure B.2 Circuit Diagram of Switched-Capacitor DAS (Schematic 2 of 2)

Parts List

Integrated Circuit Components

DEVICE	FUNCTION	PART#	MFG.	#PINS
U1	Voltage Reference	AD584	Analog Devices	8
U2	Low-Noise Op Amp	OP-37	PMI	8
U3	SAR	MC14549	Motorola	16
U4	SAR	MC1449	Motorola	16
U5	Dual DPST Switch	DG5145	Siliconix	16
U6	Voltage Reference	AD584	Analog Devices	8
U7	CMOS 14 Bit DAC	DAC-HA14B	Datel-Interstil	20
U8	Low-Noise Op Amp	OP-27	PMI	8
U9	BIFET Op Amp	AD547	Analog Devices	8
U10	Dual SPDT Switch	DG5143	Siliconix	16
U11	Quad 2-Input OR	MM74HC32	Nat. Semi.	14
U12	Quad Comparator	CMP-04	PMI	14
U13	Dual SPDT Switch	DG5143	Siliconix	16
U14	Dual DPST Switch	DG5145	Siliconix	16
U15	Monolithic Dual JFET	U401	Siliconix	6
U16	Quad 2-Input Mux	MM74HCT157	Nat. Semi.	16
U17	Current Regulator Diode	CR022	Siliconix	2
U18	Dual DPST Switch	DG5145	Siliconix	16
U20*	Dual-Port RAM	MCM68HC34	Motorola	40
U24*	Microprocessor	MC68HC11	Motorola	48
		Total no. of pins		312

*** Not shown on schematic**

Resistors

DEVICE	VALUE (ohms)	DESCRIPTION	QTY.
R1	1	5% Carbon	2
R2	10	5% Carbon	9
R4	500	Multiturn Pot.	1
R5	20K	1% Metal Film	1
R6	10.2K	1% Metal Film	2
R10	100K	5% Carbon	1

Capacitors

DEVICE	VALUE (uF)	DESCRIPTION	QTY.
C0	0.0011	Teflon*	1
C1	0.0022	Teflon	1
C2	0.005	Teflon	1
C3	10	Tantalum	12
C4	0.01	Ceramic	12
C5	59 pF	Ceramic	1
C7	0.01	Ceramic	1
C8	0.01	Ceramic	9
C9	0.001	Ceramic	1

* obtained by placing two 0.0022 uF capacitors in parallel

A DATA ACQUISITION SYSTEM WITH SWITCHED CAPACITOR SAMPLE-AND-HOLD

by

KENTON DEAN HARBOUR

B. A., Mid-America Nazarene College, 1984

AN ABSTRACT OF A MASTER'S THESIS

submitted in partial fulfillment of the
requirements for the degree

MASTER OF SCIENCE

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1986

Abstract

A preliminary design of a 15-bit data acquisition system for low frequency, low power, signal processing applications is described. Major design features include 33.7 mW power consumption, 94 dB dynamic range, 500 Hz sampling rate, and a bipolar input range (±5 V). The design requires no custom components, and it may be possible to fit the circuit on a single 3"x5" printed circuit board.

Power switched analog components are used to minimize power consumption, and a switched capacitor sample-and-hold is used to obtain 15-bit resolution with only a 14-bit DAC. In effect, the switched capacitor sample-and-hold is a low resolution ADC with an intrinsic sample-and-hold capability. The switched capacitor sample-and-hold is used to make a rough estimate of the input voltage that is refined by the 14-bit DAC to produce the data acquisition system's high resolution output. A linearization algorithm, executed by an onboard microcomputer, can correct for errors due to capacitor mismatch and variations due to temperature.

A one-channel wire-wrapped system has been constructed to test the design. The test system will also indicate the best method of adding a second input channel. The power consumption for a two channel system is expected to be less than 60 mW.